# Improvement of Thin Gate Dielectrics Reliability by High Temperature Oxidation using N<sub>2</sub>O and O<sub>2</sub> Ambient

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Abstract: - In this paper, we proposed the high temperature oxidation method to grow thin gate dielectric film  $(EOT < 30 \text{\AA})$  in dilute N<sub>2</sub>O and O<sub>2</sub> ambient. As the previous study, nitrogen incorporation can promote the gate oxide reliability. However, excess nitrogen incorporation will also deteriorate performance of gate dielectrics. Therefore, we grew the gate dielectrics at high temperature for very short time. Due to dilute N<sub>2</sub>O gas, the electrical properties of the gate dielectrics can be improved. In addition, this film exhibits relatively weak temperature dependence due to a Fowler-Nordheim (FN) tunneling mechanism. It appears to be promising for future VLSI devices.

Key-Words: - gate oxide, time to breakdown, charge to breakdown, SILC, nitrogen, N<sub>2</sub>O and thin gate oxide.

## **1** Introduction

As the device scaling down, the shrinking of thermal  $SiO_2$  as the gate dielectric has run into difficulties due to excess leakage current [1]. Moreover, the device performance degradation by stress induced leakage current (SILC) was more and more severe along with the scaling of thermal gate dielectrics [2]. However, to increase the driving current of devices is essential. Thus, searching for an alternative gate dielectric, such as high-k material, or new methods to grow a high quality gate dielectric film has been studied in future ULSI technology.

Previous studies have shown that nitrogen incorporating at SiO<sub>2</sub>/Si interface can protect the gate dielectrics against boron penetration and enhance its However, the excessive reliability [3], [4]. incorporation of nitrogen will not only increase the interface roughness but also transfer the leakage mechanism from F-N tunneling to F-P tunneling. In early work, these kinds of gate dielectrics were prepared by annealing oxide in NH<sub>3</sub> or using NO or N<sub>2</sub>O for surface nitridation before the gate dielectrics formation. However, the gate dielectrics annealed by NH<sub>3</sub> will results in a high density of electron traps due to the presence of hydrogen [5], [6]. And the oxynitride prepared in N<sub>2</sub>O or NO has been observed several issues such as hot carrier induced degradation, increase of oxide charge and the mobility degradation. [7], [8].

In this work, we propose the high temperature oxidation in dilute  $N_2O$  and  $O_2$  ambient. It preserved the advantages of nitrogen incorporation in oxide reliability, and had oxide-like characteristics in

current transportation due to short process duration which can avoid excess nitrogen atoms incorporation.

Q field oxide isolation : 500nm

) gate dielectrics formation : N<sub>2</sub>O:O<sub>2</sub>=1:10, at 900°C

poly-gate deposition: LPCVD 150nm, at 620°C.

implantation : Phosphorus of 30keV, 5E15cm<sup>-2</sup>

dopant activation : RTA at 950°C for 30s

metalization : AI (500nm)

#### Fig. 1 MOS capacitors fabrication process flow

## 2 **Experiments**

Fig. 1 shows the process flow for the fabrication of MOS capacitors in our experiment. Following a standard Radio Corporation of America (RCA) cleaning process, a 500nm-thick field oxide was thermally grown on the p-type (100) oriented Si wafer with 3-5  $\Omega$ -cm at 1050°C for one hour. After isolation oxide formation, the active regions were defined by photolithography and etched by BOE (Buffer oxide etcher) solution. Subsequently, RCA clean was performed for eliminating the contamination. Then, the gate dielectrics were thermally grown for less 1 minute at 900°C in dilute oxygen ambient (N<sub>2</sub>O:O<sub>2</sub> = 1:10). The control samples were fabricated in the same conditions except the N<sub>2</sub>O gas. After formation of gate dielectrics, we immediately deposited a vapor

deposition (LPCVD) system. Next, all capacitors were implanted by phosphorus of 5E15cm<sup>-2</sup>, 30keV. Continuously, the rapid thermal annealing was performed for dopants activation at 950°C for 30s. The next stage is to deposit the Aluminum films of 500nm on the topside of the wafer and pattern Aluminum and poly-silicon as the electrode. Finally, deposit backside electrode and sintered both top and backside electrode at 400°C. The equivalent oxide thickness (EOT) was determined from C-V in strong accumulation region considering quantum mechanical effects and the electrical properties and reliability characteristics of MOS capacitors were measured by using the Hewlett-Packard (HP) 4156B semiconductor parameter analyzer and Keithley-82 system.

#### **3** Results and discussion

Here, Fig. 2 shows the -J-E curves of all samples. It reveals the fact that samples fabricated in dilute N<sub>2</sub>O ambient has a slightly small leakage current compared with samples fabricated in pure O<sub>2</sub> ambient. And they also have a larger breakdown voltage than controls. Fig. 3 indicates the C-V characteristics of all samples. The measured capacitor area is  $3.14 \times 10^{-4}$  cm<sup>2</sup> and the equivalent oxide thickness for two groups extracted from capacitance in accumulation region is 28Å and 29Å respectively. In previous studies, excess nitrogen incorporation will produce some defects or increase the interface states or oxide charges which can be indicated in C-V plots [10].



Fig.2 The -J-E characteristics of gate dielectrics grown in dilute  $N_2O$  ambient.



Fig.3 The high frequency C-V plots of all samples. There is no obvious increase of interface states and fixed oxide charge in dilute  $N_2O$  conditions.

However, there is no evidence in Fig. 3. In other words, in our experiments, formation gate dielectrics at high oxidation temperature in a short period will not significantly increase the interface states or any oxide charges. It demonstrates that by this method will not cause serious oxide damages. Fig. 4 exhibits the Weibull plots of electrical breakdown field ( $E_{bd}$ ) for all samples. The gate dielectrics developed in dilute N<sub>2</sub>O ambient have a larger  $E_{bd}$ . It is believed that nitrogen can replace the weak bonds, Si-H and Si-OH, to form strong Si-N bonds at the interface of SiO<sub>2</sub>/Si [9]. This formation will improve the GOI and have progressed in  $E_{bd}$ .



Fig. 4 The Weibull characteristics of electric field to breakdown (Ebd) measurement.

In Fig. 5, shows the Weibull plots of Charge to breakdown ( $Q_{bd}$ ) for two kinds of samples. Capacitors with nitrogen incorporation have a better  $Q_{bd}$  due to passivating the weak bonds at SiO<sub>2</sub>/Si interface or forming O-N bonds which will strengthen the gate dielectrics quality. By this way, the issues of stress induced leakage current (SILC) also can be improved (in Fig. 6)



Fig. 4 The Weibull characteristics of electric field to breakdown (Ebd) measurement.

Fig. 6 shows the results after constant current stress of -10uA for samples with nitrogen incorporation. No significant SILC was observed after  $6x10^3$ -s stressing. In this figure, the leakage will be saturated after stress for a period. And if the stress current is larger than 0.1mA, soft breakdown will easily occur (Fig. 7).



Fig.6 The SILC characteristics by constant current stress of N<sub>2</sub>O samples.



Fig.7 The current voltage characteristics of the capacitor before and after soft breakdown and hard breakdown.

Fig. 8 shows the voltage to breakdown with constant voltage stress for capacitors with nitrogen incorporation. And Fig. 9 illustrates the lifetime projection for all samples. And samples fabricated in dilute  $N_2O$  and  $O_2$  ambient shows a longer lifetime.



Fig.8 Voltage to breakdown with constant voltage stress of -4.3V.

Fig. 10 shows fitting curve of the Fowler – Nordheim tunneling model:

and it demonstrates the F-N tunneling instead of F–P conduction dominates the current transport in our samples.



Fig.9 Comparison of intrinsic lifetime projection for gate dielectric film grown in different conditions.



Fig.10 F-N tunneling fitting plots for samples fabricated at high oxidation temperature in dilute  $N_2O$  ambient.

### 4 Conclusion

In conclusion, thin gate dielectrics (EOT <30Å) were fabricated in dilute N<sub>2</sub>O and O<sub>2</sub> ambient for a very short time. By this way a proper amount of nitrogen will be incorporated. Such films exhibit lower leakage than their thermal oxide counterparts. The current transport properties of this film are different from conventional nitrogen-rich gate dielectric film. The F-N tunneling instead of F-P tunneling dominates the current transport in our gate dielectric film, which weakens the temperature dependence. The long T<sub>bd</sub> of this film is attributed to

its low leakage current. SILC and C-V measurement indicated that there is little charge trapping and trap generation in this gate dielectric film. These results suggest that this film may be considered as a potential candidate for future ULSI applications.

References:

- C. Hu, "Gate oxide scaling limits and projection," in IEDM Tech. Dig., pp. 319-322, 1996.
- [2] C. C. Chen, C. Y. Chang, C. H. Chien, T. Y. Huang, H. C. Lin, and M. S. Liang, "Temperature-accelerated dielectric breakdown in ultra thin gate oxides," Appl. Phys. Lett., vol. 74, pp. 3708–3710, 1999.
- [3] E. P. Guse, H. -C. Lu, E. L. Garfunkel, T. Gustafsson, and M. L. Green, IBM J. Res. Dev. 43, p. 265, 1999.
- [4] M. L. Green, D. Brasen, L. C. Feldman, E. Garfunkel, E. P. Gusev, T. Gustafsson, W. N. Lennard, H. C. Lu and T. Sorsch, in Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices, 1998.
- [5] L. K. Hanetal., "Recent development in ultra thin oxynitride gate dielectrics," Microelectron. Eng., vol. 28, pp. 89–96, 1995.
- [6] S. K. Lai, D. W. Dong, and A. Hartstein, "Effects of ammonia anneal on electron trapping in silicon dioxide," J. Electrochem. Soc., vol. 129, pp. 2042–2044, 1982.
- [7] J. F. Zhang, H. K. Sii, Guido Groeseneken, Senior Member, IEEE, and R. Degraeve, "Degradation of Oxides and Oxynitrides Under Hot Hole Stress," *IEEE Trans. on Electron Devices*, vol. 47, pp. 379-386, 2000.
- [8] Tung Ming Pan, Student Member, IEEE, Tan Fu Lei, Member, IEEE, Huang Chun Wen, and Tien Sheng Chao, Member, IEEE, " Characterization of Ultra thin Oxynitride (18–21Å) Gate Dielectrics by NH<sub>3</sub> Nitridation and N<sub>2</sub>O RTA Treatment," *IEEE Trans. on Electron Devices*, vol. 48, no. 5, 2001
- [9] Hei Wong; Gritsenko, V.A.; "Dielectric traps in amorphous silicon oxynitride," *Electron Devices Meeting, IEEE Hong Kong*, 30 June 2001.
- [10] Rideau, D.; Scheer, P.; Roy, D.; Gouget, G.; Minondo, M.; Juge, A.; "Series resistance estimation and C(V) measurements on ultra thin oxide MOS capacitors," *Microelectronic Test Structures*, 2003. International Conference, 2003