Inductor Modeling of Integrated Passive Device for RF Applications

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Abstract: - In this paper, an integrated passive device (IPD) inductor modeling is demonstrated. The IPD technology is a system in package (SiP) solution where passive devices with high quality can be fabricated on a chip and then connect with another circuit chip by using flip-chip micro-bump bonding. For an RF circuit simulation, the IPD inductor model is built and verified from the measurement results.

Key-Words: - integrated passive device, system in package, flip-chip, inductor modeling

1 Introduction

The integration of on-chip spiral inductors in CMOS process for RF applications has been the subject of many researches. In standard CMOS process, the Q factor is restricted by the metal resistance and by the substrate eddy current losses. Many technology modifications are employed to improve the Q factor [1-8]. Burghartz, et al. [1] used additional substrate contacts to improve the Q factor. Park [2] modified the internal diameter of spiral inductor layout to reduce the substrate losses. Yue [3] proposed a patterned ground between the inductor and substrate for shielding. Octangle spiral inductor and symmetrical structure were suggested by [4, 5]. Post processing, copper interconnect, and low dielectric material were demonstrated by [6, 7, 8]. Nevertheless, the ever best reported quality (Q) factors are between 10~20 [9, 10], depending on the technology. Moreover, on-chip inductor modeling is difficult and is typically limited to accuracy below 10%.

To achieve a high Q factor inductor, system in package (SiP) technology seems to be an interesting and reasonable solution. Multi-layer ceramic (MLC) and multi-chip module (MCM) are two most attractive SiP technologies. MLC technology can integrate passive devices with high Q value around 80 [11, 12], but the process cost needs to be cut. MCM technology employs lower cost flip chip packaging where passive devices with high quality can be fabricated on a chip and then connect with another circuit chip by using flip-chip micro-bump bonding [13, 14]. The passive devices fabricated can achieve a Q value higher above 50. GaAs MMIC and silicon component had been integrated together by MCM technology for RF application [15]. CMOS chips and passive devices integrated by MCM technology for RF applications were also reported in [16, 17].

Circuit simulations with accurate models are the success key for RFIC designers. For CMOS process technologies after 0.25um, the manufacturer would provide RF models for transistors and on-chip spiral inductors. The transistor models have no choice but to be used. Nonetheless, aside from the lower Q factor, the on-chip inductor models are typically limited to accuracy below 10%. Domestic manufacturer [18] supports MCM packaging as well as high Q inductors fabricated by integrated passive device (IPD) technology. Hence, in this paper, to use the IPD inductor for CMOS RFIC designs, the IPD inductor models are built and verified from the measurement results. The models are used in designing a cascode LNA employing IPD inductors. The simulation results show its superiority when compared with conventional on-chip inductor LNA.

2 Inductor Modeling

In this section, the flow to build an inductor model is described step by step and illustrated by an example. The example is a 2.5-turn on-chip rectangular spiral inductor fabricated by 0.25μm 1P5M CMOS process.

2.1 Modeling Steps

The first step is to choose the desired inductor to be modeled. A 2.5-turn on-chip rectangular spiral inductor is chosen, and its layout is shown in Fig.1. Some physical parameters of the process, including the thickness of metal layer and oxide layer, the

dielectric constant, etc., are required to perform an electromagnetic simulation by using Agilent's ADS. The distribution of electromagnetic field of the inductor would be calculated and analyzed. From these analysis and calculations, a set of S parameters will be derived.

The second step is to construct an equivalent circuit based on the layout and inductor structure. A corresponding equivalent circuit [19] is shown in Fig.2. L_s and R_s are the series inductor and resistor. C_p is the capacitor for inter-metal and metal overlap. C_{ox} is the capacitor between metal and substrate ground. R_{sub} and C_{sub} serve for substrate loss. Using the S parameters derived at the previous step, a set of conversion equations are applied to calculate component values of the equivalent circuit [20].

The next step is to verify the equivalent circuit model by measurements on a manufactured inductor testkey. The actual S parameters are measured. If these parameters have an unacceptable mismatch from the simulation values, perform the second step for these measured parameters to find a convergence.

2.2 Simulation and Measurement

An example of 2.5-turn on-chip rectangular spiral inductor was fabricated by 0.25μm CMOS process. The measurements were performed by using on-wafer probing with Agilent 8510 sited on CIC, as shown in Fig.3. Calibration and de-embedding were carefully carried out, respectively.

The measurement results compared with simulation results are shown in Fig.4 for R_s, L_s and Q, respectively. From these figures, the measured results outperform simulation ones, we can expect that our simulation model is a little conservative, especially in higher frequency. Since, we are only interested in the 5GHz band, the results are acceptable.

3 IPD Inductor Modeling

To overcome the inherent substrate loss of CMOS on-chip inductor, integrated passive device (IPD) inductors employing flip chip packaging are developed. Fig.5 is the illustration of multi-chip module packaging. A CMOS circuit chip with active devices and a IPD chip with passive devices are fabricated, and then micro-bump bonding is used to interconnect these two chips.

To use the IPD inductors in RF circuit designs, models of the IPD inductors are needed. Testkeys are fabricated and measured. The measured S parameters are converted to the simulation models using the steps described in Section 2. Fig.6 is a 3.5-turn IPD inductor. Its measurement results and simulation results are shown in Fig.7 for R_s, L_s, and Q, respectively. The results are well matched. Its Q value is about 40 at 5GHz. Table 1 lists the comparisons of IPD and on-chip inductors. With the same inductor values, IPD inductor has smaller resistance and higher Q value. The area is a little larger than on-chip inductor due to bonding pads, however it is much smaller than off-chip inductor.

To demonstrate the superiority of IPD inductor over on-chip inductor, two cascode LNAs using different inductor realizations are designed, as shown in Fig.8. The simulation results are listed in Table 1. Operating at the same supply voltage and power consumption, the IPD-inductor LNA has lower NF and higher gain than the on-chip-inductor LNA. The LNAs were submitted to CIC for fabrication.

4 Conclusion

In this paper, an integrated passive device (IPD) inductor modeling is demonstrated. The inductor models are built by measuring S parameters of testkey, and then converting into simulation model. To manifest the superiority of the IPD inductors, the derived models are used to design two cascode LNAs with on-chip and IPD inductors, respectively. The simulation results show that the IPD-inductor LNA has lower NF and much higher gain than the on-chip-inductor LNA. The IPD technology which has high quality passive device and compatible with CMOS process is a promise for RF applications.

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Table 1 Comparisons of IPD and on-chip inductors

Inductor	R(Ω)	L(nH)	Q 5.2GHz	Area	Integration
On-chip L	3.42	2.17	7	$250\mu m \times 300\mu m$	On-chip
IPD L	0.54	2.27	38	$400\mu m \times 400\mu m$	Flip-chip

Table 2 Comparisons of LNAs

Cascode LNA	Voltage (V)	Current (mA)	NF (dB)	Gain (dB)	S11 (dB)	S12 (dB)	S22 (dB)	P_{1dB} (dBm)
On-chip L	2.5	6.32	3.45	9.3	-8.9	-23.3	-10.8	-4
IPD L	2.5	6.32	2.37	15.2	-8.5	-20	-14	-10

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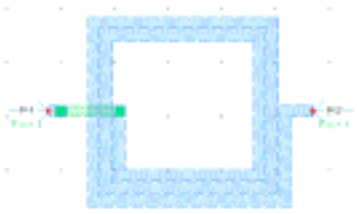

Fig.1 A 2.5-turn spiral on-chip inductor

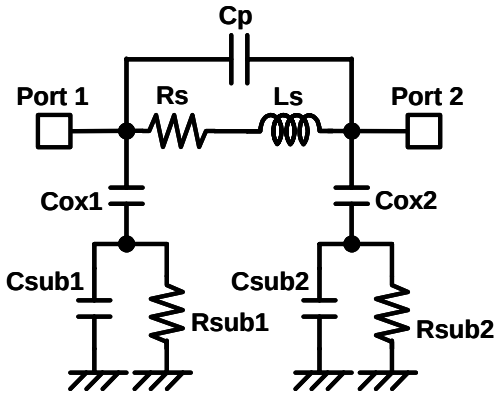

Fig.2 Equivalent circuit of on-chip inductor

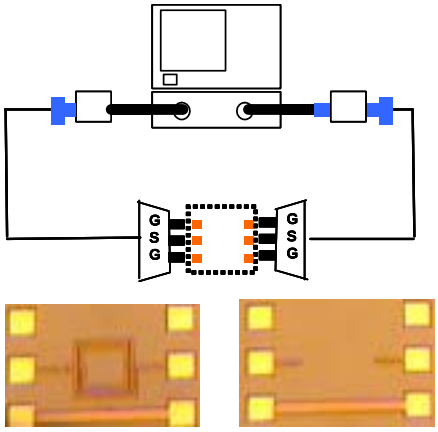

Fig.3 The measurement setup and chip photos

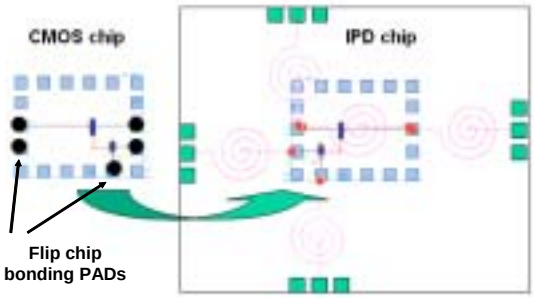

Fig.5 The flip-chip microbump bonding

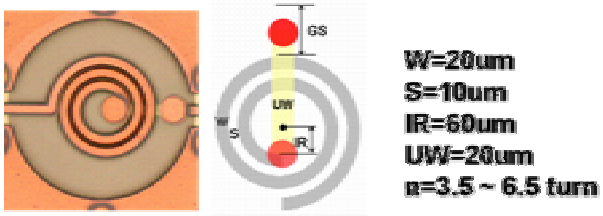

Fig.6 The IPD inductor

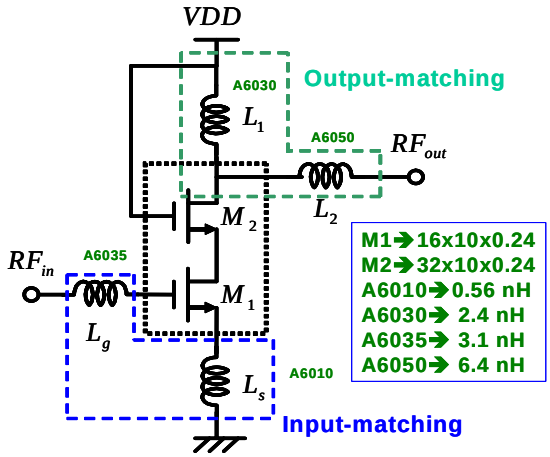

Fig.8 The Cascode LNA

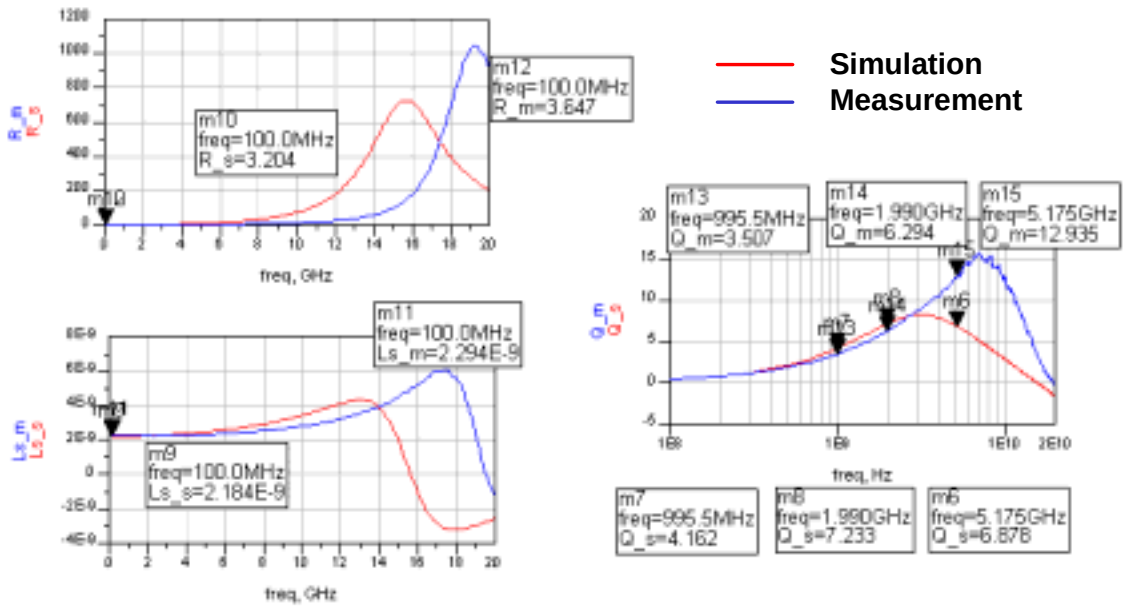

Fig.4 Measurement and simulation results of on-chip L

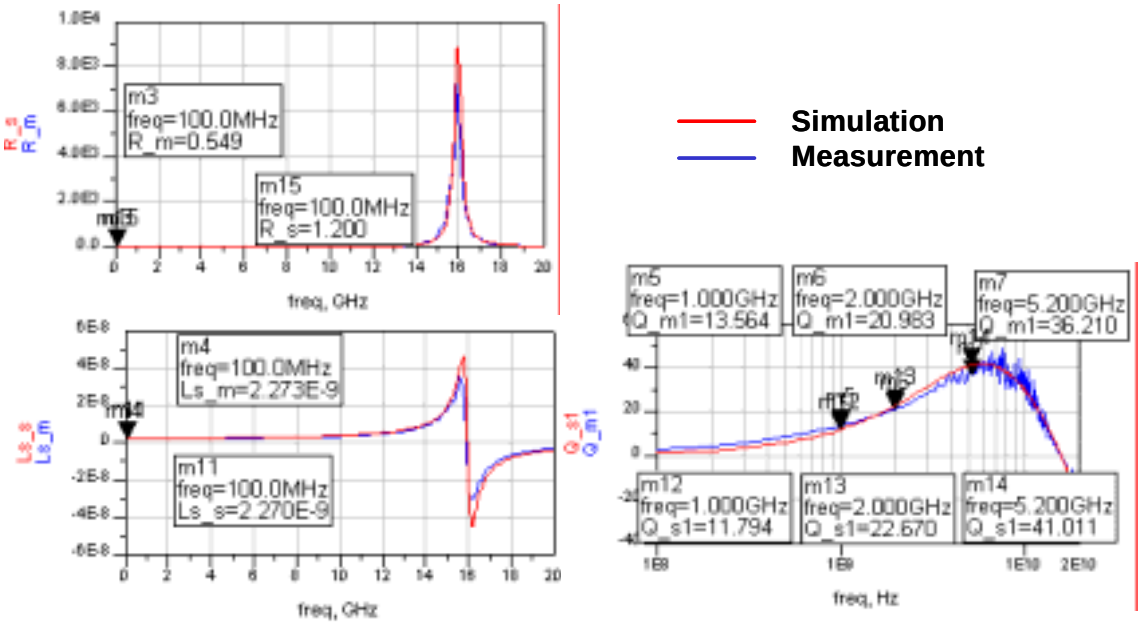

Fig.7 Measurement and simulation results of IPD L