Testing of Infrared Focal Plane Array

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Abstract: - The increase in array size and decrease in pixel size make the testing of infrared focal plane array (IR FPA) being difficult. In this paper, I will demonstrate a test socket chip for easily testing large array size FPA by measuring dark currents of IR sensors. A calibration technique of leakage current is applied to certify the correctness of measurement. I will also show a crosscheck test scheme for efficiently testing FPA. For an array size of M by N, the testing times can be reduced from the order of M*N to M+N. Analysis on the detection of proposed fault model by the crosscheck test scheme is also presented in this paper.

Key-Words: - Test Socket Chip, Infrared, Focal Plane Array, Built-in Test, Crosscheck Test, Fault Model

1 Introduction

Large array and small pixel are essential to achieve high-resolution infrared (IR) focal plane array (FPA) for applications in military, medical and astronomy, [1-4]. There are two major parts in an IR FPA : a sensor array and a readout circuit, [5-8]. The sensor array could be a two dimensional array of photovoltaic IR detectors. One type of photovoltaic detector, InSb P-N junction device, and its I-V characteristic curve are shown in Fig.1. The readout circuit is used to bias the sensor and provide an interface for accessing the sensed signal. CMOS readout circuits are now commonly used, [9,10]. Indium bump flip chip technology, as shown in Fig.2, is applied to consolidate the readout circuit chip and the sensor array chip.

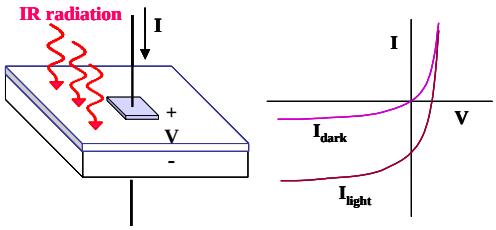


Fig.1 A photovoltaic detector

The increase in array size and decrease in pixel size will unavoidably increase the number of defects during manufacturing and packaging. The high density flip chip package will also make the testing of FPA being even more worse. Hence, it is urgent to find economical and efficient test methods for the detector array and readout chips of a large size FPA.

To test the readout circuit, current sources built in the readout circuit itself to replace the function of sensor cell during testing had been proposed in [12-14]. To test the sensor array before packaging, the sensor cell can be probed directly for measuring its characteristic, [15,16]. Nevertheless, the total probe time will be proportional to the array size and become unacceptable when the array size grows large. Beside that, each time when the probe contact on a cell there will exist uncertainty problems. In [17], we had demonstrated a test socket chip for efficiently testing large array size FPA at one-time contact. The test socket chip with RAM-like access capability can select individual cell for measuring dark current. A modification on the cell selection scheme to allow different selection mode had also been proposed to calibrate unwanted leakage current when performing the current measurement, [18].

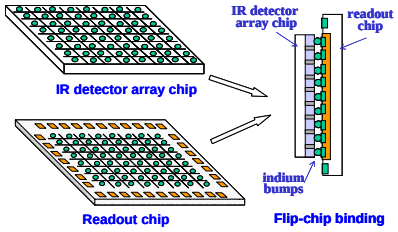


Fig.2 Flip chip packaging

All the above mentioned methods test a cell each time, for an array size of M by N, M*N times of tests are at least required to test every cell once. To reduce the total number of testing times, we had proposed a parallel test scheme, called crosscheck test, [19]. Column by column and row by row, crosscheck test is performed with a modified cell selection maneuver. Hence, the testing times can be reduced from the order of M*N to M+N. Based on

the test scheme, a fault model and its detectability are unveiled in [20].

In this paper, the test socket chip and calibration method are demonstrated in section 2. The crosscheck test scheme and fault model are presented in section 3. A conclusion is made in the final section.

2 Test Socket Chip

To reduce the cost of flip chip packaging, it is necessary to have a functional examination on the detector array before the flip chip process to ensure a high yield. The dark current of IR detector is a favorable candidate to be examined. A small dark current means a good dynamic performance of detectors. A large dark current will lessen the performance of the detector as well as the normal operation of the readout circuit. Hence, it is a good practice to characterize the dark current for the testing of detector array.

2.1 Test Socket Circuit for Measuring Dark Current

To measure dark currents, the detectors can be directly probed at their bump pads. However, the direct probing method can only probe a pixel each time and requires time-consuming setup for each probe. Besides, the uncertainty of the probing contact and interference from open environment would both make the measuring being more difficult. A test socket chip, which contacts with the whole detector array via aligned bump pads, can inherently segregate the uncertainty, was proposed to overcome these difficulties, [17].

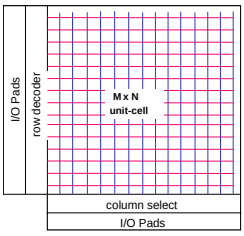


Fig.3 Architecture of test socket chip

The proposed test socket chip, whose accessing resembles random access memory, is shown in Fig.3. Each detector will be directly accessed through the selection of address lines. When addressed, as shown in Fig.4(a), a measuring path connecting the selected detector to an I/O pad is constructed through a series of switches. The dark current is then measured by applying a reverse bias on the detector.

Nevertheless, there will be a lot of switches at OFF-state tied to the measuring path. All these OFF-state switches will contribute a small leakage current, I_{OFF}, to the path, and totally will have a fairly influence on the measuring result. Hence, it is necessary to calibrate these unwanted leakage currents to get the exact value of the detector's dark current.

2.2 The Calibration Scheme for the Leakage Current

Due to the leakage current of OFF-state switches, the measured current will have a large error when the array size increases. To cancel these unwanted leakage currents, by slightly modifying the address decoder, we had proposed a calibration scheme in [18].

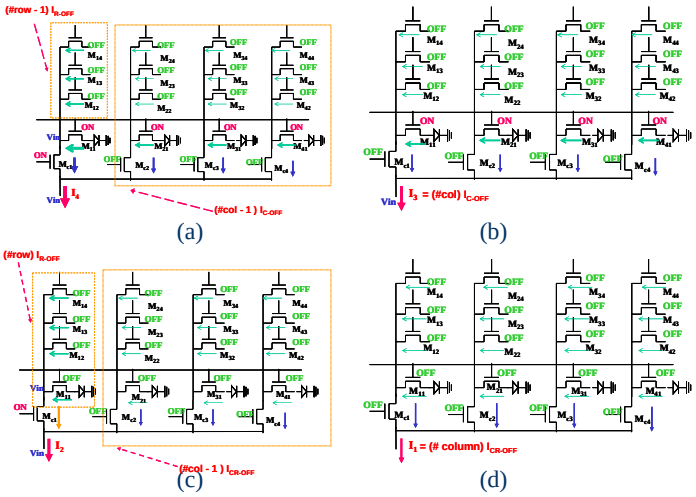


Fig.4 The four cases of pixel selection

Two extra control I/O pins are used to disable the address selection. That is, even the address has been applied, the output of the selected decoder is still disabled. Accordingly, there are four cases for the two control inputs, as shown in Fig.4. Case 1 is that both the addressed row and column are disabled. All the switches are at OFF-state. Case 2 is that the addressed row is disabled while the addressed column is enabled. Therefore, only the addressed column switch is ON and all other switches are OFF. Case 3 is that the addressed row is ON and the addressed column is OFF. Thus, all the switches at the addressed row are ON, while all other switches are OFF. Case 4 is the normal selection. Only one row and one column are enabled to select a pixel. Hence, all the switches along the addressed row are ON, and the switch of the addressed column is ON.

For each pixel, by measuring the currents under these four cases, four currents, namely I_4, I_3, I_2, and I_1, are measured. Based on the relationship of the

four measured currents derived in [18], we can calibrate the leakage and get the accurate detector's dark current to be $I_D = I_4 - k_1I_3 - k_2I_2 + k_1k_2I_1$, where k_1 = (#col–1)/#col, k_2= (#row–1)/#row, #col and #row are the number of columns and rows, when #row and #col are large enough, (i.e., k_1, k_2 >>1), the dark current will be $I_D \cong I_4 - I_3 - I_2 + I_1$.

2.3 Implementation

We had designed a test socket chip for a 128 x 128 IR FPA whose unit pixel size is 30um x 30um. In our test socket chip, the unit cell includes 3 NMOS switches, a small size P+/N-Well diode for testing purpose, and a bump pad. Fig.5 is its schematic and layout. The technology used is 0.5 μm 2P2M CMOS process. The layout is shown in Fig.6. The chip size is 4518 um x 4364 um. It has been fabricated through MPC service of Chip Implementation Center (CIC). The chip has been verified. An automatic measuring system, as shown in Fig.7, which is under developing at National Chi Nan University.

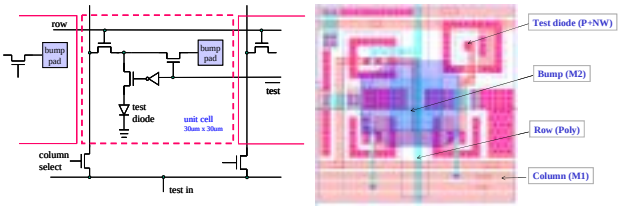


Fig.5 Schematic and layout of unit cell

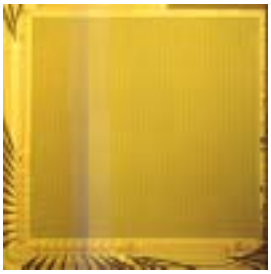


Fig.6 The photo of 128x128 test socket chip

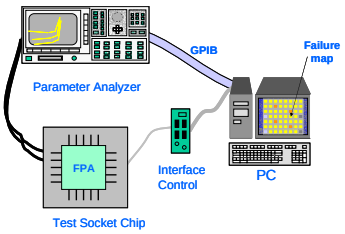


Fig.7 Automatic measurement system

3 Crosscheck Test Scheme

To accelerate the testing times of a large size FPA, a parallel test scheme, called crosscheck test, was proposed in [19]. Column by column and row by row, the testing times can be reduced from the order of M*N to M+N. Based on the crosscheck test scheme, a fault model and its detectability are also discussed in this section.

3.1 Built-In Current Source for Readout Circuit

A readout chip for FPA consists of a row decoder, a column selector, and a two-dimensional array of unit cells for sensor readout, as shown in Fig.3. The unit cell, as depicted in Fig.8, contains a bump pad for sensor binding, a readout circuit, and a row-select MOS switch. Each sensor cell in the FPA will be sequentially accessed through the row and column selections. The row decoder and the column select are generally realized by shift registers with MOS selecting switches. In normal operation, only one DFF in row shift register and one DFF in column shift register are set to activate the row's and column's MOS switches respectively. Hence, a row is addressed and a cell in the addressed row are selected.

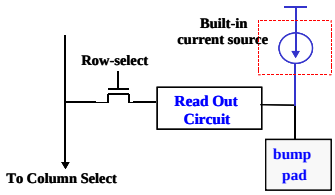


Fig.8 The unit cell with built-in current source

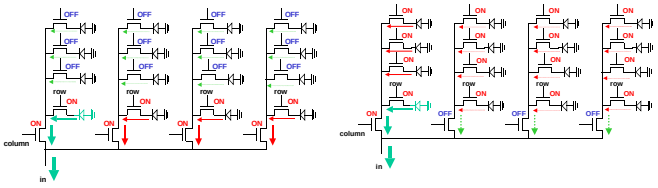
Before the flip chip binding, the bump pad is floating, hence the readout circuit can not operate functionally and be tested. A possible testing method is to include a current source, as shown in Fig.8, attached to the bump pad. During testing, the function of sensor will be replaced by the built-in current source that can provide a current to the readout circuit. By measuring the current, the readout chip can be verified.

3.2 The Crosscheck Test Scheme for FPA

To test a large size FPA, conventional methods need at least M*N times of tests to exercise all pixels (for convenient, we assume that M is the number of columns and N is the number of rows). When the array size grows large, the testing time becomes unacceptable. In order to reduce the test times, a parallel test scheme, called crosscheck test, was proposed in [19].

To perform crosscheck test, the shift register in readout circuit must have the functions of *clear*/

preset and *load*. In normal operation, each time, only one row and one column are activated, that is, only one DFF in the shift register is ON. To perform a parallel test, it demands that all rows and all columns could be intentionally selected to be ON. Hence, we can select all rows or all columns for parallel test. That is, for example, if a full row of cells are needed to be tested in parallel, the DFF for the tested row should be ON, and all the DFFs in column shift register should be ON too, as shown in Fig.9(a). It is similar to perform a parallel test on a full column, as shown in Fig.9(b).



(a) (b)

Fig.9 Selection of a full row and a full column

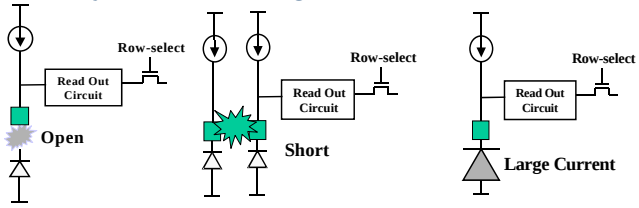
For each row, measure the total currents of one full row. If there is no faulty sensor cell in the row, the measured current will be M times of one cell's. And if there exist faulty cells, the measured current will be different from the expected value. For each column, measure the total currents of one full column. If there is no faulty sensor cell in the column, the measured current will be N times of one cell's. And if there exist faulty cells, the measured current will be different from the expected value.

From the measurement results of the rows and columns, we can crosscheck them to identify which cell is faulty. For example, if cell (i,j) is faulty, then the measurements of i^{th} column and j^{th} row will reflect this fault. Consequently, row by row and column by column, the number of test times is M+N.

3.3 Fault Detection of Crosscheck Test

Crosscheck test can efficiently perform parallel test on FPA. However, there does exist possibility of fault masking. In this subsection, a functional fault model is investigated, [20].

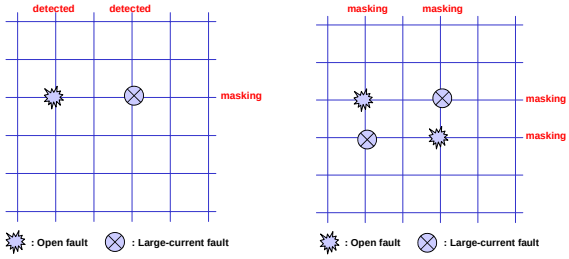
The testing of FPA is mainly relying on the current measurement, it is convenient to classify the possible faults, after binding of readout and sensor array chips, into three categories : open fault, short fault and large-current fault, as illustrated in Fig.10. The open fault, as shown in Fig.10(a), is caused by an unhealthy binding where the bumps between readout and sensor array chips are not connected. Therefore the bump pad of the readout is floating and no current appears. The short fault, as shown in Fig.10(b), is also caused by an unhealthy binding where the adjacent bumps are shorting together. Consequently, the shorted cells will receive extra currents from each other. The large-current fault, as shown in Fig.10(c), is caused by bad sensor cell that has a large leakage current. Since, the short fault can be regarded as a special type of large-current fault. For simplicity, we will only treat the open fault and large-current fault in subsequent analysis. If the cells are individually tested, the open fault and large-current fault can be obviously identified. Yet if they are tested by crosscheck test, there does exist possibility of fault masking.



(a) (b) (c)

Fig.10 The fault model

When only single-fault is considered, there does no fault masking exist. All single-fault can be evidently detected and located by crosscheck test. When double-fault is considered, if only one fault type is allowed, say open fault or large-current fault, then both faults of the double-fault can be detected and located. However, if both open and large-current fault types are allowed in a test, then both faults can be detected yet not located in some special cases. For example, as shown in Fig.11(a), an open fault and a double-current fault exist in a same row. In this case, when performing crosscheck test, testing row by row can not identify the faulty row due to current cancellation of the two faults. Nevertheless, testing column by column can identify the two faults. It is similar that when double-fault exists in a same column. If a double-fault does not exist in the same row or same column, both faults can be detected and located. When higher level of multiple-fault is considered, the possibility of fault masking will increase. And if the faulty cells canceling each other currents by row and by column simultaneously, then there will be no fault detected, as shown in Fig.11(b) for a quadruple-fault case.



(a) (b)

Fig.11 The fault masking

3.4 Verification

To verify the proposed crosscheck test scheme, a test chip of readout circuit for 4x4 array, as shown in Fig.12, is fabricated by using 0.5μm 2P2M CMOS process. A current source is built in with each cell of the array. The measurement results for the array are shown in Table 1-4. In the tables, the last column records the parallel test of each row, and the last row records the parallel test of each column. To inject an open fault, a laser cutter is employed to cut the connection wire between the current source and cell. To inject a short fault, the intentionally connect wire between two adjacent cells is left uncut, while the wire is cut for the good one case.

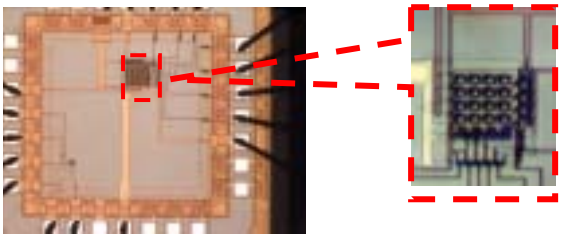


Fig.12 The photo of a 4x4 readout

Table 1 is the good one case. The crosscheck test of rows and columns are evident that there does not exist fault in the array. Table 2 is demonstrating an open fault on cell(3,2). The crosscheck test results of row-3 and column-2 smaller than others exhibit the open fault. Table 3 is the short fault case between cell(4,3) and cell(4,4). The column-3 and column-4 results are larger than normal one to show that a short fault exists between column 3 and 4. However, due to fault masking, the row-4 result can not distinguish from others. Table 4 is a double-fault case, where an open fault on cell(3,2) as well as a short fault between cell(2,1) and cell(3,1) are injected. A fault masking is occurred at the row-3 test.

4 Conclusion

The increase in array size and decrease in pixel size make the testing of infrared focal plane array being very difficult. A test socket chip for measuring the dark current of infrared detectors in a FPA is presented. To cancel the leakage current resulting from OFF-state switches, a novel calibration scheme adapted to this chip is also demonstrated. Therefore, the detector's dark current in an FPA can be accurately acquired. A crosscheck test scheme for FPA is also proposed to reduce the number of testing times, for an array size of M by N, from the order of M*N to M+N. A fault model for the crosscheck test scheme is also investigated in this paper.

The works presented in this paper are applied to IR FPAs. Our future works are modifying them for applications on other image sensor FPAs.

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Table 1: good

	1	2	3	4	row
1	0.95	0.94	0.92	0.94	3.78
2	0.96	0.95	0.93	0.95	3.83
3	0.94	0.94	0.95	0.94	3.81
4	0.97	0.96	0.95	0.96	3.87
col	3.88	3.84	3.80	3.81	

Table 2: open fault

	1	2	3	4	row
1	0.96	0.96	0.92	0.95	3.81
2	0.96	0.96	0.92	0.94	3.82
3	0.95	0	0.94	0.95	2.88
4	0.98	0.95	0.93	0.95	3.85
col	3.90	2.92	3.79	3.83	

Table 3: short fault

	1	2	3	4	row
1	0.96	0.94	0.93	0.95	3.81
2	0.96	0.94	0.94	0.95	3.83
3	0.95	0.94	0.95	0.95	3.82
4	0.96	0.95	0.96	0.96	3.89
col	3.90	3.82	5.01	5.02	

Table 4: open + short

	1	2	3	4	row
1	0.95	0.94	0.93	0.95	3.79
2	0.95	0.95	0.93	0.95	4.81
3	0.95	0	0.95	0.94	3.83
4	0.96	0.95	0.94	0.95	3.85
col	3.89	2.90	3.81	3.84	

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