Characteristics Optimization of Sub-10 nm Double Gate Transistors

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Abstract: - Double gate metal-oxide-semiconductor field effect transistors (DG MOSFETs) have recently been of great interest in modern nanoelectronics community. Device channel length L, thickness of silicon film (T_{si}), and oxide thickness (T_{ox}) play important roles in optimal characteristics design for DG MOSFETs. In this paper, we theoretically investigate the geometric effect on electrical characteristics for nanoscale (sub-10 nm) DG MOSFET devices by considering quantum correction transport model. We find that the thickness of silicon film should be simultaneously scaled down to a regime of the gate length. The thinner channel film greatly suppresses the short channel effect, but also suffers the on current issue. A compromise between the silicon film thickness and the gate channel length should be maintained at the same time so that an optimal device characteristic can be obtained. This investigation is useful for nanodevice and re-configurable design of system-on-a-chip (SOC) era.

Key-Words: DG MOSFET, geometric effect, Drain current, On/Off current, Channel length effect, Silicon film thickness effect, Modeling and Simulation

1 Introduction

Double gate silicon-on-insulator (SOI) devices are becoming more and more attractive candidates for sub-10 nm ultralarge scaled integrated (ULSI) circuits [1-16]. This is mainly caused from their inherent suppression of short-channel effects (SCEs), high transconductance, and ideal subthreshold swing (S-swing). It is well known that the double gate MOS structure has superior channel controllability in comparing with the traditional single gate MOS structures [3,8-16]. With the relatively better ability in channel control, the drain induced channel barrier height lowing (DIBL), threshold voltage roll off, and off state leakage should be greatly suppressed; however, the structure still has to be optimized to sustain the structural benefit.

Among the optimization parameters, the channel film thickness, channel doping concentration, and the gate oxide thickness are the most important factors. These first order effects on the device performance have to be carefully calculated to have a good result in, such as suppression of SCE. Though the double gate MOS structures have been widely studied, a theoretically analysis is not been drawn. Therefore, a large number of experimental conditions have to be designed and tested to ensure an optimal device characteristic, in particular for the reduction of SCE in ultrasamll nanodevices.

In this paper, we apply a TCAD tool to perform the device characteristics optimizations. The used TCAD tool was developed in our earlier work [4-7,15], which consists of drift-diffusion (DD), hydrodynamic (HD), and quantum correction models. In this computational model, the two-dimensional density gradient model is used in the DG MOSFET simulation. It has been shown already that the 1st quantum corrections, which satisfactorily describe quantum confinement effects, can be introduced into efficient technology computer-aided-design (TCAD) orientated drift-diffusion simulators using the density gradient approach. This quantum correction model is a modification of the conventional DD model. Base on the highly computationally efficient, a complete set of device is simulated, explored, and analyzed to have the best device structure. It concludes that the channel film thickness plays the most important factor in avoiding the SCE. That is, in suppressing the SCE in sub-10nm MOSFETs, the thickness of the silicon film must be scaling down simultaneously.

This paper is organized as follows. Section 2 states the computational models. Section 3 reports the results and discussion. Optimization is performed with respect to different device channel length L, thickness of silicon film (T_{si}), and oxide

thickness (T_{ox}). Section 4 draws the conclusions.

2 Computational Models

For ultrasmall nanodevices, in particular sub-20 nm devices a full quantum mechanical model is necessary due to the De Broglie thermal wavelength is a significant fraction of the channel length. We employ here only a quantum correction model. Therefore, to validate the model stated below, we have calibrated the simulated device characteristics with the measured devices. We also refer to Non-Equilibrium Green's Function simulations to calibrate the density gradient formalism in respect of both confinement and source-to-drain tunnelling using different effective masses in directions normal and parallel to the conducting channel.

In the computational model, we apply the two-dimensional (2D) density gradient (DG) model to the DG MOSFET simulation. The DG model (the so-called quantum drift-diffusion model) can be viewed as a modification of the conventional DD model. A "quantum potential" Λ is introduced into the classical equations of the electron density n and the current density J_n:

$$n = N_C \exp(\beta(E_{F,n} - E_C - \Lambda)) \text{ and} \quad (1)$$

$$J_n = -\mu kT\nabla n - \mu n\nabla(E_C + \Phi_m + \Lambda)). \quad (2)$$

The current density (2) can be re-written as:

$$J_n = -\mu n\nabla E_{E,n}. \quad (3)$$

In (1), $\beta = 1/k\mathrm{T}$, the electron quasi-Fermi energy $E_{F,n}$, the conduction band energy E_c and a mass driving term $\Phi_m = -kT\log N_c$ from density of state discontinuities. In the formulation presented here. Λ is the solution of the partial differential equation:

$$\Lambda = -\frac{\gamma\hbar^2}{12m}(\nabla^2 \log n + \frac{1}{2}(\nabla \log n)^2). \quad (4)$$

We can further reduce (4) as:

$$\Lambda = -\frac{\gamma\hbar^2\beta}{12m}(\nabla^2(\xi E_{F,n} - \overline{\Phi}) + \frac{\beta}{2}(\nabla(\xi E_{F,n} - \overline{\Phi})^2), \quad (5)$$

where ξ = 1, γ is a fitting parameter, and $\overline{\Phi} = E_C + \Phi_m + \Lambda$. Together with the Poisson and continuity equation, the above equations form a system to be solved self-consistently [1-2,6,8]. For holes, we have a similar governing equation. Fig. 1 shows the simulated device geometry.

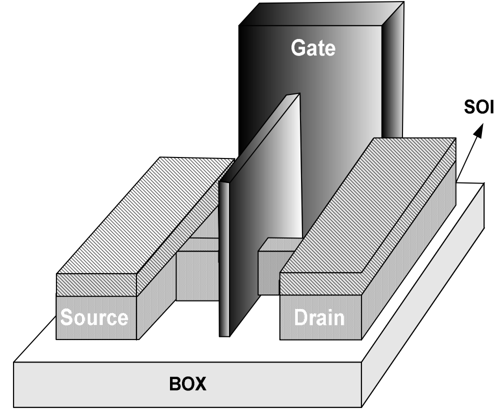

Fig. 1. A schematic diagram of the double gate MOSFET.

To solve the equations above, we use the adaptive computational technique. It is mainly based on the Gummel's decoupling scheme, finite volume method, unstructured mesh algorithm, and monotone iterative method. First of all, the coupled equations are decoupled with the Gummel's decoupling scheme. Each decoupled equation is discretized with the finite volume method on the unstructured mesh. The discretized equation forms a system of nonlinear algebraic equations. The nonlinear system is solved with the monotone iterative method. This advanced simulation methodology has been proposed by us for solving different transport models [5-6].

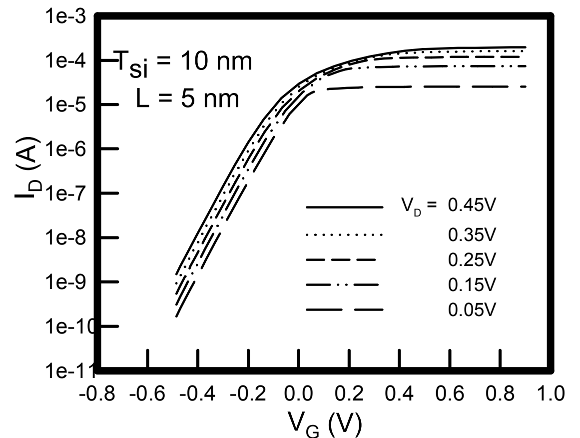

Fig. 2. I_D-V_G characteristics of the 5 nm device. T_{si} = 10 nm, L = 5 nm, and V_D varies from 0.05 to 0.45 V.

3 Results and discussion

Figs. 2-4 are I_D-V_G characteristics of DG MOSFET devices fabricated on 10 nm thicken silicon film. It

could be found that the shorter the channel length, the worse the SCE. That is, the threshold voltage is continuously decreasing with the increment of the drain-biased voltage. The threshold voltage lowering effect is caused from the drain induced barrier height lowering (DIBL). In our estimation, about 0.1 V of threshold voltage shift occurs in the 5 nm devices. We find about one-fourth voltage shift in the 10 nm devices. For all studies in this work, T_{ox} = 1 nm.

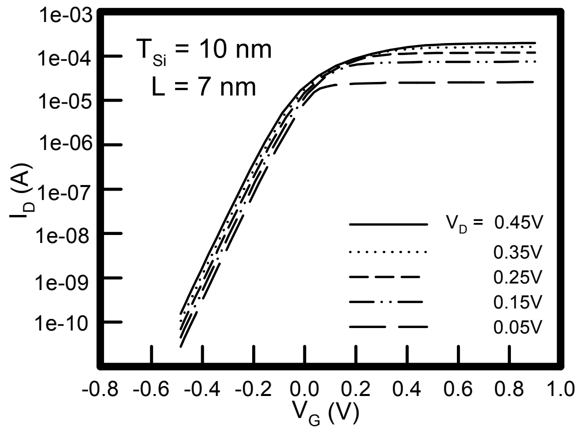

Fig. 3. I_D-V_G characteristics of the 7 nm device.

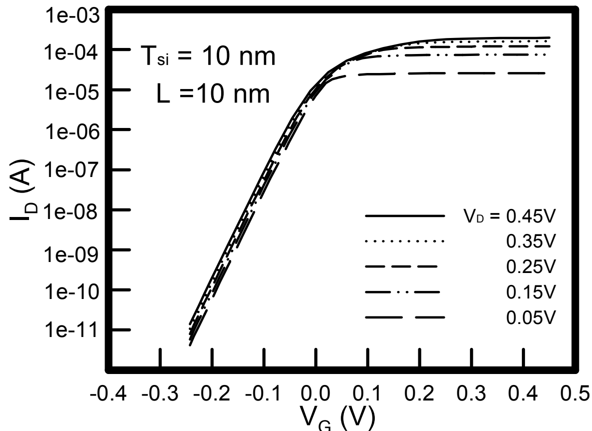

Fig. 4. I_D-V_G characteristics of the 10 nm device.

A more clearly results could be explored from the Fig. 5 that the 10 nm thicken silicon film devices with different length gate are compared. It is found that, the short gate devices have worse DIBL characteristics; moreover, the substhreshold swing is becoming larger in the shorter gate devices. Those characteristics become serious problems in device scaling engineering. Without considering of the SCE, no on current enhancement is observed from the simulation result. This should be caused from the fact that parasitic resistance is relatively high that limits the on current of those thin film devices.

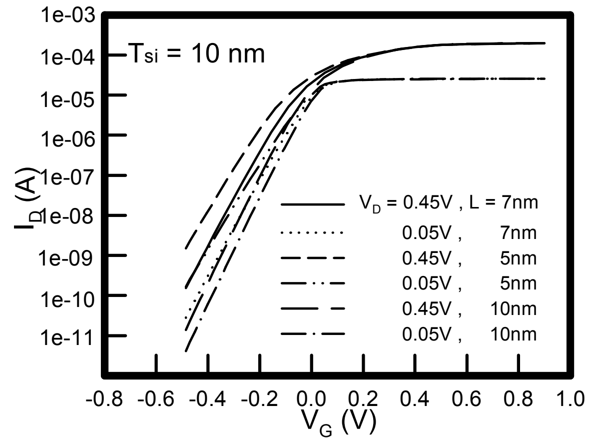

Fig. 5. Comparison of the I_D-V_G characteristics for the different gate lengths DG MOSFET devices. The thickness of silicon film is 10 nm.

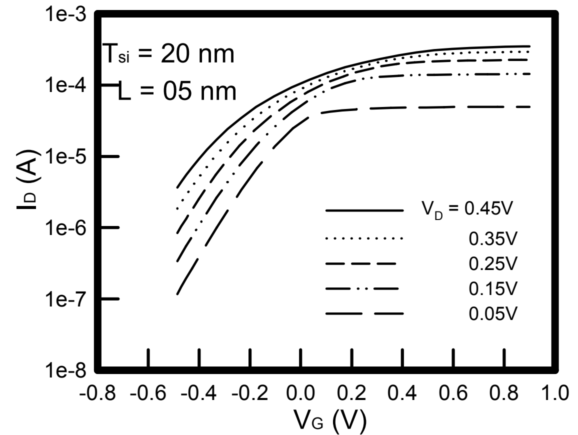

Fig. 6. I_D-V_G characteristics of the 5 nm device. T_{si} = 20 nm, L = 5 nm, and V_D varies from 0.05 to 0.45 V.

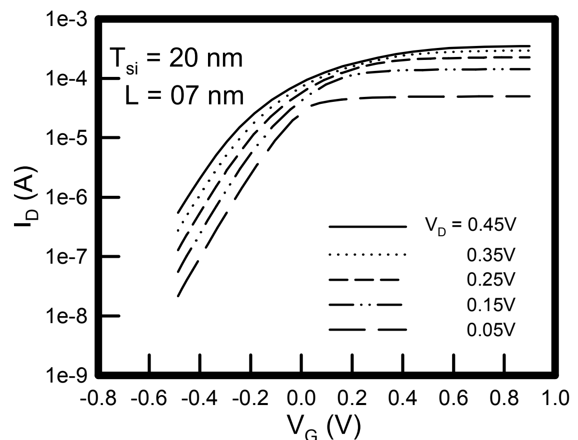

Fig. 7. I_D-V_G characteristics of the 7 nm device.

We note that due to the fully depleted channel effect, the threshold voltage of the thin body devices are relatively low and hard to be adjusted by

increasing the channel doping. Consequently, it is becoming a more important course in fine-tuning the metal-semiconductor work function.

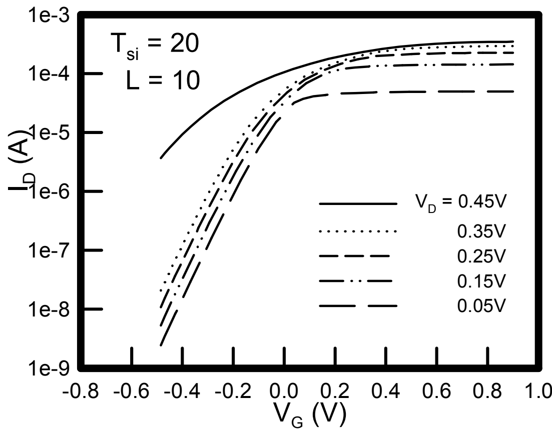

Fig. 8. I_D-V_G characteristics of the 10 nm device.

Though the I_D-V_G transfer curves of the 10 nm thicken silicon channel film device shown a slightly DIBL effects. The 20 nm and 30 nm thicken devices have much larger DIBL effects as shown in Figs. 6-11. Moreover, the off state current of the thicker channel devices are much higher than that of the thinner channel one. Those drawbacks are mainly caused from the fact that the thicker the channel films the weaker the controllability of gate electrodes. Owing to the inefficient gate controllability, the thicker channel devices have a lower channel barrier height, obtain a higher leakage current, and get a worse result for drain induced barrier height lowering (DIBL) effects.

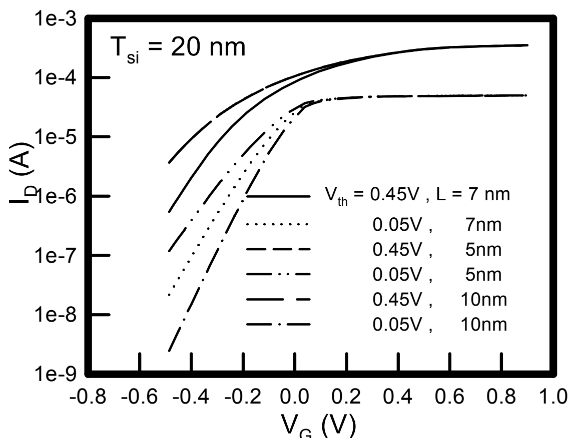

Fig. 9. I_D-V_G characteristics with respect to V_{th}, L, and the thickness of silicon film is 20 nm.

Other than the off state current and threshold voltage lowering, the on state current should be another one important factor for novel devices operations. That is, the greater the on state current the higher the operation frequency. Figs. 12-14 present the on state current of the different thicken channel film devices. It has to address that the thicker the channel films the higher the on state current. Owing to a much worse performance in threshold voltage and off state current, the benefit of the on state current is relatively minor in optimization of the double gates devices.

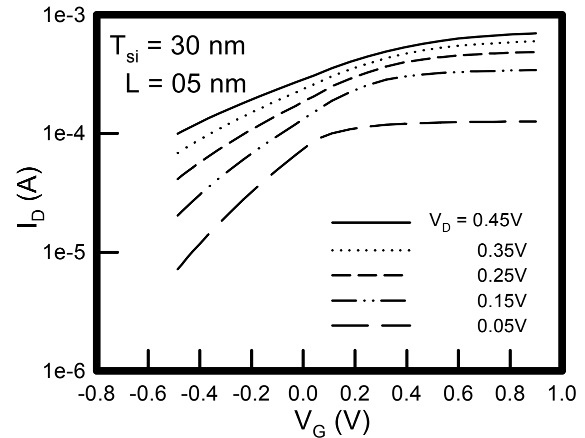

Fig. 10. I_D-V_G characteristics of the 5 nm lengthen double gate device, where T_{si} = 30 nm.

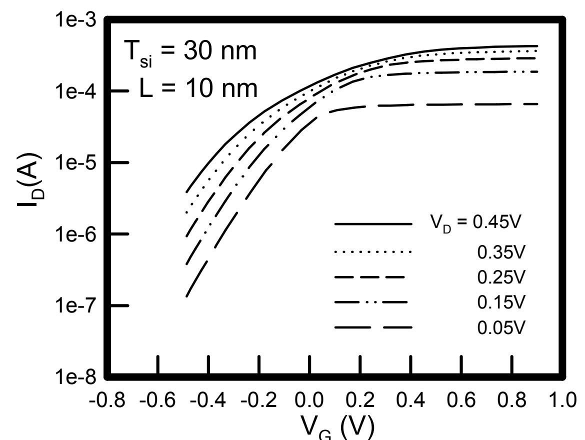

Fig. 11. I_D-V_G characteristics of the 10 nm device. The thickness of silicon film is 30 nm.

The DIBL effects are also presented in the Fig. 15 that the thicker channel film devices have a higher DIBL effect. Therefore, in reducing the effect, the thickness of the channel films should be carefully optimized. That is, for a reasonable on state current, the channel film thickness should be keep as thin as possible. We conclude that the film thickness of the double gate devices will strongly affect device characteristics; especially for the considerations of threshold voltage roll off, DIBL,

and off state current. Those effects are strongly determined from the controllability of the gate electrodes. In lowering those drawbacks, the film thickness should be kept thin enough.

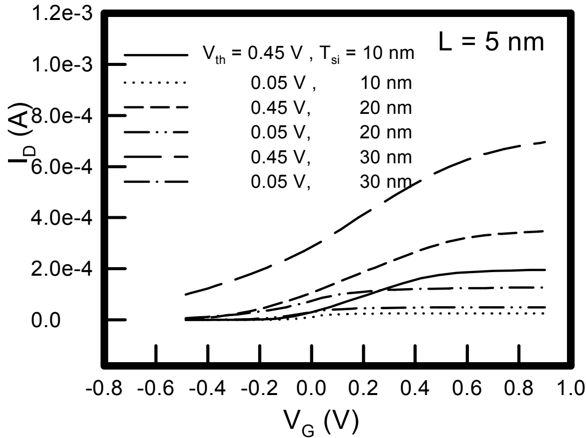

Fig. 12. I_D-V_G characteristics with respect to V_{th} and T_{si}, where the channel length L = 5 nm.

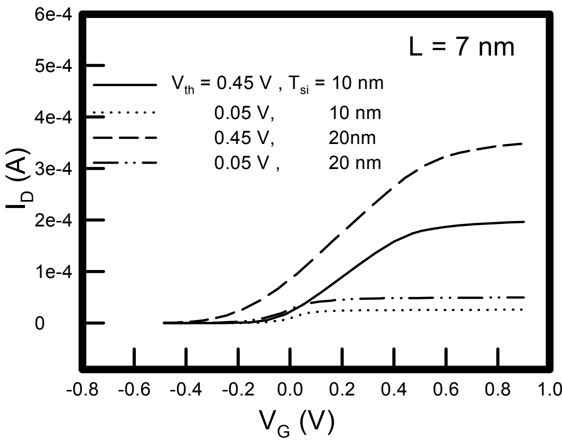

Fig. 13. I_D-V_G characteristics with respect to V_{th} and T_{si}. The gate length is 7 nm.

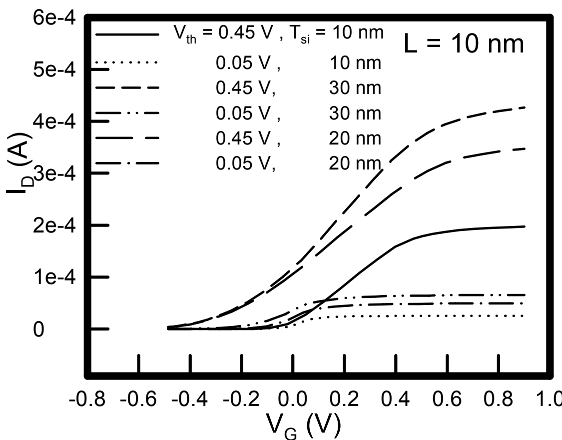

Fig. 14. I_D-V_G characteristics with respect to V_{th}, T_{si}, and the channel length L = 10 nm.

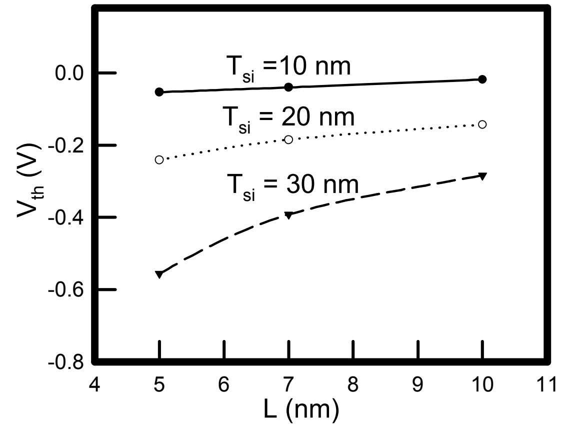

Fig. 15. The channel film thickness effect on the V_{th} roll off. Plot of V_{th} versus L. T_{si} varies from 10 nm to 30 nm.

The threshold voltage roll off effect is shown in the Fig. 16, it is found that the devices with the thicker channel films will suffer a worse roll off in threshold voltage. Additionally, a thinner channel film will result in a higher threshold voltage. Those good characteristics will improve the scalability of nanodevices.

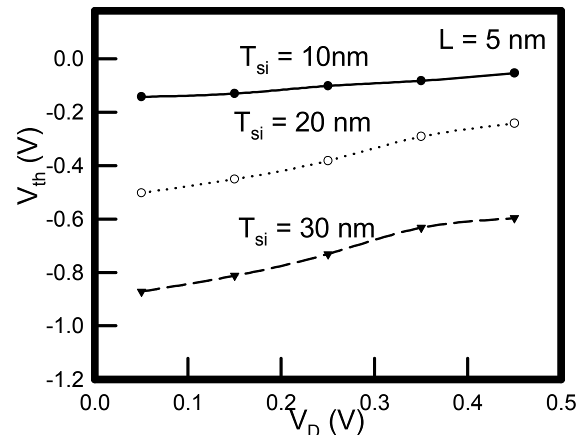

Fig. 16. The V_{th} versus the drain bias with respect to different T_{si}, where L = 5 nm and T_{si} varies from 10 nm to 30 nm. A comparison of the silicon film thickness related DIBL effects.

4 Conclusions

In this paper, we have demonstrated that the optimization of the double gate MOSFET devices could be achieved by our developed highly efficient device solver. It has been found that the thickness of the silicon film should be simultaneously scaled down with the gate length. The thinner channel film has greatly suppressed the short channel effect, but also suffered the on

current issue. A compromise between the silicon film thickness and the gate channel length should be maintained at the same time so that an optimal device characteristic can be obtained. This investigation is useful for the development of nanodevice technology and SOC design.

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