Numerical Simulation of Nanoscale Double-Gate and Gate-All-Around Metal-Oxide-Semiconductor Devices

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Abstract: - A numerical model for physical characteristics simulation of nanoscale double-gate and gate-all-around Metal-Oxide-Semiconductor (MOS) under strong inversion is presented. Together with an effective potential quantum correction, one-dimensional (1D) Poisson equation with symmetric boundary conditions is solved in both Cartesian and cylindrical coordinates for single-gate, double-gate, and gate-all-around MOS structures. Comparison on these three different MOS structures is explored in terms of the total inversion layer charge and the average inversion charge depth. By considering the same surface potential, it is found that the concentration of the induced inversion charge for the gate-all-around MOS is significantly higher than the others. Therefore, this implies the gate-all-around MOS structure has better gate controllability and higher current density.

Key-Words: - single-gate, double-gate, gate-all-around, nanoscale MOS, quantum correction, effective potential, Poisson equation, Cartesian and cylindrical coordinates, the total inversion layer charge, the average inversion charge depth.

1 Introduction

Study of advanced nanoscience and nanotechnology has recently been of great interest, in particular nanoscale semiconductor structures and devices [1-3]. The channel length of metal-oxide semiconductor field effect transistors (MOSFETs) is currently in the nanoscale regime (e.g. 10-90 nm). Two promising structures such as the symmetric double-gate (DG) and gate-all-around (GAA) MOS have attracted increased research interests [13-17]. They introduce the concept of volume inversion: the inversion charge spreads throughout the whole ultrathin silicon (Si) body, which improves the device characteristics (e.g., higher current due to the substrate mobility). Strong inversion plays an important role in nanoscale MOS device physics as it provides the information of the swept charge as well as the saturation current. Systematical examination on intrinsic physical properties is necessary for the development of nanoscale DG and GAA MOS structures.

In this paper we numerically solve the classical 1D Poisson equation together with the effective potential (EP) quantum correction model in the Cartesian and cylindrical coordinates for nanoscale DG and GAA MOS structures [7-12]. Firstly, without considering the quantum mechanical effect, the classical potential and electron density are simulated and compared among single gate (SG), DG, and GAA MOS structures. Under the same bias condition, the GAA MOS has higher classical electron density than the SG and DG's. To accurately account the quantum mechanical effect [4-7, 18-19] for the nanoscale MOS structures, we further solve the classical 1D Poisson equation with the EP model self - consistently. Simulation of inversion-layer charge density with various Si film thickness, oxide thickness, and gate bias voltage is performed on DG and GAA MOS structures. For the same surface potential, it is found that the concentration of the induced inversion charge for the GAA MOS is significantly higher than the others. The GAA MOS has larger average inversion charge depth than that of DG MOS.

This paper is organized as follow. Mathematical model for the SG, DG, and GAA MOS structures are described in Section 2. Simulation procedure for the quantum correction model is discussion in the section. Section 3 presents the simulation results and discussion. Finally, Section 4 draws conclusions and suggests the future work.

2 Computational Model

Simply considering the Boltzmann statistics for the carrier concentrations, a general model to describe the electrostatic potential distribution for semiconductor MOS structures is known as the Poisson equation [5, 7]:

$$\nabla^2 \varphi = -\frac{q}{\varepsilon_s}(n_i e^{\frac{\varphi_p - \varphi}{V_T}} - n_i e^{\frac{\varphi - \varphi_n}{V_T}} - N_a + N_d) \quad (1)$$

In 1D situation, (1) becomes:

$$\frac{d^2\varphi}{dr^2} + \frac{m}{r}\frac{d\varphi}{dr} = -\frac{q}{\varepsilon_s}(n_i e^{\frac{\varphi_p - \varphi}{V_T}} - n_i e^{\frac{\varphi - \varphi_n}{V_T}} - N_a + N_d) \quad (2)$$

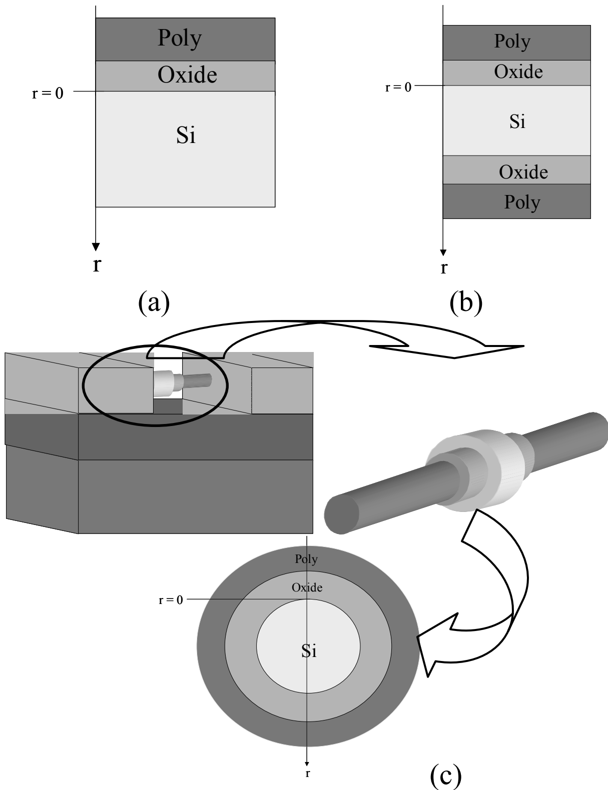


Fig. 1. Illustration of the structures of (a) SG (b) DG and (c) GAA MOS.

For the DG MOS structure in the Cartesian coordinate, m is set to be zero in (2). For the GAA MOS structure in the cylindrical coordinate: $m = 1$. The schematic description of the device structure is shown in Fig. 1. In (2), N_a is the doping concentration of the Si body and N_d is the doping concentration of the poly-silicon. The symmetric boundary conditions for both structures are:

$$\frac{d\varphi}{dr}(r = r_0) = 0 \quad (3)$$

$$\varphi(r = 0) = \varphi_s \quad (4)$$

Here $r = r_0$ is at the center of the Si body and $r = 0$ is on the surface, φ_s is the surface potential.

Currently the thickness of gate oxide is scaling down to the 0.8-3 nm and the DG and GAA Si film body is within 50 nm; therefore it is necessary to include quantum mechanical effects when modeling their physical transport phenomena. Various theoretical approaches have been considered to study the quantum confinement effects, such as full quantum mechanical model (e.g. nonequilibrium Green's function) and quantum corrections to the Boltzmann, drift-diffusion and hydrodynamic transport models. A set of Schrödinger-Poisson equations has been applied to study the quantum effect in the inversion layers, but it is a time-consuming task in the application to realistic device simulations. We apply the EP model to the simulation of inversion-layer charge density. This model is based on the following integral transformation from the classical potential $V(x)$ to EP $V_{eff}(x)$ as [7-12]

$$V_{eff} = \frac{1}{\sqrt{2\pi}\alpha}\int_{-\infty}^{\infty} V(x+\xi)\exp(-\frac{\xi^2}{2\alpha^2})d\xi \quad (5)$$

where $\alpha = \hbar / \sqrt{8m^* k_B T}$.

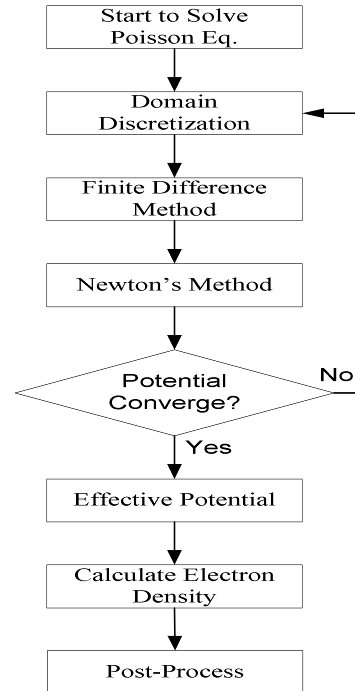


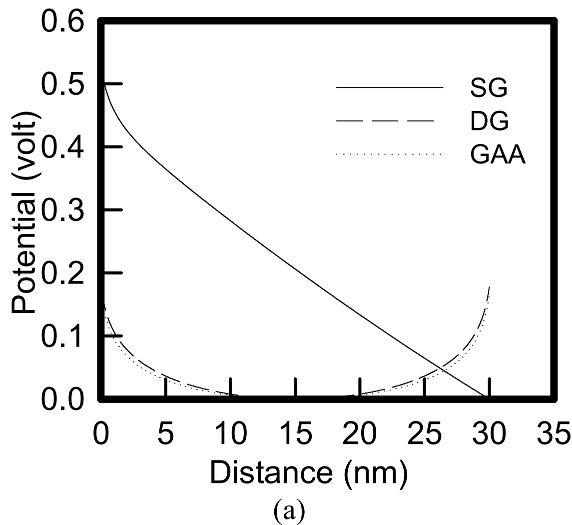
Fig. 2. Solution procedure for the quantum correction model.

The classical potential initially calculated from the Poisson equation. After the quantum correction potential is obtained from the EP equation, the electron concentration $n(x)$ is calculated using the Boltzmann statistics. We then solve the Poisson equation again until a consistency is reached. As shown in Fig. 2, the classical Poisson equation is solved with the finite difference and the Newton's method iteratively. Once the computed classical potential is convergent, we calculate the quantum correction potential with (5). Therefore, the electron density is solved with the Boltzmann statistics. For device with heavily doping concentration, we can replace the Boltzmann statistics with the Fermi-Dirac statistics in Eq. (1)

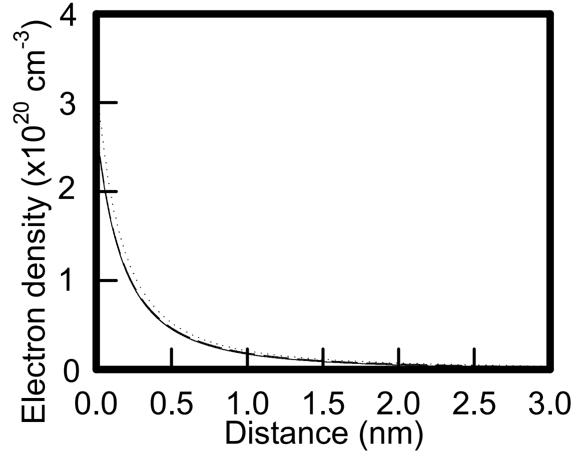
3 Results and Discussion

The three structures, SG, DG, and GAA MOS system are solved with the 1D Poisson equation and EP model. The effective mass m^* shown in the EP model is as an adjusting parameter. For the simplicity, m is chosen as 1.0 in our simulation. The potential and inversion charge concentration of the classical model, both as a function of the distance r from the oxide and substrate interface, are calculated and Shown in Figs. 3(a) and 3(b). The DG and GAA structures are with a 30-nm-thick body (e.g., r_0 = 15 nm, $N_a = 10^{17}$ cm^{-3}, and V_g = 1.0 V), and SG structure with the same condition except the 100-nm-thick body.

As shown in Fig. 3(a), the solid line is the classical potential of SG MOS, the dash and dot lines are for DG and GAA MOS, respectively. The GAA MOS has higher electron density, shown in Fig. 3(b), in comparing with the others. Due to the totally surrounding geometry on the gate, it is no surprise that the GAA MOS structure has better charge controllability than those others.



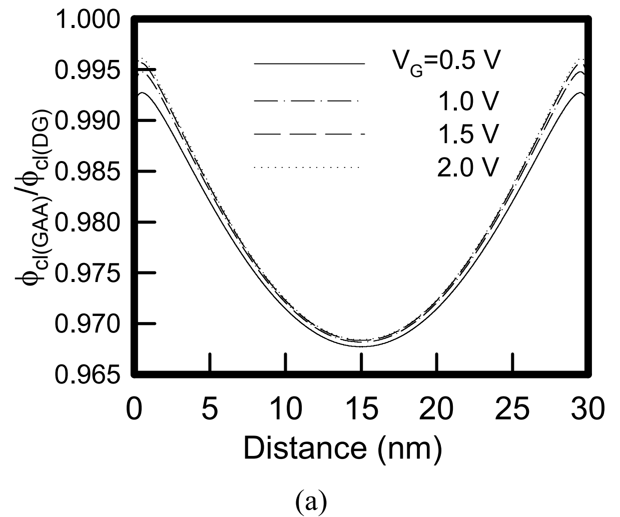
(a)



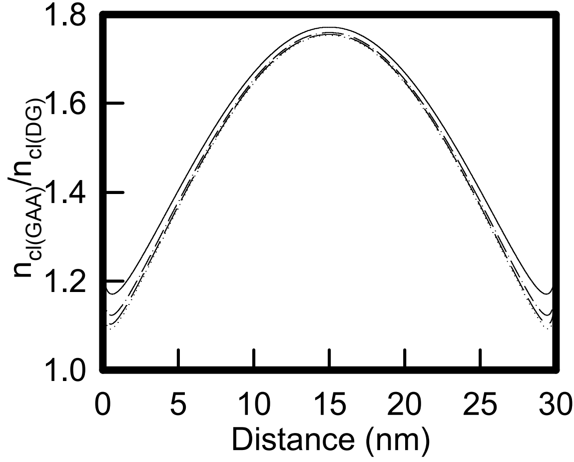
(b)

Fig. 3. Computed classical (a) potential and (b) electron density for the three structures.

Fig. 4 shows the ratio of the potential and the carrier concentration for the GAA and DG structures, respectively. They are computed by only considering the classical Poisson equation. In Fig. 4(a), we see that the classical potential of the GAA MOS is always smaller than that of DG MOS in the silicon film region. From the calculated results, it is found when the two structures have the same current, the GAA MOS dissipate lower power than DG MOS. In Fig. 4(b), the ratio of the electron concentration is always bigger than one. It means the electron concentration of the GAA MOS is larger than that of DG MOS (~ 1.8 times). According to the results above, we may have a better controllability for the charge of GAA MOS structure. In other words, in comparing with the DG MOs structures, a lower gate voltage is enough to produce the same charge for GAA MOS structures under the inversion layer.



(a)



(b)

Fig. 4. (a) Potential ratio of the GAA vs. DG MOS and (b) ratio of the electron concentration of the GAA vs. DG MOS, where the symbols are the same as fig. 4(a).

To investigate the quantum mechanical effect on the devices, we add the EP model to the Poisson equation in our following studies. Fig. 5 shows the electron density calculated by the EP model which is different from the classical results shown in Fig. 3(b). While keeping the same gate voltage, the GAA MOS has a higher peak of the electron density than the others. It is found that the peak density of GAA MOS is about 1.5 times larger than that of SG MOS. The peak location for all cases shifts away from the interface of Si/SiO_2 about 1 nm. Fig. 6 shows the examination on the ratio of the electron concentration for GAA and DG MOS structures. The ratio calculated with the EP model is similar to Fig. 4(b).

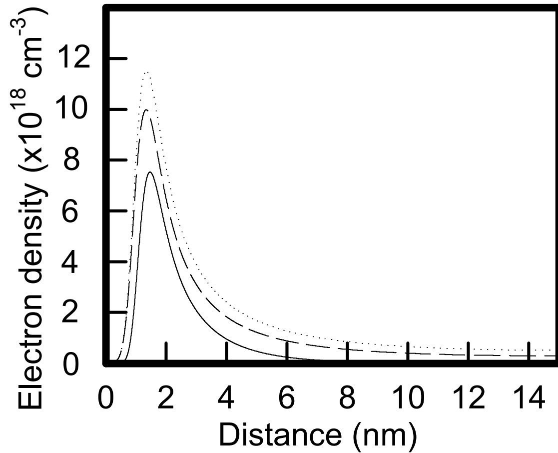


Fig. 5. Electron density with the EP model. The solid, dash, and dot lines are for SG, DG and GAA MOS, respectively.

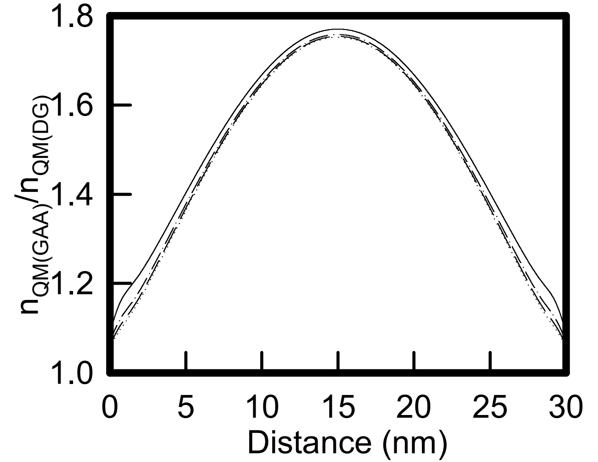


Fig. 6. Ratio of the electron concentration of the GAA vs. DG MOS with the EP model, where the symbols are the same as fig. 4.

Fig. 7 shows the total inversion layer charge <*Q*> with respect to the applied gate voltage. <*Q*> is the integration of the inversion layer charges defined as

$$< Q >= \int_0 n(r)dr, \qquad (6)$$

where $n(r)$ is the electron density. As the gate voltages increase, the total inversion layer charges increase. We see that the GAA MOS (dot line) has the largest inversion layer charges under the same gate voltage. It also demonstrates larger variation of the inversion layer charges when V_G varies from 0.5 to 2.0 V.

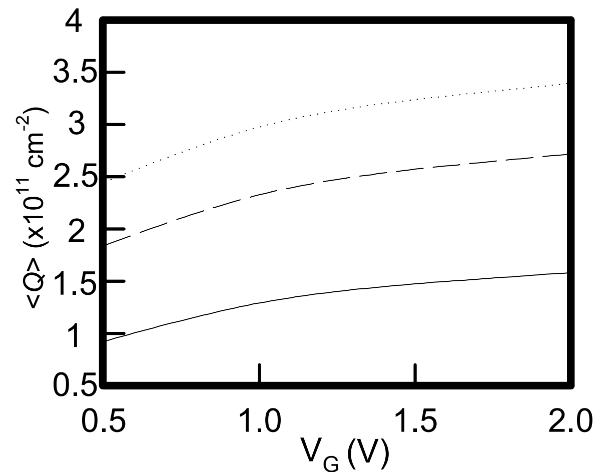


Fig. 7. The total inversion layer charge <*Q*> with respect to the applied gate voltage. The solid, dash, and dot lines are for SG, DG and GAA MOS, respectively.

Fig. 8 shows the average inversion charge depth (i.e., average distance) versus various gate voltages for the three MOS structures. The average inversion charge depth <*X*> is defined as

$$< X >= (\int_0 rn(r)dr)/(\int_0 n(r)dr) \cdot \quad (7)$$

Due to the surrounding topology for the GAA MOS structure, it is obvious that the GAA MOS has larger average inversion charge depth than those of DG and SG MOS. As the average inversion charge depth increases, the friction between the free electron and oxide layer (SiO_2/Si) interface decreases. Therefore, the channel mobility increases.

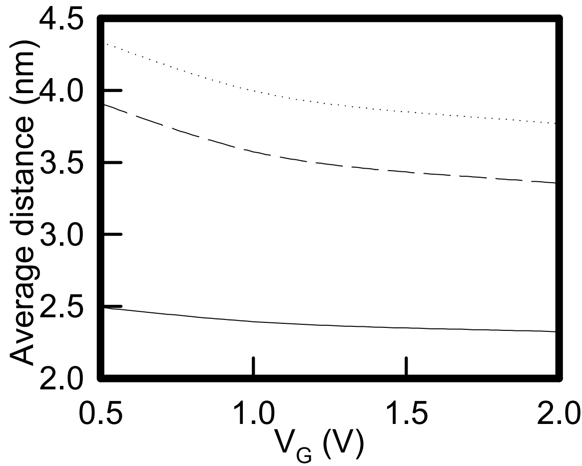


Fig. 8. The average inversion charge depth versus the gate bias for the three MOS structures. The symbols are the same as Fig. 7.

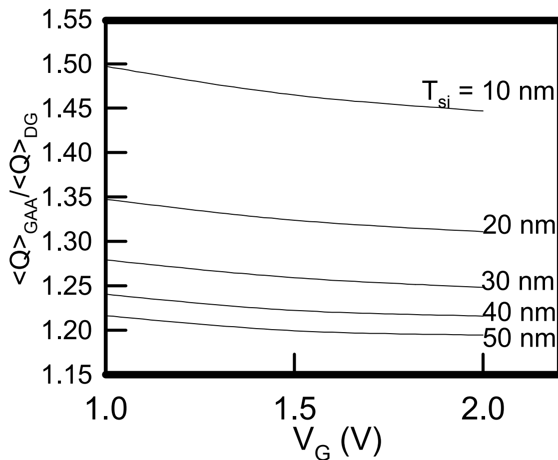


Fig. 9. Ratio of the inversion layer charges.

Fig. 9 shows the ratio of $<Q>_{GAA}$ to $<Q>_{DG}$ with respect to the applied voltages for different thickness of Si film. <*Q*> is the integration of the inversion layer charges as defined above. Notice the upper limitation in the integral of (6) is 30 nm (Because the thickness of Si body is 30 nm). We find that the ratio of $<Q>_{GAA}$ to $<Q>_{DG}$ is slightly decreases when the V_G increases. It also shows the ratio of the inversion layer charges for EP model increases with the film thickness decrease. Due to the mention above, we find the quantum effect near to the SiO_2/Si interface of the MOS is more noticeable when the film thickness is decreased.

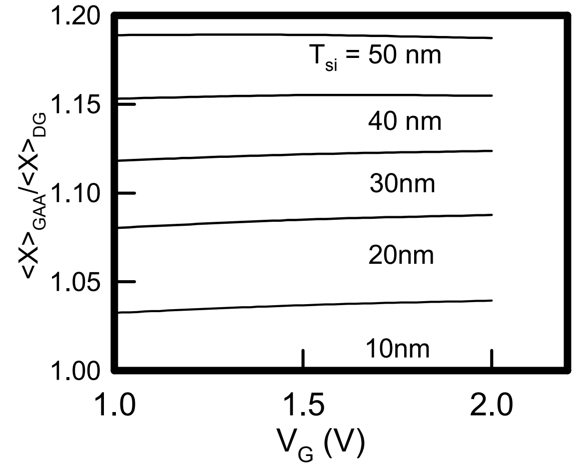


Fig. 10. Ratio of the average inversion charge depth.

Fig. 10 shows the ratio of $<X>_{GAA}$ to $<X>_{DG}$ with respect to the applied gate voltages for different thickness of Si film. The average inversion charge depth <*X*> is defined above. We find that the ratio of $<X>_{GAA}$ to $<X>_{DG}$ increases when the T_{si} increases. The ratio is independent of V_G. With the film thickness decrease, the quantum effect near to the Si/SiO_2 interface of the MOS is more noticeable. The peak of the electron density moves to the structure center. The peak in the left side is more closed to the right side one. However, the electron charges in the both side are the same polarization. They are both negative charge. Due to the physical formula that the two same polarization charges repulsive, the peak in the both side move slowly when the film thickness decrease. The ratio of the average inversion charge depth for EP mode is smaller when the film thickness is decrease.

5 Conclusions

A numerical model for physical characteristics simulation of ultrasmall nanoscale double-gate and gate-all-around MOS under strong inversion has been presented. Together with the effective potential

quantum correction formulation, the 1D Poisson equation with symmetric boundary conditions has been solved in both Cartesian and cylindrical coordinates for single-gate, double-gate, and gate-all-around MOS structures. Comparison on these three different MOS structures has been explored in terms of the total inversion layer charge and the average inversion charge depth. By considering the same surface potential, it has been found that the concentration of the induced inversion charge for the gate-all-around MOS is significantly higher than the others. Therefore, this implies gate-all-around MOS structure has better gate controllability and higher current density.

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