

ESD Protection Scheme for I/O Interface of CMOS IC Operating in the Power-Down Mode on System Board

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Abstract: - Design on ESD protection circuit for IC with power-down-mode operation is proposed. By adding a VDD ESD bus line and the diodes into the ESD protection scheme, the leakage current from the I/O pin to VDD power line can be blocked to avoid malfunction under the power-down-mode operating condition. Under normal circuit operating condition, the proposed ESD protection schemes have no leakage path to interfere with the normal circuit functions. Power-rail ESD clamp circuits between VDD ESD bus and VSS power line, or between VDD power line and VSS power line, are used to achieve the whole-chip ESD protection design. From the experimental results, the human-body-model ESD level of the proposed ESD protection schemes can be greater than 7.5kV in a 0.35- μ m CMOS process.

Key- Words: - Electrostatic discharge (ESD), ESD protection circuit, Power-down-mode, ESD bus

1 Introduction

For power consumption consideration, IC with power-down-mode operation becomes more and more attractive especially in the SOC (System on a Chip) design for the portable and mobile devices. However, if the power-down-mode operation of the IC is needed, the extraordinary design on the I/O circuits or internal circuits is required [1], [2]. An example of two chips connected in a system is shown in Fig. 1, where the output pad of the chip₁ is connected to the input pad of the chip₂. When the chip₂ goes into the power-down-mode operation, two situations are explained as follows. First, if VDD2 power line is grounded, a large leakage current may be induced from the input pad to the VDD2 power line through the parasitic diode of pMOS connected between the input pad and VDD2 power line, when the output voltage level of the chip₁ is high. Second, if the VDD2 power line is floating, the internal circuits of the chip₂ may be triggered to cause malfunction by charging the VDD2 power line through the parasitic diode of pMOS connected between the input pad and VDD2 power line, when the output voltage level of the chip₁ is high. Therefore, the parasitic diode of pMOS connected between the input pad and VDD2 power line need to be removed to avoid the occurrence of large leakage current or function misoperation, when the chip₂ goes into the power-down-mode operation in this example.

ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode),

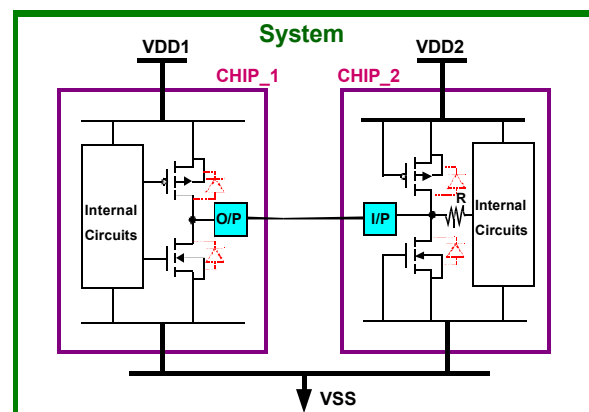


Fig. 1 An example to show the power-down-mode operation issue on a system with two chips, which are biased with separated VDD1 and VDD2 power supplies.

negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stress conditions [3]. To avoid unexpected ESD damage in the internal circuits of CMOS ICs [4]-[5], the power-rail ESD clamp circuit must be placed between the VDD and VSS power lines [6]. For the traditional ESD protection scheme shown in Fig. 2, the ESD current at the I/O pad under the positive-to-VSS ESD stress condition can be discharged through the parasitic diode of pMOS and the VDD-to-VSS ESD clamp circuit to ground. In addition, the ESD current at the I/O pad under the positive-to-VDD ESD stress condition can be discharged through the parasitic diode of pMOS to VDD power line. Therefore, the traditional I/O circuits cooperating with the VDD-to-VSS ESD

clamp circuit can achieve a much higher ESD level [6]. But, due to the limitation of placing a diode from the I/O pad to VDD in the power-down-mode operation, the positive-to-VSS ESD voltage zapping on the I/O pad cannot be diverted from the pad to VDD power line, and cannot be discharged through the additional power-rail (VDD-to-VSS) ESD clamp circuit. Such positive-to-VSS ESD current on the I/O pad is discharged only through the gate-grounded nMOS (GGNMOS) between the I/O pad and VSS power line by snapback breakdown. However, because the junction breakdown voltage is close to the oxide breakdown voltage as the device is shrunk, the GGNMOS could not provide efficient ESD protection to the internal circuits in sub-quarter-micron CMOS technology [7], [8]. Especially, the non-uniform turn-on issue often causes the GGNMOS to have a low ESD level [9]. In addition, the positive-to-VDD ESD voltage zapping on the I/O pad cannot be diverted from the I/O pad to VDD power line without causing the pMOS breakdown. Such positive-to-VDD ESD current on the I/O pad will be discharged through the GGNMOS by snapback breakdown to the VSS line, and then through the parasitic diode of VDD-to-VSS ESD clamp circuits to the grounded VDD power line. Therefore, the absence of the diode between the I/O pad and VDD power line for power-down-mode operation may seriously degrade ESD performance of the I/O pad under the positive-to-VSS and positive-to-VDD ESD stress conditions.

One way to realize the ESD protection circuits for IC with power-down-mode operation is to replace the diode by the GGNMOS between the I/O pad and VDD power line [10]. But, the GGNMOS in snapback breakdown to discharge ESD current often suffers the non-uniform turn-on issue to result in a low ESD level, even if the nMOS is drawn with a large device dimension. Another way is to focus on improving the ESD robustness of the ESD protection circuit between the I/O pad and VSS power line [11]. If no ESD protection device or circuit are connected between the I/O pad and VDD power line, the ESD current is discharged only through the ESD protection circuit from I/O pad to VSS when the I/O pad is under positive-to-VSS or positive-to-VDD ESD stress. To achieve a high enough ESD specification, the ESD protection circuit will become complicated and the area consumption is increased.

In this paper, two new ESD protection schemes for IC with power-down-mode operation are proposed. The new ESD protection schemes for IC with power-down-mode operation have been successfully verified in a 0.35- μm CMOS process with a very high ESD level.

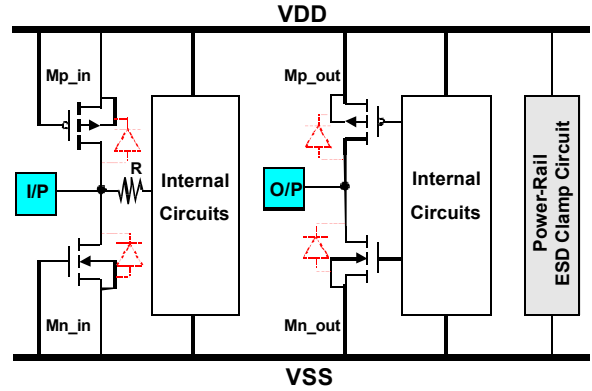


Fig. 2 Traditional ESD protection scheme in a CMOS IC with pMOS and nMOS as ESD protection devices for input and output pads.

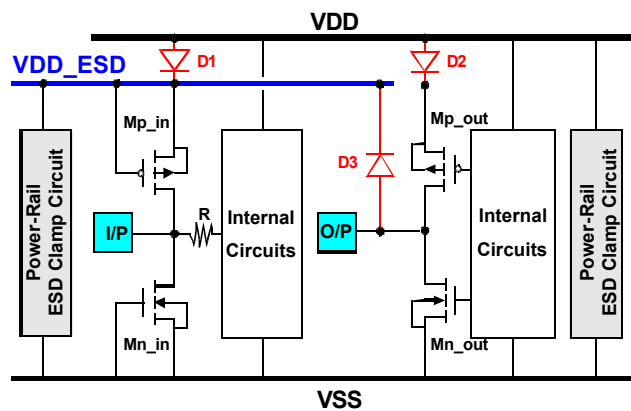


Fig. 3 The new proposed ESD protection scheme I for the IC with power-down-mode operation.

2 New ESD Protection Schemes

2.1 ESD Protection Scheme I

The proposed ESD protection scheme I for the IC with power-down-mode operation is shown in Fig. 3 with the additional ESD bus line, which is realized by a wide metal line in CMOS IC. The diode D1 is connected between the VDD power line and VDD ESD bus line to block the leakage current path from the input pad to VDD, when the power of VDD is off. The diode D2 is connected between the VDD power line and the source of Mp_out to block the leakage current path from the output pad to VDD, when the power of VDD is off. The VDD ESD bus line is not connected to the source of Mp_out in this scheme I, because Mp_out may be turned on and induces leakage current when the power of VDD is off. The diode D3 is connected between the output pad and VDD ESD bus line for ESD protection purpose. The power-rail ESD clamp circuit is connected between the VDD power line and the VSS power line. A second power-rail ESD clamp circuit is connected between the VDD ESD bus line and the VSS power line. The ESD current at the input (output) pad under

the positive-to-VSS ESD stress condition can be discharged through the parasitic diode of Mp_in (the diode D3) and the ESD clamp circuit between the VDD ESD bus line and the VSS power line to ground. The ESD current at the input (output) pad under the positive-to-VDD ESD stress condition can be discharged through the parasitic diode of Mp_in (the diode D3) to VDD ESD bus line, the ESD clamp circuit to VSS power line, and then the parasitic diode of ESD clamp circuit to the grounded VDD power line.

2.2 ESD Protection Scheme II

The proposed ESD protection scheme II for the IC with power-down-mode operation is shown in Fig. 4. The design concept is similar to that of the ESD protection scheme I. The diode D1 is connected between the VDD power line and VDD ESD bus line to block the leakage current path from the input or output pad to VDD, when the power of VDD is off. The gate of Mp1 is connected to the VDD power line. Therefore, Mp1 is turned off under the normal circuit operating condition. Under power-down-mode operating condition, the Mp1 is turned on to keep the Mp_out off. In addition, the power line of the pre-driver internal circuits which controlled the gate of Mp_out is connected to the VDD ESD bus line to avoid the leakage current from the pre-driver internal circuits to VDD power line, when the power of VDD is off. The ESD current at the input (output) pad under the positive-to-VSS ESD stress condition can be discharged through the parasitic diode of Mp_in (Mp_out) and the ESD clamp circuit between the VDD ESD bus line and the VSS power line to ground. The ESD current at the input (output) pad under the positive-to-VDD ESD stress condition can be discharged through the parasitic diode of Mp_in (Mp_out) to VDD ESD bus line, the ESD clamp circuit to VSS power line, and then the parasitic diode of ESD clamp circuit to VDD power line.

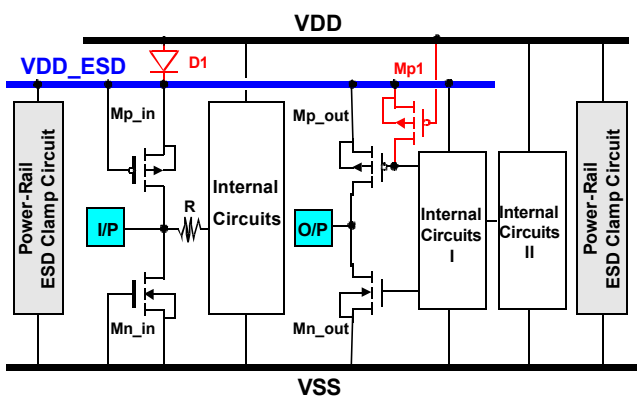


Fig. 4 The new proposed ESD protection scheme II for the IC with power-down-mode operation.

Therefore, with the new proposed ESD protection schemes, the leakage current or function misoperation issues in the IC operating under power-down-mode condition can be avoided. The internal circuits of CMOS IC can be fully protected against ESD damage by the new proposed ESD protection schemes.

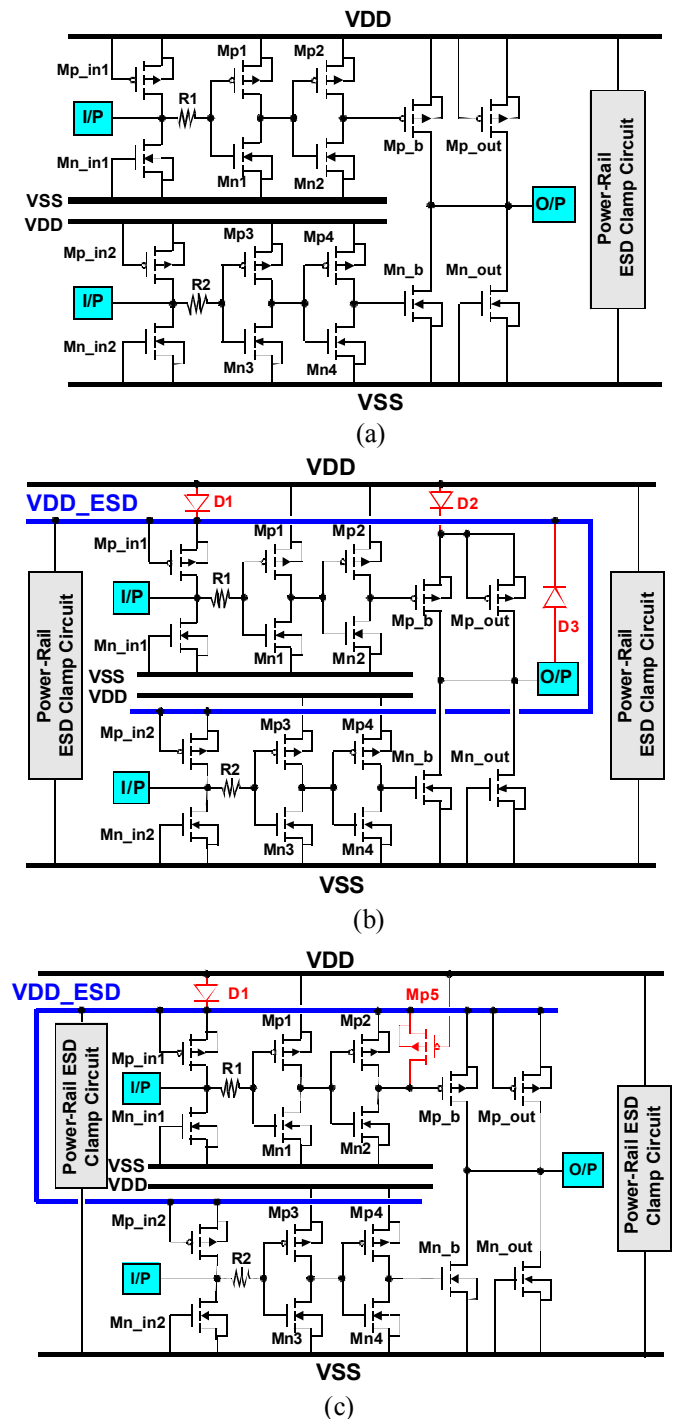


Fig. 5 The test chips with (a) the traditional ESD protection scheme, (b) the proposed ESD protection scheme I, and (c) the proposed ESD protection scheme II, realized in a 0.35- μ m CMOS process.

3 Experimental Results

The test chips with the proposed ESD protection schemes for IC with power-down-mode operation and the traditional ESD protection scheme had been fabricated in a 0.35- μm CMOS process, as those shown in Figs. 5(a) ~ 5(c). The input ESD protection circuit is realized by the gate-connect-to-source pMOS (Mp_in) and gate-grounded nMOS (Mn_in) with both the device dimensions (W/L) are drawn as 490/0.5 ($\mu\text{m}/\mu\text{m}$). The output ESD protection circuit is realized by the gate-connect-to-source pMOS (Mp_out), output buffer of pMOS (Mp_b), gate-grounded nMOS (Mn_out), and output buffer of nMOS (Mn_b) with the device dimensions (W/L) of 350/0.5, 140/0.5, 420/0.5, and 70/0.5 ($\mu\text{m}/\mu\text{m}$), respectively. Each gate bias of Mp_b and Mn_b is controlled by the input pad through two series inverters. The traditional ESD protection scheme is shown in Fig. 5(a), which was fabricated and measured as reference. The proposed ESD protection scheme I for the IC with power-down-mode operation is shown in Fig. 5(b), and the junction perimeter of the diodes (D1, D2, and D3) is drawn as 50 μm . The proposed ESD protection scheme II for the IC with power-down-mode operation is shown in Fig. 5(c). The junction perimeter of the diode (D1) is drawn as 50 μm , and the device dimension (W/L) of the Mp5 is drawn as 20/0.5 ($\mu\text{m}/\mu\text{m}$). The power-rail ESD clamp circuit used in the ESD protection scheme is realized by the substrate-triggering field-oxide device [12].

3.1 Leakage Current

The leakage current under normal circuit operating condition is a concern for an ESD protection circuit connected to an I/O pin. The leakage current of the input stage among the different designs under normal circuit operating condition is shown in Fig. 6(a). The leakage current is measured (by HP4155) by applying a voltage ramp from 0 to 3.3V to the input pad under the bias condition of 3.3-V VDD and 0-V VSS. In Fig. 6(a), the maximum leakage currents of the traditional ESD protection scheme, the proposed ESD protection scheme I, and II with a 3.3-V input signal applying to the input pad are 109pA, 134pA, and 122pA, respectively.

The leakage current from the I/O pin to the VDD power line is a major concern when IC goes into power-down-mode operation with VDD of 0V. The leakage currents of the input stage and output stage among the different designs under power-down-mode operating condition are measured and compared in Figs. 6(b) and 6(c), respectively. The leakage current is measured by applying a voltage

ramp from 0 to 3.3V to the input or output pad under the bias condition of 0-V VDD and 0-V VSS. In Fig. 6(b), the leakage currents of the proposed ESD protection scheme I and II under 3.3-V bias at input pad are only $\sim 130\text{pA}$. On the contrary, the traditional ESD protection scheme has a very high leakage current of up to several mA when the input voltage is only increased to 0.7V. The leakage currents of output pad in Fig. 6(c) shows the same result to that in Fig. 6(b), the leakage currents of the proposed ESD protection scheme I and II under 3.3-V bias are $\sim 300\text{pA}$.

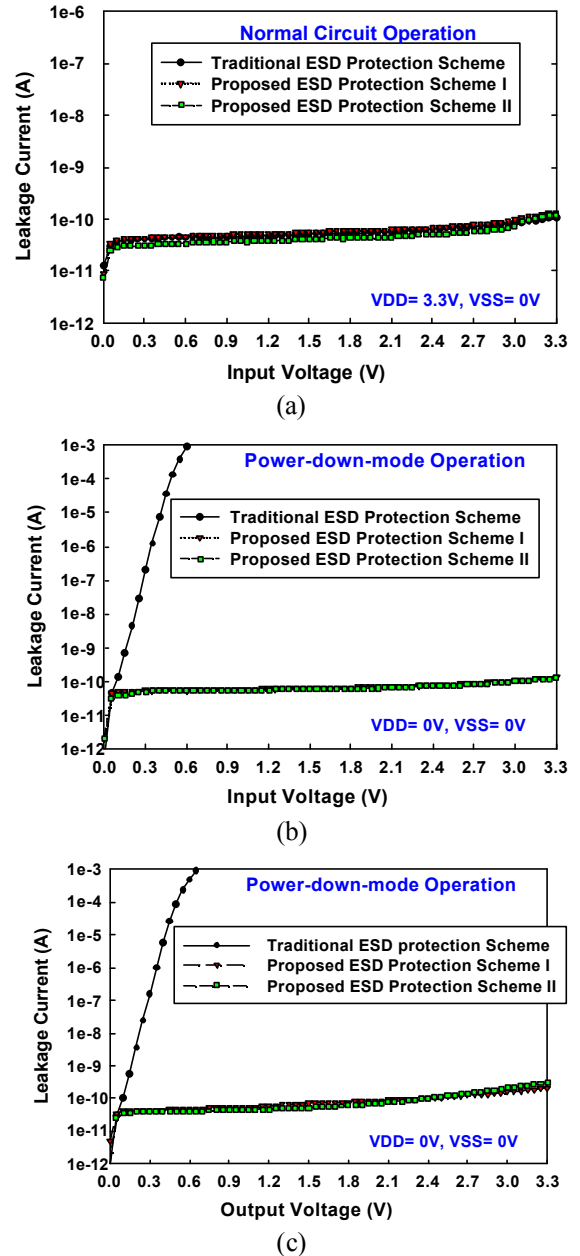


Fig. 6 Comparison of the leakage currents of the proposed ESD protection schemes and the traditional ESD protection scheme for (a) the input stage under normal circuit operating condition, (b) the input stage under power-down-mode operating condition, and (c) the output stage under power-down-mode operating condition.

The high leakage current of the traditional ESD protection scheme is induced by the parasitic diode of pMOS connected between the I/O pin and VDD under forward-biased condition. The leakage current in the proposed ESD protection scheme has been successfully blocked by the diode of D1 or D2. The experimental results have verified that the proposed ESD protection schemes can avoid the leakage current from the I/O pin to VDD power line under the power-down-mode operating condition.

3.2 Function Verification

The measurement setup to verify the function of I/O cells with the proposed ESD protection schemes, or the traditional ESD protection scheme, under normal circuit operating condition and power-down-mode operating condition is shown in Fig. 7. To verify the function among the different designs under normal circuit operating condition, a 0-to-3.3 V voltage pulse with a rise time of 20 ns is applied to the input pad under the bias condition of 3.3-V VDD and 0-V VSS. In addition, to verify the function among the different designs under power-down-mode operating condition, a 0-to-3.3 V voltage pulse with a rise time of 20 ns is applied to the input pad under the bias condition of 0-V VSS but VDD is floating.

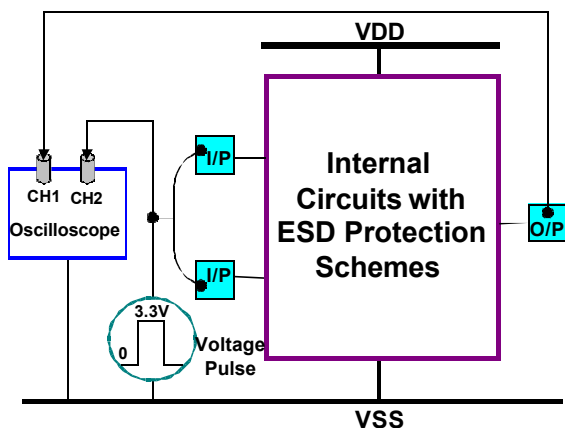
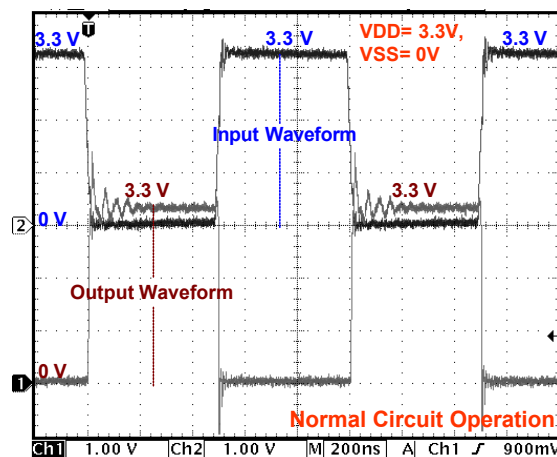


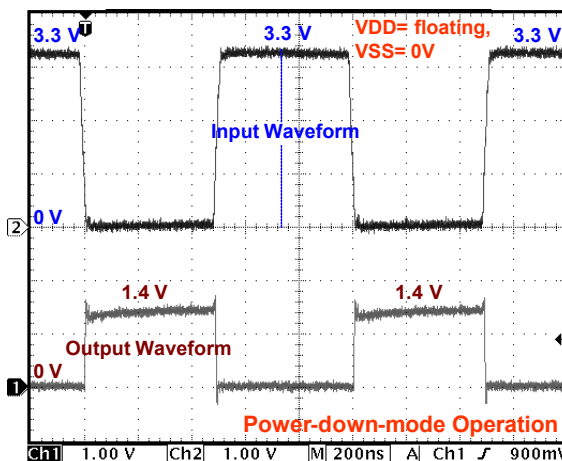
Fig. 7 The measurement setup to verify the function of I/O cells among different ESD protection schemes, under normal circuit operating condition and power-down-mode operating condition.

Figs. 8(a) and 8(b) show the voltage waveforms on the input/output pad of the I/O cells with the traditional ESD protection scheme under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 8(a), the I/O cells with traditional ESD protection circuits can be operated normally under normal circuit operating condition. However, under the power-down-mode condition, the voltage waveform on the output pad is dropped to a voltage level of

~1.4V, when the input voltage level is 0V, as that shown in Fig. 8(b). It implies that the internal circuits are triggered by the input voltage waveform under power-down-mode operating condition, although the circuits are expected to be off. With the wrong voltage waveform at the I/O pads, the system could be malfunction.



(a)

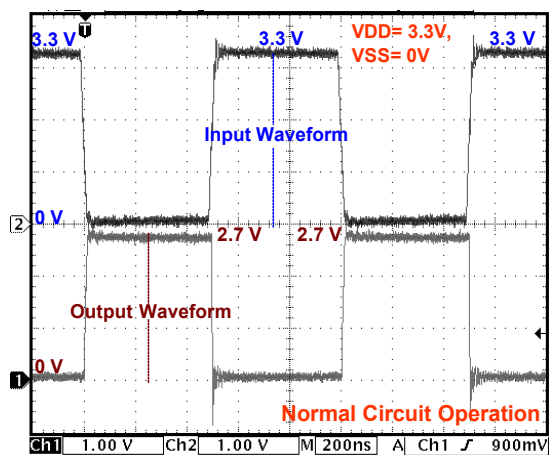


(b)

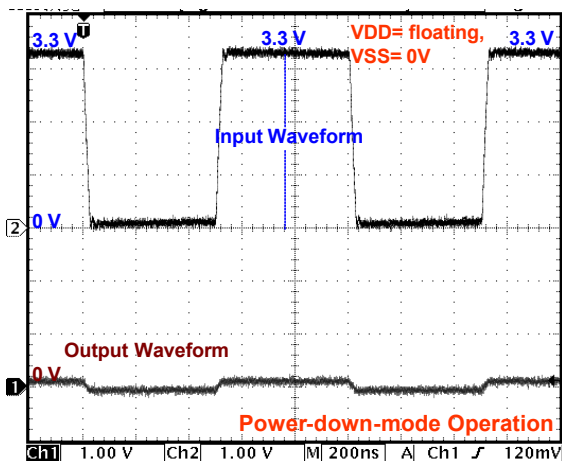
Fig. 8 The measured voltage waveforms on the input/output pads of IC with the traditional ESD protection scheme under (a) normal circuit operating condition, and (b) power-down-mode operating condition. (Y axis = 1 V/Div., X axis = 200 ns/Div.)

Figs. 9(a) and 9(b) show the voltage waveforms on the input/output pad of the I/O cells with the proposed ESD protection scheme I under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 9(a), the I/O cells with the proposed ESD protection scheme I can be operated normally under normal circuit operating condition. The high voltage level on the output pad is about 2.7V (VDD-V_d, where V_d is the cut-in voltage of the diode D2). In Fig. 9(b), the voltage level on the output pad is always kept at ~0V

under power-down-mode operating condition. It implies that the internal circuits can be really turned off by the proposed ESD protection scheme I under power-down-mode operating condition. In addition, the voltage waveforms on the input/output pad of I/O cells with the proposed ESD protection scheme II show the same results to that in Figs. 9(a) and 9(b) under normal circuit operating condition and power-down-mode operating condition, respectively.



(a)



(b)

Fig. 9 The measured voltage waveforms on the input/output pads of IC with the proposed ESD protection scheme I under (a) normal circuit operating condition and (b) power-down-mode operating condition. (Y axis = 1 V/Div., X axis = 200 ns/Div.)

3.3 ESD Robustness

The human-body-model (HBM) ESD robustness of the proposed ESD protection schemes under the four pin-combination modes of ESD stress on the I/O pad and VDD to VSS ESD stress is listed in Table I. In this ESD verification, the failure criterion is defined as the leakage current of the circuits after ESD zapping is greater than $1\mu\text{A}$ under the normal operating voltage of 3.3V. For the proposed ESD protection scheme I, the ESD levels of the input pad

under the PS- and PD-mode ESD stresses are 7.5kV, whereas the ESD levels of the output pad under the PS-, PD-, NS-, and ND-mode ESD stresses, or those of VDD to VSS ESD stress are even over 8kV. For the proposed ESD protection scheme II, the ESD levels of the input pad under the PS- and PD-mode ESD stresses are 7.75kV, and the ESD levels of the output pad under the PS- and PD-mode ESD stresses are 7.5kV and over 8kV, respectively. From the experimental results, the ESD levels of the I/O pad under the PS- and PD-mode ESD stresses can be efficiently improved by the proposed ESD protection schemes for the IC with power-down-mode operation.

Table I

HBM ESD robustness of the proposed ESD protection schemes for the IC with power-down-mode operation

HBM ESD Stress Protection Scheme	PS-Mode VSS(+)	NS-Mode VSS(-)	PD-Mode VDD(+)	ND-Mode VDD(-)	VDD-to-VSS(+)	VDD-to-VSS(-)
Scheme I (Input Pin)	7.5kV	>8kV	7.5kV	>8kV	>8kV	>8kV
Scheme I (Output Pin)	>8kV	>8kV	>8kV	>8kV		
Scheme II (Input Pin)	7.75kV	>8kV	7.75kV	>8kV	>8kV	>8kV
Scheme II (Output Pin)	7.5kV	>8kV	>8kV	>8kV		

4 Conclusion

The new ESD protection schemes for IC with power-down-mode operation have been successfully designed and verified in a 0.35- μm CMOS process. Under the normal circuit operating condition, the I/O cells with proposed ESD protection schemes can be operated normally. Under the power-down-mode operating condition, the proposed ESD protection schemes can provide the I/O pad with a very low leakage current and avoid to trigger the circuits those should be “off”. Whole-chip ESD protection design can be achieved by the proposed ESD protection schemes to sustain the HBM ESD stress of 7.5kV in a 0.35- μm CMOS process.

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