# Controlling Factors of Drain Induced Barrier Lowering Coefficient in Short Channel MOSFET

**B. JHARIA*, S. SARKAR and R. P. AGARWAL**
Department of Electronics and Computer Engineering
Indian Institute of Technology Roorkee, Roorkee –247667, INDIA

*Abstract*: - An analytical study of drain induced barrier-lowering coefficient in short channel MOSFET is presented. Analysis shows that the DIBL-coefficient is a non-linear decreasing function of drain-source voltage. This makes the resulting shift in threshold voltage to behave similarly. The threshold voltage-shift can be reduced by decreasing oxide thickness and increasing the substrate doping. The DIBL-coefficient decreases with increase in temperature and this decrease is more pronounced in short channel devices.

*Key-Words*:-MOSFET, DIBL-coefficient, Threshold voltage-shift, Short-channel effect

## 1 Introduction

The threshold voltage of a MOSFET is known to vary with drain-source voltage, $V_{DS}$ [1-6], because of drain-induced barrier lowering (DIBL). Most of the analytical works considered this shift in threshold voltage (with change in $V_{DS}$) for constant effective channel length. Theoretical as well as experimental observation shows that for constant effective length the threshold voltage shift is linearly related to $V_{DS}$. The rate of change of threshold voltage-shift with $V_{DS}$ is known as the DIBL-coefficient, $\sigma$.

Both theoretical and experimental studies show that for constant effective length, the DIBL-coefficient is independent of $V_{DS}$. When a MOSFET, operates with variable $V_{DS}$, channel length modulation makes the effective length to vary. Thus, it is of interest to know the influence of $V_{DS}$ on DIBL-coefficient of an individual MOSFET. An accurate estimate of the shift in the potential minimum is especially important since the channel current is exponentially dependent on the barrier height.

The purpose of this paper is to analyze the dependence of DIBL-coefficient and threshold voltage-shift of an individual MOSFET as its drain-source voltage. The influences of some technological parameters are also examined.

*On study leave under Q.I.P. from Govt. Engineering College, Jabalpur.

## 2 Theory

The threshold voltage shift in terms of DIBL-coefficient $\sigma$ and $V_{DS}$ is

$$\Delta V_T = -\sigma V_{DS} . \tag{1}$$

The DIBL-coefficient is given by [1]

$$\sigma \approx \frac{2\eta\chi\, d_{dep}^{0}}{\lambda} \frac{\sinh\left(\frac{x_s}{\lambda}\right)}{\cosh\left(\frac{L-x_d}{\lambda}\right) - \cosh\left(\frac{x_s}{\lambda}\right)} \tag{2}$$

where $\eta$ is the sub threshold ideality factor, $\chi$ is a constant (on the order of 0.5) which accounts for the charge sharing in depletion region, L is the gate length, $x_s$ is the source-channel depletion width, $x_d$ is the drain-channel depletion width, $d_{dep}^{0}$ is the depletion width at zero drain-source bias and $\lambda$ is a parameter that accounts for the effect of gate oxide thickness on depletion layer width.

These parameters can be expressed by

$$\eta = 1 + c_{dep}/c_{ox} \tag{3}$$

$$x_s = \sqrt{\frac{2\varepsilon_s}{qN_a}\left(-\psi_s^o\right)} \tag{4}$$

$$x_d = \sqrt{\frac{2\varepsilon_s}{qN_a}\left(V_{DS} - \psi_s^0\right)} \tag{5}$$

$$d_{dep}^0 = \sqrt{\frac{2\varepsilon_s}{qN_a}\left(\psi_s^0 + V_{bi}\right)} \quad (6)$$

$$\lambda = d_{dep}^0 \left(1 + \frac{\varepsilon_i\, d_{dep}^0}{\varepsilon_s\, t_{ox}}\right)^{-1/2} \quad (7)$$

and, $\psi_s^0 = -V_{bi} + 2\varphi_b + V_{GT} / \eta$ (8)

where $c_{ox}$ is the gate oxide capacitance, $c_{dep}$ is the depletion layer capacitance, $\psi_s^0$ is the constant potential at the semiconductor-insulator interface at zero drain bias, $N_a$ is the acceptor doping density in the substrate, $\varepsilon_s$ is the dielectric permittivity of the semiconductor, $\varepsilon_i$ is the electrical permittivity of the insulator, $V_{bi}$ is built-in-potential, $t_{ox}$ is the thickness of the gate oxide, and $\varphi_b$ is the bulk potential. For the gate-source voltage $V_{GS}$ and zero drain-source bias threshold voltage $V_{T0}$, the parameter $V_{GT}$ is

$$V_{GT} = V_{GS} - \left(V_{T0} - \sigma V_{DS}\right). \quad (9)$$

Defining

$$\left.\begin{aligned} a_1 &= \frac{2\varepsilon_s}{qNa}\left(2\varphi_b + \frac{\left(V_{GS} - V_{T0}\right)}{\eta}\right); \\ a_2 &= \frac{2\varepsilon_s}{\eta qNa} V_{DS}; \\ a_3 &= \frac{2\varepsilon_s}{qNa} V_{bi}; \\ \text{and,} \quad a_4 &= \frac{\varepsilon_i}{\varepsilon_s\, t_{ox}}. \end{aligned}\right\} \quad (10)$$

Combining (10) and (3)-(8)

$$x_s = \sqrt{a_3 - a_1 + a_2\sigma}\,; \quad (11)$$

$$x_d = \sqrt{a_3 - a_1 + (\eta + \sigma)a_2}\,; \quad (12)$$

$$d_{dep}^0 = \sqrt{a_1 - a_2\sigma}\,; \quad (13)$$

$$\text{and, } \lambda = \frac{\sqrt{a_1 - a_2\sigma}}{1 + a_4\sqrt{a_1 - a_2\sigma}}. \quad (14)$$

Substituting (11)-(14) in (2)

$$\sigma - \frac{2\eta\chi\left(1 + a_4\sqrt{a_1 - a_2\sigma}\right)\sinh(A)}{\cosh(B) - \cosh(A)} = 0 \quad (15)$$

where $A = \dfrac{\left(\sqrt{a_3 - a_1 + a_2\sigma}\right)\left(1 + a_4\sqrt{a_1 - a_2\sigma}\right)}{\sqrt{a_1 - a_2\sigma}}$;

and,

$$B = \frac{\left(L - \sqrt{a_3 - a_1 + a_2(\eta + \sigma)}\right)\left(1 + a_4\sqrt{a_1 - a_2\sigma}\right)}{\sqrt{a_1 - a_2\sigma}}.$$

$\sigma$ as a function of $V_{DS}$ can be obtained by solving (15).

## 3 Results and Discussion

To analyze the $V_{DS}$ dependence of $\sigma$, the case of an n-channel MOSFET, characterized by the parameters given in the Table 1 is considered.

Table1. MOSFET Parameters

| | | |
|---|---|---|
| $\varepsilon_s$ | 1.04E-10 | $Fm^{-1}$ |
| $\varepsilon_i$ | 3.36E-11 | $Fm^{-1}$ |
| $N_a$ | 7.00E+22 | $m^{-3}$ |
| $n_i$ | 6.50E+14 | $m^{-3}$ |
| $t_{ox}$ | 8.6 | nm |
| $V_T$ | 0.2884 | V |
| $\eta$ | 1.196 | |

Figure 1 illustrates the variation of DIBL-coefficient with drain- source voltage. $\sigma$ is a non-linear function of $V_{DS}$, and it increases as $V_{DS}$ is increased. Furthermore the increase in $\sigma$ is more pronounced in the higher regime of $V_{DS}$. The concept of $V_{DS}$ independent $\sigma$ is

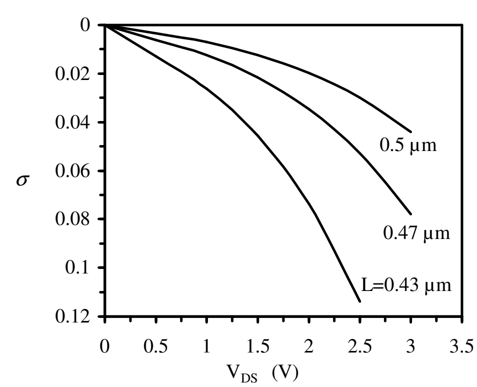


Fig. 1. Variation of DIBL-coefficient with drain - source voltage for different channel lengths.

valid in the lower regime of drain-source voltage.

Figure 1 also shows the expected channel length dependence of $\sigma$, that is it is higher for devices of shorter channels. The slope of the $\sigma$-$V_{DS}$ characteristics is relatively higher in a device of short channel.

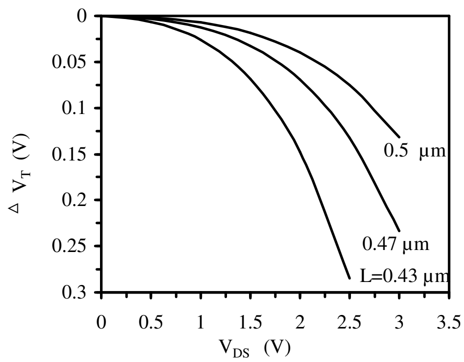


Fig. 2. Threshold voltage shift as a function of drain bias for different channel lengths.

The effect of non-linear variation of $\sigma$ with $V_{DS}$ results in a non-linear relationship between the threshold voltage-shift, $\Delta V_T$ and $V_{DS}$. Figure 2 shows that in the higher regime of $V_{DS}$, a large swing in $\Delta V_T$ may result for a small change in $V_{DS}$. The $\Delta V_T$ swing is larger in cases of a short channel. The non-linearities in the $\sigma$-$V_{DS}$ and $\Delta V_T$-$V_{DS}$ curves shows that $\sigma$ determined from $\Delta V_T$-$V_{DS}$ plots with effective channel length as the parameter does not yield a correct picture of DIBL-effect on threshold voltage.

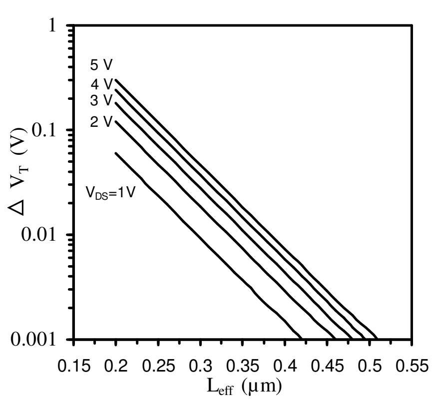


Fig.3. Shift in threshold voltage as a function of effective channel length with $V_{DS}$ as the parameter.

Figure 3 shows the logarithmic plot of $\Delta V_T$ as obtained from (15). This is in agreement with experimental results of Chung et al. [2].

The dependence of $\sigma$ on oxide thickness and substrate doping concentration are shown in Figure 4. Significant reduction in threshold voltage shift can be achieved by decreasing oxide thickness, $t_{ox}$ or increasing doping concentration, $N_a$.

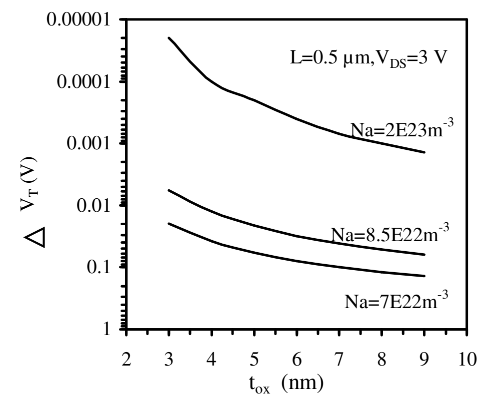


Fig. 4. Variation of threshold voltage shift with oxide thick- ness for different doping

Fikry et al. [4] showed that the DIBL parameter is almost independent of temperature between 50 and 300K but it is not so in our case. It is observed that the $\sigma$ decreases with increase in temperature and this decrease is more pronounced for short channel devices. Figure 5 shows the variation of $\sigma$ with temperature. This is because of the variations of

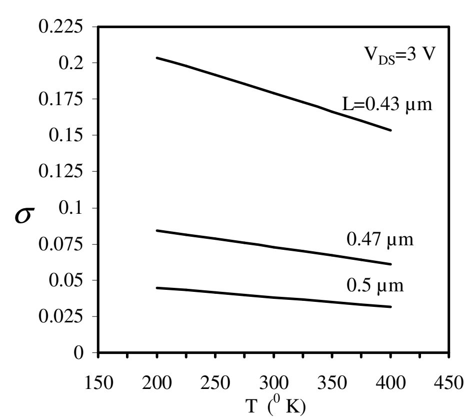


Fig.5. DIBL-coefficient versus temperature for different channel lengths.

the $\eta$, $\psi_s^0$, and $V_{bi}$ with temperature. This is in agreement with experimental results of Ghitani [5].

## 4 Conclusion

The dependence of DIBL-coefficient and threshold voltage-shift due to drain-source voltage variation is analyzed. It is found that the DIBL-coefficient being a non-linear function of drawn gate length, the threshold voltage-shift varies non-linearly with drain-source voltage. Furthermore, the threshold voltage shift can be controlled by proper selection of gate oxide thickness and substrate doping. Also, it is observed that the DIBL-coefficient decreases with increase in temperature and this decrease is more pronounced for short channel devices.

*References*:


[1] T.A. Fjeldly and M. Shur, Threshold Voltage Modeling and the Subthreshold Regime of Operation of Short-Channel MOSFET's, *IEEE Trans. on Electron Devices*, Vol.40,No.1,1993, pp.137-145.

[2] J. E. Chung, M. C. Jeng, J. E. Moon, P. K. Ko, C. Hu, Performance and reliability design issues for deep-sub-micrometer MOSFET's, *IEEE Trans. on Electron Devices*, Vol.38, No.3, 1991, pp. 545-554.

[3] Z. H. Liu, C. Hu, J. H. Huang, T. Y. Chan, M. C. Jeng, P. K. Ko, Y. C. Cheng, Threshold Voltage Model for Deep-Submicrometer MOSFET's, *IEEE Trans. on Electron Devices*, Vol.40, No. 1, 1993, pp.86-94.

[4] W. Fikry, G. Ghibaudo and M. Dutoit, Temperature Dependence of Drain-Induced Barrier Lowering in Deep-Submicrometer MOSFETs, *IEEE Electron Devices Letters*, Vol.30, No. 11, 1994, pp. 911-912.

[5] H. El Ghitani, DIBL-Coefficient in Short-Channel NMOS Transistors, *16th National Radio Science Conference, NRSC'* 1999, pp. D4-1-5.

[6] A. A. Mutlu, M. Rahman, Two-Dimensional Analytical Model for Drain Induced Barrier Lowering (DIBL) in Short Channel MOSFETs, *IEEE Proceedings* 2000, pp. 340-344.