Improved Characteristics of Ultra-Thin Cerium Dioxide with Rapid Thermal Annealing

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ABSTRACT

In this study, the characteristics of ultra–thin cerium dioxide with rapid thermal annealing are investigated. The cerium dioxide film with post-deposition rapid thermal annealing exhibits the thin effective oxide thickness (EOT ~1.4nm for the RTA950^oC sample) and superior properties. Based on the experimental results, the rapid thermal annealing can effectively improve the reliability and quality of the cerium dielectric film owing to the elimination of traps in the dielectrics and interfacial layer between CeO_2/Si. In addition, the cerium dioxide has excellent thermal stability on Si substrate and high temperature to crystallize. The cerium dioxide with post-deposition rapid thermal annealing is a potential candidate for the future ultra-large scale integrated circuit (ULSI) applications.

I. INTRODUCTION

Recently, many high dielectric constant (high-k) materials like Al_2O_3, ZrO_2, and HfO_2 [1]-[4] have been widely studied to replace the silicon dioxide owing to the inevitability of its high leakage as the thickness scales down. Gate dielectric materials with a high dielectric constant, a low interface state density and a good thermal stability appear to be promising for next generation gate dielectric applications. Moreover, materials with too lower or too higher dielectric constant may not be adequate choice for alternative gate dielectric application. Ultra high-k materials such as STO or BST may cause fringing field induced barrier lowing effect [5]. And materials having relatively low dielectric constant such as Al_2O_3 and Y_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4 [6]. Cerium dioxide (CeO_2), which has been extensively researched for its use as a buffer layer for $YBa_2Cu_3O_{(7-x)}$ (YBCO) on sapphire [7], a buried insulator for silicon-on-insulator (SOI) [8] and $PbZrTiCeO_3$ (PZT) ceramics [9], has lately been used as gate dielectric material [10]. Many superior properties of cerium dioxide, such as a lattice nearly matched to that of silicon (a=0.5411nm) and a sufficiently high dielectric constant (~26) ensure its high thermal stability on silicon and high scaling capacity. In this study, the electrical and physical characteristics of ultra–thin cerium dielectrics with rapid thermal annealing are investigated.

II. EXPERIMENT

Al/CeO_2/n-Si capacitors of an area of 6.36×10^{-5} cm^2 were fabricated on 4 inch n-type (100)-oriented Si wafers. Figure 1 shows key process flows of cerium dielectrics with post-deposition anneal (PDA). All samples were first cleaned by a standard Radio Corporation of America clean. The CeO_2 film was then deposited by electron beam evaporation. After the gate dielectric had been formed, the samples were treated by rapid thermal anneal (RTA) at 600 ~ 950^oC for 60s in N_2 ambient. Then, a 5000 Å Al film was deposited on the CeO_2 film by a thermal coater. After that, the gate of the capacitor was defined lithographically and etched. Finally, a 5000 Å Al film was also deposited on the backside of the wafer to form the ohmic contact. There may be an interfacial oxide layer between CeO_2 and Si. Therefore, the barrier parameters to be discussed in this paper are "effective" values that include the effects of these interfacial layers. The effective oxide thickness (EOT) was estimated by the high frequency (0.1 MHz) capacitance versus voltage (C-V) curve in the strong accumulation region without considering quantum mechanical effects. The electrical properties were measured by using an HP 4156B semiconductor parameter analyzer and an HP4284A precision LCR meter.

III. RESULTS AND DISCUSSION

Figure 2 shows the J-E characteristics of these samples. The breakdown electric field becomes larger and the leakage current density decreases as the annealing temperature increases. It should be noted that CeO_2 still has excellent electrical performance, even through the high temperature annealing up to 950^oC. It is seemed that the CeO_2 film does not crystallized after high temperature RTA treatment. Figure 3 shows the high frequency (0.1MHz) capacitance versus gate voltage (C-V) characteristics of cerium dielectrics with rapid thermal annealing at different annealing temperature. We can see that as the annealing temperature increases, the EOT decreases simultaneously. High temperature annealing can densify the CeO_2 film and

make the dielectrics more stoichiometric. Besides, there are some distortions for the as-deposited sample and the sample with RTA at 600°C. We believe that it is owing to the serious interface state (fast traps) at the CeO_2/Si substrate interface [11]. Ultra high temperature annealing may help to improve this distortion.

Figure 4~7 show the high resolution transmission electron microscopy (HRTEM) images of the cerium dioxide without treatment and with rapid thermal annealing at 600~950°C, respectively. For the TEM image of the as-deposited sample in Fig. 4, the physical thickness of the CeO_2 film is about 54 Å and obviously there is an interfacial layer (IL) about 18 Å existing between CeO_2 and the Si substrate. From Fig.5 to Fig.7, we can find that as the annealing temperature increases, the thickness of the CeO_2 film becomes thinner and densified. Besides, it is apparent that the interfacial layer thickness gradually decrease and finally almost disappear. Therefore, we can rationally suppose that the high temperature annealing can reduce the interfacial layer and improve the cerium dielectrics. The HRTEM results can explain the C-V characteristics of cerium dielectrics, as shown in Fig.3.

Figure 8 shows the Weibull plots of the leakage current density at V_g=1V for the cerium dioxide treated by RTA at different temperature. We can observe the RTA treatment improves not only the leakage current density but also the distribution uniformity (Weibull slope). Figure 9 shows the Weibull plots of the dielectric breakdown voltage for the samples treated by RTA. As the RTA temperature increases, the breakdown voltage is raised form 1.4V to 2.3V. The Weibull plots of time to breakdown for the samples treated by RTA is presented in Figure 10.The samples are stressed at V_g=1V. Obviously, the time-dependent dielectric breakdown (TDDB) is improved after high temperature RTA treatment. Furthermore, the RTA treatment can effectively improve the reliability of the cerium dielectric film owing to the elimination of traps in the dielectrics and interfacial layer between CeO_2/Si.

Figure 11~12 show the Auger electron spectrometer (AES) analysis of the as-deposited and RTA 950℃ samples respectively. Form Fig.11, we can find the apparently interfacial layer between CeO_2 and Si substrate (marked in this figure). After the RTA 950℃ treatment in Fig.12, the composition of CeO_2 film is still stable and the interfacial layer becomes smaller. Figure. 13~14 show the Ce3*f* electron spectroscopy for the chemical analysis (ESCA) spectra of the as-deposited and RTA 950℃ samples. A take-off angle (TOA) of 90° was used to measure the ESCA spectra. The peaks of Ce-O bonding are respectively at 884 eV ($Ce3d_{3/2}$) and 902 eV ($Ce3d_{5/2}$). We can find the peaks and profiles of the as-deposited and RTA 950℃ samples are almost the same. It means that any other bonding, especially Ce-Si bonding, dose not formed in the cerium dielectrics after high temperature RTA treatment. Therefore, the cerium dielectric has excellent thermal stability on Si substrate.

IV. CONCLUSIONS

In conclusion, we propose an ultra-thin cerium dioxide with post-deposition rapid thermal annealing, which exhibits the thin EOT (~1.4nm for the RTA950°C sample) and superior properties. Based on the experimental results, the rapid thermal annealing can effectively improve the reliability and quality of the cerium dioxide owing to the elimination of traps in the dielectrics and interfacial layer between CeO_2/Si. Besides, the cerium dioxide has excellent thermal stability on Si substrate and high temperature to crystallize. Therefore, it can be the candidate for the future ultra-large scale integrated circuit (ULSI) applications.

ACKNOWLEDGEMENT

The authors would like to thank the National Science Council of the Republic of China, Taiwan, for financially supporting this research under Contract No. NSC92-2215-E009-022. The National Nano Device Laboratory, R.O.C. is also appreciated for their technical assistance.

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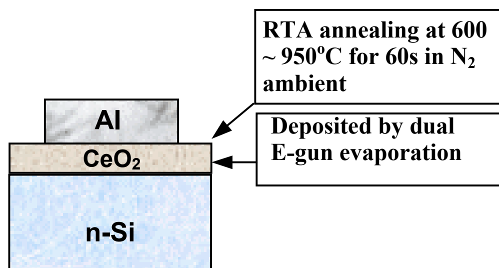

Fig.1 Key process flows of the fabrication for cerium dielectrics with post-deposition anneal (PDA).

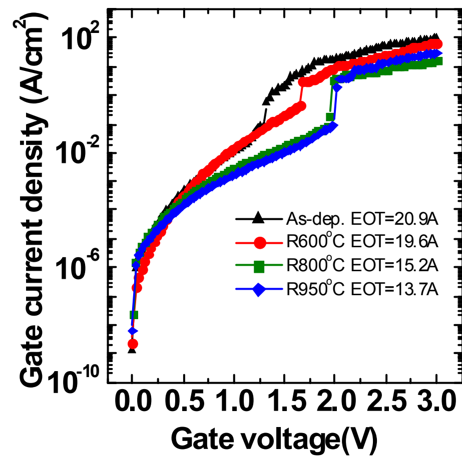

Fig.2 The J-E characteristics of cerium dielectrics with RTA at different temperature.

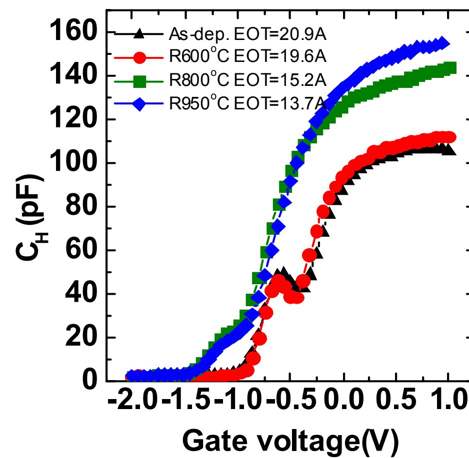

Fig.3 The high frequency (100kHz) C-V characteristics of cerium dielectrics with RTA at different temperature.

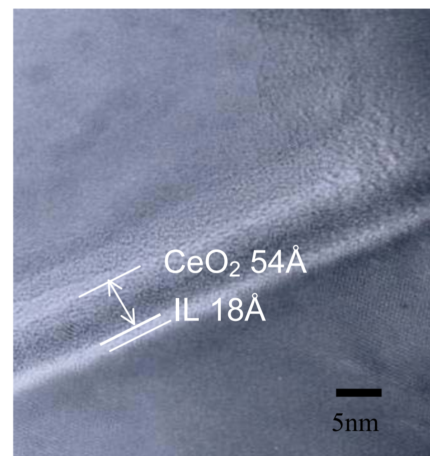

Fig.4 The TEM image of the cerium dioxide without RTA treatment

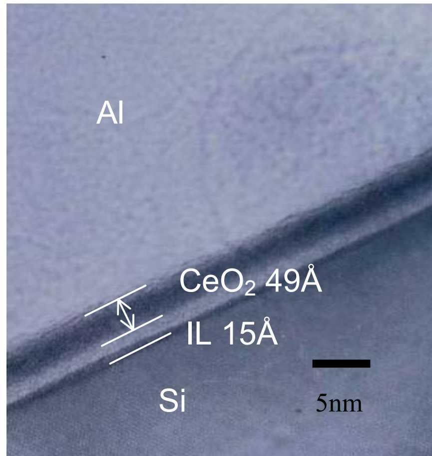

Fig.5 The TEM image of the cerium dioxide with RTA 600°C.

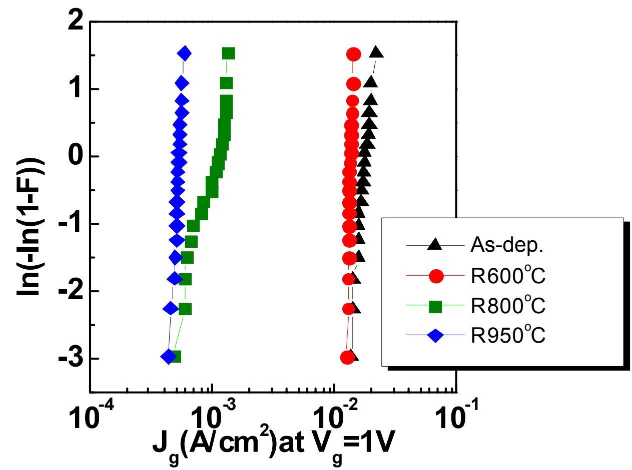

Fig.8 Weibull plots of the leakage current density at V_g=1V for the samples treated by RTA.

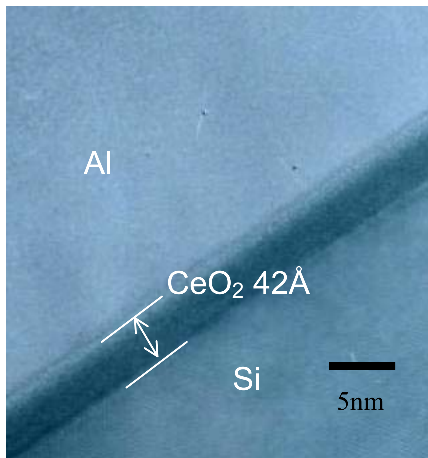

Fig.6 The TEM image of the cerium dioxide with RTA 800°C.

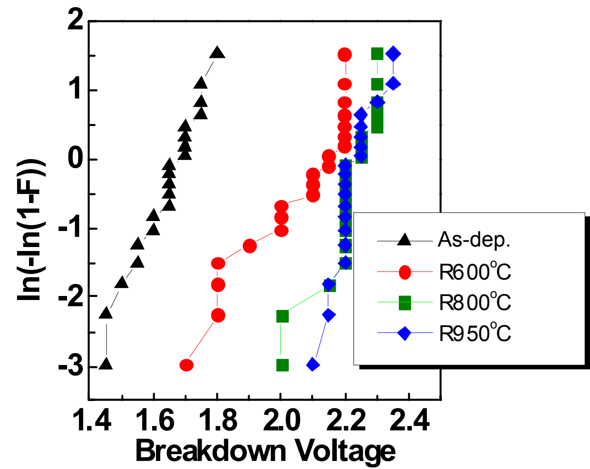

Fig.9 Weibull plots of dielectric breakdown voltage for the samples treated by RTA.

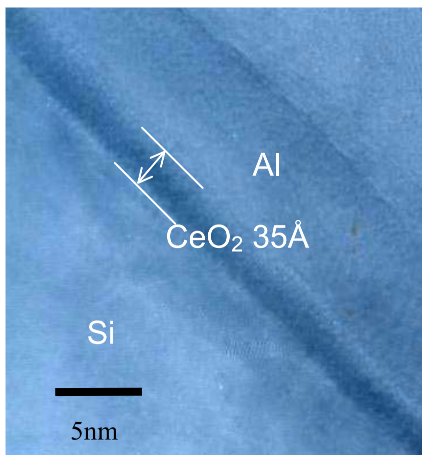

Fig.7 The TEM image of the cerium dioxide with RTA 950°C.

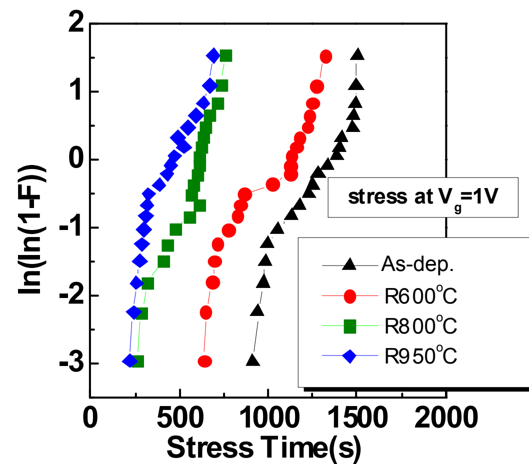

Fig.10 Weibull plots of time to breakdown for the samples treated by RTA.

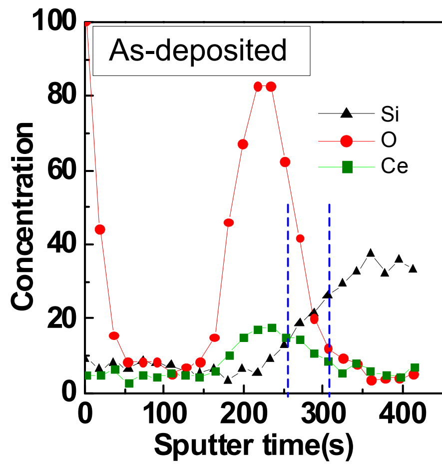

Fig.11 AES analysis of the as-deposited sample.

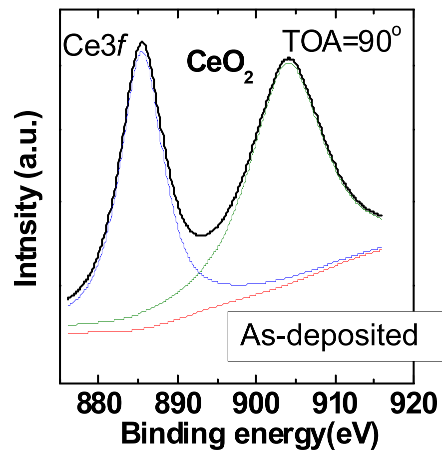

Fig.13 Ce3*f* ESCA spectra of the as-deposited sample.

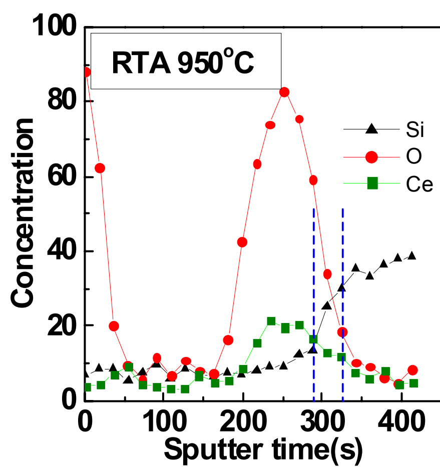

Fig.12 AES analysis of the sample treated by RTA 950°C.

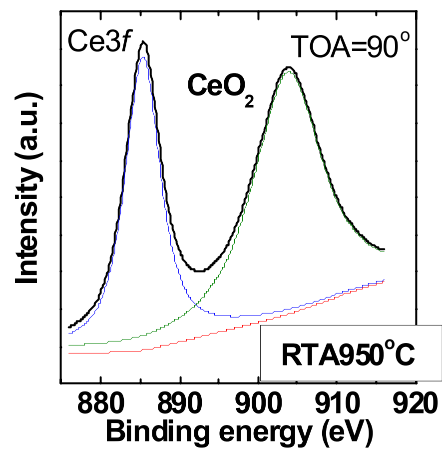

Fig.14 Ce3*f* ESCA spectra of the sample treated by RTA 950°C.