

The Characterization of HfO₂ Thin Film Treatment by N₂O

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Abstract — The physical and electrical characteristics of hafnium oxide (HfO₂) in MOS capacitors with various annealing gas and annealing conditions were investigated. The results show that hafnium oxide with N₂O annealing samples has best reliability than other ones. Besides, it is shown that HfO₂ with N₂O annealed sample has thicker thickness and smaller dielectric constant compared with other annealing conditions. This result may be contributed to that ionic oxygen penetrate through HfO₂ films and react with silicon substrate. This can be found in cross-section TEM picture. In the above discussions, HfO₂ is indeed an alternative gate dielectric for future VLSI gate applications for gate oxide < 12Å or below process.

Index Terms—High-K materials, N₂O anneal, hafnium oxide.

I. Introduction

According to 1999 ITRS roadmap, for beyond 0.1 μm technology, ultra thin gate oxide with EOT of less than 12 Å are needed. [1] However, SiO₂ is facing the scaling limitation due to direct tunneling current that limits low power application and reliability problems [2-3].

Key issues related to the development of high-K gate dielectric material are thermal stability of high-K materials in direct contact with silicon and poly-Si at high temperatures, high quality interfaces with channel and gate electrode, reasonable barrier height to achieve low leakage current, and suppressed boron penetration.

Recently, HfO₂ films have emerged as the promising gate dielectric due to its dielectric constant of up to 40, energy gap of 5.65eV, and thermodynamically stable when in contact with Si. [4]

In this work, we used HfO₂ as gate dielectric material of capacitor and then annealed with N₂O and N₂. Besides, we investigated the mechanism of N₂O and N₂ annealing for different temperature and time of HfO₂ gate dielectric material.

II. Experimental

For this research, silicon wafers were cleaned and different physical thickness (80 and 100 Å) of HfO₂ were deposited by reactive sputtering method. Then these samples were annealed using Rapid Thermal annealing methods with different ambient (N₂ and N₂O) for different time (15, 30, 45 and 60 seconds) and different temperatures (800, 850 and 900°C). Finally, gold and Alumini were chosen for top and back side electrodes, respectively. Control samples were also fabricated by Rapid Thermal N₂O oxidation (RTN₂O) with the same oxidation conditions compared with HfO₂ ones. We use HP4285 for capacitor-voltage high frequency measurement and HP4195 for current-voltage measurement. The results were shown in Fig1 and 2.

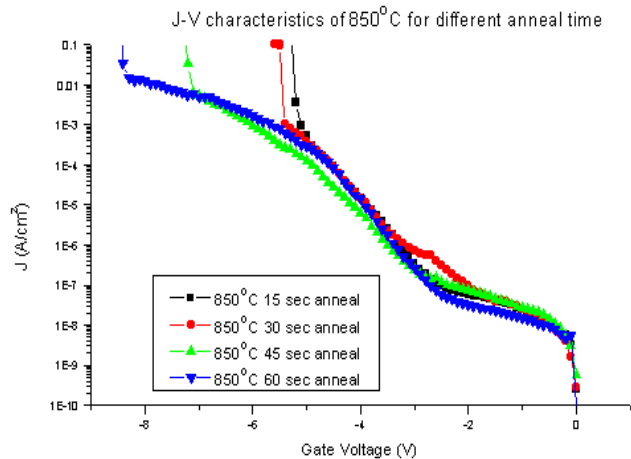


Fig.1 J-V Characteristics of 850°C anneal for different anneal time (15 sec, 30 sec, 45 sec and 60 sec with N₂O) T_{HfO2}=80Å

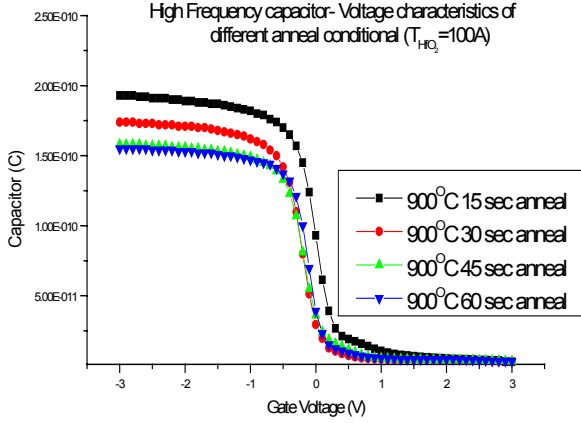


Fig.2 High Frequency C-V for different anneal conditions.

III. Results and Discussion

Fig.3 shows the equivalent oxide thickness (EOT) for different annealing processes. The EOT is calculated from the formula

$$EOT = \frac{\epsilon_{ox} \epsilon_0}{C} A$$

And in those formulas, ϵ_{ox} is the relative dielectric constant of SiO_2 , usually is the value of 3.9, ϵ_0 represents the dielectric constant in vacuum, and is the value of $8.85 \text{ e-}14 \text{ F/cm}$, C is the accumulation capacitor after C-V measurement by HP 4285, A is pattern area.

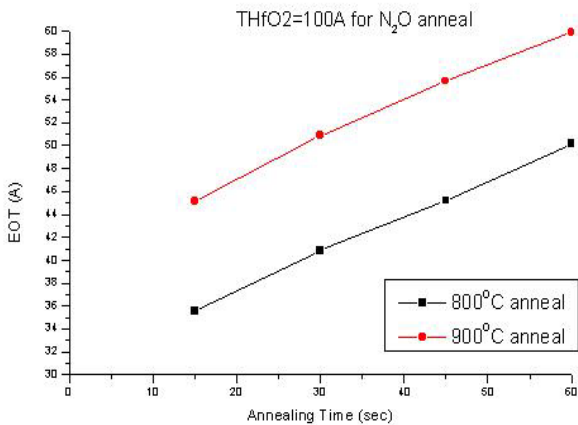


Fig.3 Extracted EOT v.s annealing time for different annealing temperatures ($T_{\text{HfO}_2}=100\text{A}$ with N_2 anneal)

From the data shown above, we observed that

EOT increases with increasing temperature and anneal time. This is due to that ionic oxygen penetrate through HfO_2 layer and react with Si substrate to form a interface layer between HfO_2 and silicon substrate. The cross-sectional TEM picture of Fig.4 also confirms this phenomenon.

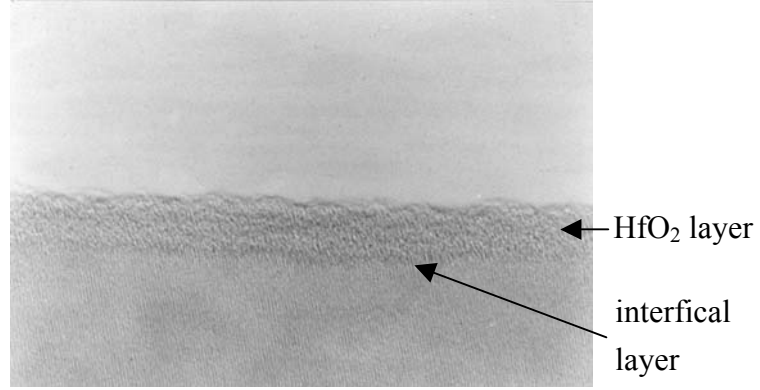


Fig.4 TEM picture of HfO_2 gate dielectric capacitor. The interfacial layer is seen obviously.

At the same time, we also extracted dielectric constant by the method :

$$\text{Dielectric Constant } t = \frac{3.9 \times (Phy_1 - Phy_2)}{EOT_1 - EOT_2}$$

And at here, Phy_1 and Phy_2 stands for two different physical thickness of HfO_2 layer after annealing. EOT_1 and EOT_2 are two different equivalent oxide thickness, respectively. When using this formula, we have an assumption : it supposed that the interfacial layer over whole dielectric and after annealing is not changed. In this way, we have dielectric constant approach to ideal value 30.

Fig.5 shows for that the dielectric constant after higher temperature is lower than that under lower temperature anneal. That is due to at higher temperature anneal, there will grow thicker interfacial layer with lower dielectric constant (<10), therefore, the dielectric constant of higher temperature annealing will be lower.

IV. Conclusion

Several findings are present at below :

- (1) Gate leakage current of HfO₂ gate dielectric is smaller than that of RTN₂O gate dielectric for about 1-2 orders with proper anneal conditions.
- (2) After proper annealing conditions, breakdown field of HfO₂ gate dielectric can be larger than SiO₂ gate dielectric.

From above discussions, we can conclude that HfO₂ has several advantages such as low leakage current, larger breakdown field and good dielectric strength. That means HfO₂ is indeed an alternative gate dielectric for future VLSI gate applications for gate oxide <12Å or below process.

Reference

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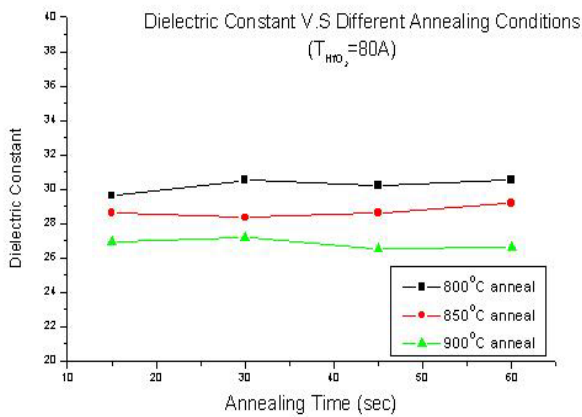


Fig.5 Dielectric Constant v.s annealing time for different annealing temperatures

Fig.6 shows that the leakage current density compared with three different gate dielectric: HfO₂ gate dielectric annealed with N₂O and N₂, and RTN₂O oxidation SiO₂ gate dielectric. From the plot, we can find that the leakage current density of RTN₂O oxidation SiO₂ gate dielectric is of the order of 1E-6, for HfO₂ gate dielectric annealed with N₂O and N₂ are 1E-8 and 1E-7 respectively. From our earlier discussion, lower leakage current means lower trap density and higher physical thickness. We compare with HfO₂ dielectric and RTN₂O dielectric, the leakage current of HfO₂ dielectric is lower, then there we may use it as future gate dielectric.

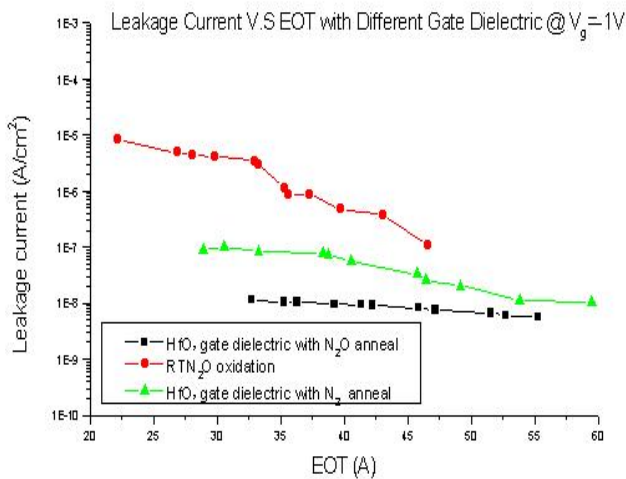


Fig.6 Leakage current with different gate dielectric.

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