Geometric Effect on Electrical Characteristics for Sub-10 nm Double Gate Metal-Oxide-Semiconductor Field Effect Transistors

HUNG-MU CHOU[1], JAM-WEM Lee[2], and YIMING LI[2,3,*]
[1]Department of Electrophysics, National Chiao Tung University
[2]Departmenet of Nano Device Technology, National Nano Device Laboratories
[3]Microelectronics and Information Systems Research Center, National Chiao Tung University
[*] P.O. Box 25-178, Hsinchu 300, TAIWAN

Abstract: - Double gate metal-oxide-semiconductor field effect transistors (DG MOSFETs) have recently been of great interest in modern nanoelectronics community. Device channel length L, thickness of silicon film (T_{si}), and oxide thickness (T_{ox}) play important role in optimal characteristics design for DG MOSFETs. In this paper, we investigate the geometric effect on electrical characteristics for ultrashort nanoscale (sub-10 nm) DG MOSFET devices by considering quantum correction transport model.

Key-Words: - DG MOSFET, geometric effect, Drain current, On/Off current, Channel length effect, Silicon film thickness effect, Modeling and Simulation

DG MOSFETs have recently been of great interest in modern nanoelectronics community [1,2]. Device channel length L, thickness of silicon film (T_{si}), and oxide thickness (T_{ox}) play important role in optimal characteristics design for DG MOSFETs. Unfortunately, geometric effect on electrical characteristics for ultrasmall nanoscale DG MOSFET devices has never been studied in these years. By considering quantum correction transport model [2], we for the first time explore the important geometric effect on the physical properties for relatively small DG MOSFETs under different bias conditions and dimensions.

Figure 1 shows the Id-Vg transfer curves for the 10 nm thicken silicon channel film device. It is found that the threshold voltage is slightly reduced when the drain bias is increased. Though the threshold voltage is slight decreased in the 10 nm thicken device, the 20 nm and 30 nm thicken devices have much larger threshold voltage lowering effects as shown in Figs. 2 and 3. Moreover, the off state current of the thicker channel devices are much higher than that of the thin channel one. Those drawbacks are mainly caused from the fact that the thicker the channel films the weaker the controllability of gate electrodes. Owing to the inefficient gate controllability, the thicker channel devices have a lower channel barrier height, obtain a higher leakage current, and get a worse result for drain induced barrier height lowering (DIBL) effects. Other than the off state current and threshold voltage lowering, the on state current should be another important factor for novel devices operations. That is, the greater the on state current the higher the operation frequency. Figure 4 presents the on state current difference between the three devices. It has to address that the thicker the channel films the higher the on state current. Owing to a much worse performance in threshold voltage and off state current, the benefit of the on state current is relatively minor in optimization of the double gates devices.

The threshold voltage roll off effect is shown in the Fig. 5, it is found that the devices with the thicker channel films will suffer a worse roll off in threshold voltage. Additionally, a thinner channel film will result in a higher threshold voltage. Those good characteristics will improve the scalability in nanodevices. The DIBL effects are also presented in the Fig. 6 that the thicker channel film devices have a higher DIBL effect. Therefore, in reducing the effect, the thickness of the channel films should be carefully optimized. That is, for a reasonable on state current, the channel film thickness should be keep as thin as possible. We conclude that the film thickness of the double gate devices will strongly affect device characteristics; especially for the considerations of threshold voltage roll off, DIBL, and off state current. Those effects are strongly determined from the controllability of the gate electrodes. In lowering those drawbacks, the film thickness should be kept thin enough.

This work is supported in part by the National Science Council of TAIWAN under contract numbers: NSC – 92 – 2112 – M – 429 – 001, NSC – 92 – 2815 – C – 492 – 001 – E, and NSC – 92 – 2215 – E – 429 - 010. It is also supported in part by the grant of the Ministry of Economic Affairs, Taiwan under contract No. 91-EC-17-A-07-S1-0011.

[1] M. Masahara, T. Matsukawa, K. Ishii, et al., *IEDM Tech. Dig*., p. 949, 2002; B. Yu, L. Chang, S. Ahmed, et al., *IEDM Tech. Dig*., p. 251, 2002; T. Schulz, W. Rosner, E. Landgraf, et al., *Solid-State Electronics*, vol. 46, 2002, 985; S.H. Tang, P. Xuan, J.Bokor, C. Hu, *Proc. IEEE Int. SOI Conf.*, p. 120, 2002.

[2] N. Sano, A. Hiroki, K. Matsuzawa, *IEEE T. Nanotech.*, vol. 1, 2002, 63; S.E. Laux, A. Kumar, M.V. Fischetti, *IEDM. Tech. Dig.*, p. 715, 2002; G. Pei, J. Kedzierski, P. Oldiges, et al., *IEEE T. Elec. Dev.*, vol. 49, 2002, 1411; J. G. Fossum, L.Ge, M.H. Chiang, *IEEE T. Elec. Dev.*, vol. 49, 2002, 808; M. Mouis, F.-N. Genin, and A. Poncet, *Proc. Device Res. Conf.*, p. 195, 2001; F. Stern and W. E. Howard, *Phys. Rev*., vol. 163, 1967, 816; C. Fiegna and A. Abramo, *Proc. IEEE SISPAD*, p. 93, 1997; Y. Li, T.-S. Chao, and S. M. Sze, *Int. J. Modelling & Simulation*, vol. 23, 2003, 94; T.-w. Tang and Y. Li, *IEEE T. Nanotech.*, vol. 1, 2002, 243; Y. Li, T.-w. Tang, and X. Wang, *IEEE T. Nanotech.*, vol. 1, 2002, 238; M. Ogawa, H. Tsuchiya, and T. Miyoshi, *IEICE Trans. Electronics*, vol. E86-C, 2003, 363; Y.-K. Choi, D. Ha, T.-J. King, and J. Bokor, *Jpn. J. Appl. Phys*., vol. 42, 2003, 2073.

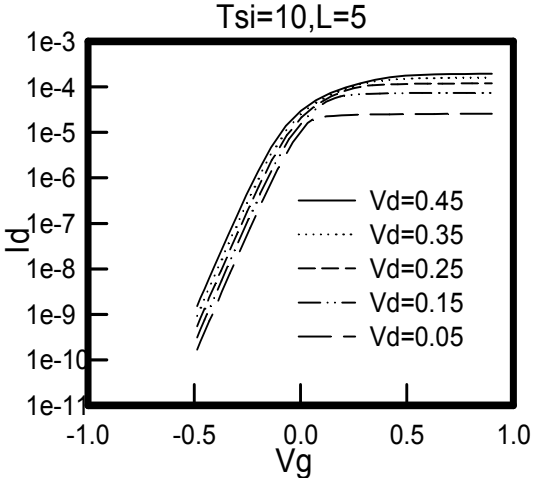

Fig. 1. Id-Vg transfer curves for the device with a 10 nm silicon film.

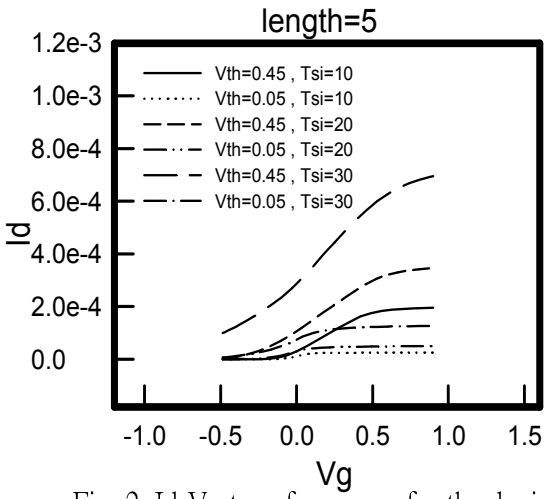

Fig. 2. Id-Vg transfer curves for the device with a 20 nm silicon film.

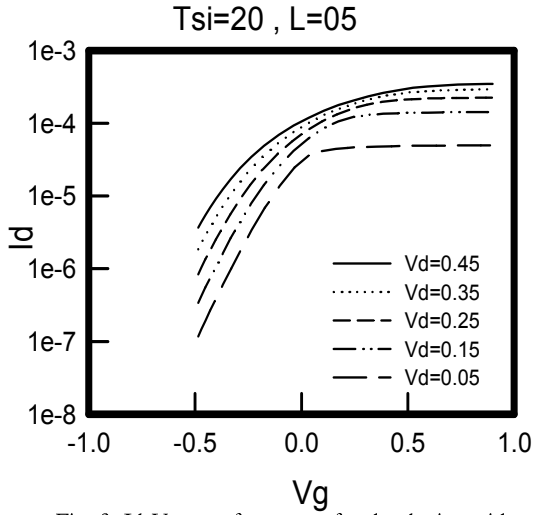

Fig. 3. Id-Vg transfer curves for the device with a 30 nm silicon film.

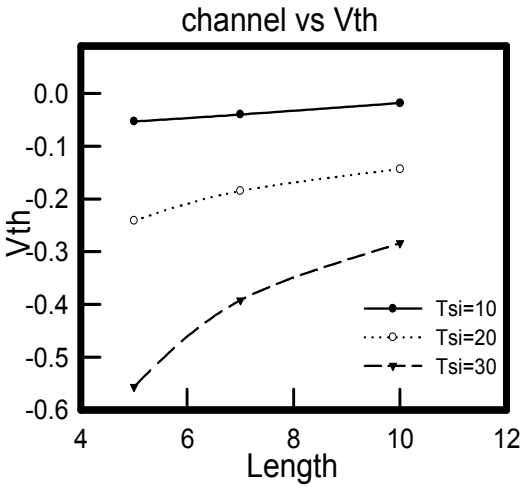

Fig. 4. The on state current difference between the three devices.

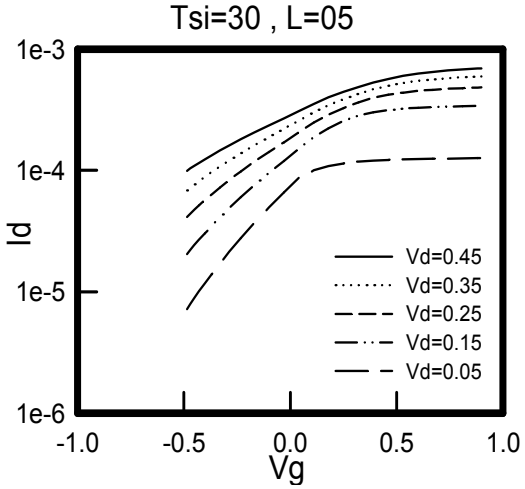

Fig. 5. The threshold voltage roll off effect for different silicon films.

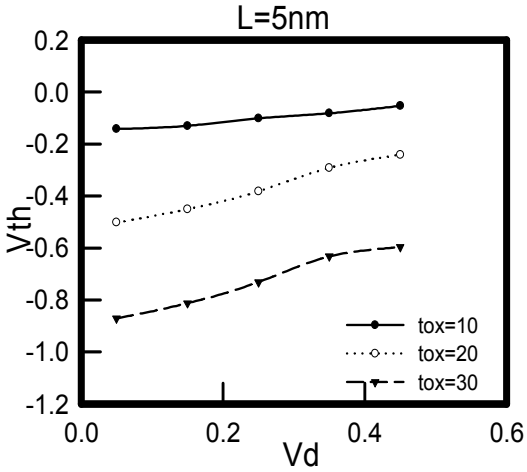

Fig. 6. The DIBL effects for different oxide thickness.