Low-Power CMOS SRAMs with Current-Mode Techniques

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Abstract: - This paper describes two techniques for high-speed low-power SRAM's: a current-mode sense amplifier and a current-mode write driver. The sensing speed and write pulse width are insensitive to the bit-line and data-line capacitances and a separated positive feedback technique is used to enable the circuit to operate at high-speed and low-power. These techniques always keep the voltage swing of the bit-line and data-line quite small. Based on current-mode operation, a memory cell that operates at low-power current-mode is developed. The memory cell has almost equally sized access and inverter transistors, which can be toggled using a small differential bit-line voltage. An experimental 32Kx8 CMOS SRAM with a 9ns access time at a supply voltage of 3V, using 0.35um 1P2M CMOS logic technology is described to evaluate the new current-mode techniques. The active current is 28mA at 100MHz and 25℃.

Key-Words: - current-mode; sense amplifier; write driver; CMOS; SRAM; flip-flop

1 Introduction

Since hand-held products become increasingly popular, low-power system design needs to consider power consumption reduction for battery-operated devices. Therefore, low-power SRAM becomes more and more important for data storage in mobile phone, notebook PC, personal digital assistants (PDA) .. etc. As the memory density increases, the power dissipation and the associated parasitic are inevitably increased. Hence, the large bit-line and data-line capacitances constitute a major bottleneck in achieving higher sensing speed and shorter writing time.

During the reading access cycle, the sense amplifier is one the most critical element of memory circuit. The conventional sense amplifier is based on the voltage-mode technique, but its sensing time increases as the bit-line capacitance increases and its AC operation power consumption is very large. Several design techniques have been proposed to reduce the power dissipation of static RAM [1] in the past. On the other hand, several current-mode sensing circuits [2-4] have been proposed to overcome the problem of possible speed degradation due to large bit-line or data-line capacitances. The power consumption of writing data into memory always dominates for large percentage of whole chip during the writing cycle. In the past, voltage-mode writing circuit was used. Using this mechanism, the voltage swing at the bit-line always needs almost full supply voltage swing. Therefore, the dynamic power consumption at the bit-line will increase as large as voltage swing at the bit-line variation. The current-mode technique for write operation [5] had been proposed to reduce the large voltage swing at the bit-line. However, this method increases the transistor number in a memory cell resulting large memory size.

In this paper, the current-mode techniques for read and write operation of CMOS SRAMs are proposed. Due to current-mode operation, the voltage swing at the bit-line and data-line can be kept quite small all the time. It also reduces active power consumption and reduces chip size of high-density SRAM's. This circuit enables the smallest column current without increasing the block division. Due to the less block division, the memory core can be made to be smaller than with conventional divided word-line (DWL) structure [6]. For low power operation, we present an approach to SRAM cell operation. The cell can be written to with low bit-line voltage swing, thereby significantly reducing the power required to write.

The concept of the current-mode operation is described in Section 2. The proposed current-mode sense amplifier and write driver are described in Section 3 and Section 4, respectively. In Section 5, the memory cell for low power operation is discussed. The design and performance of the experimental 32Kx8 SRAM using these techniques are presented in Section 6. Conclusions will be given in the last section.

2 Concept of the current-mode operation

Power consumption in SRAMs, for a normal operation cycle, is given by

$$Power = Vdd \times Idd \quad (1)$$

$$Idd = (mI_{act}\Delta t + C_{PT}V_{INT})f + I_{SC} \quad (2)$$

where, Vdd is an external supply voltage, Idd is the total current, m is the number of columns, I_{act} is the effective active current, Δt is the word line activation time, V_{INT} is an internal supply voltage, C_{PT} is the total capacitance of the peripheral circuits, I_{SC} is the total static current and f is the operation frequency. This equation is based on the fact that in SRAMs, holding current is very small [1] and decoder charging current is negligible because of NAND decoders [1,7]. To reduce the total power consumption, active current should be reduced as it dominates the total current. Active current is the current that flows during word line activation, i.e., during charging or discharging of bit-line capacitance. This active current is directly proportional to bit-line capacitance and voltage swing. Divided word line and hierarchical word decoding [8] approaches reduce the Idd by reducing the value of m, i.e., the number of columns activated during the operation cycle. Approaches involving the pulse operation of word line and column circuitry reduce the Idd by reducing the value of Δt in (2). In contrast, the approach presented in this paper reduces Idd by reducing the active current, I_{act} in (2).

The total effective charging current flowing through a bit-line, during the operation, can be expressed as

$$I_{eff} = C_{eff} \times \frac{\Delta V}{\Delta t} \quad (3)$$

where C_{eff} is the effective bit-line capacitance and ΔV is the voltage swing on the bit-line.

Similarly, expression for power can be written as,

$$Power = (I_{eff} \times V \times \Delta t) \times f \quad (4)$$

$$= (C_{eff} \times \Delta V \times V) \times f \quad (5)$$

To reduce the power consumption, the capacitance of bit-line or voltage swing should be reduced. However, conventional read/write circuits are based on voltage-mode techniques, which are sensitive to parasitic capacitance. In this paper, we propose the new current-mode read/write circuits, which are insensitive to both bit-line and data-line capacitance. Voltage swing can be reduced by the current-mode techniques, since charging and discharging of the bit-lines and data-lines are not required.

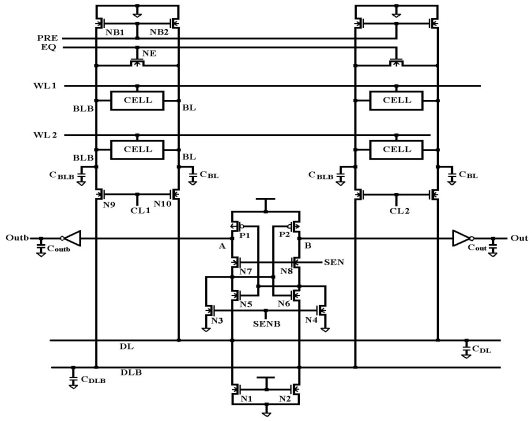

Fig. 1 A current-mode sense amplifier and a simplified data path circuit

3 Current-mode sense amplifier

3.1 Circuit description and operation

Fig. 1 presents the read data path of an n-type separated flip-flop current-mode sense amplifier. The N5-N6 and P1-P2 are made in a manner similar to positive feedback latches. N1 and N2 connect the input nodes and pull down the data-lines close to the ground level. The transistors N7 and N8 are the separating transistors, and the transistors N3 and N4 are the equalization transistors. The bit-line and data-line capacitances are represented by C_{BL} and C_{DL}, respectively, and WL and CL are the word-line and column-line selector signals, respectively. The inputs to the current-mode cross-coupled latch are at the sources of the transistors N5 and N6. The low impedance at the input nodes causes the current signals at the data-lines to be injected into the cross-coupled latch without charging or discharging the data-line capacitances. Hence, the sensing speed is insensitive to both the bit-line and the data-line capacitances.

When the sense amplifier is in the standby state, the signal "SENB" is at high-level and the signal "SEN" is at low-level. Under this condition, N3 and N4 are on, so they pull down the drains of the N5 and N6 to low-level. Hence, N5 and N6 are in the cut-off state, and P1 and P2 operate in the linear region, since their gate voltages are at low-level. The "SEN" is at low-level, so N7 and N8 are in the cut-off state, therefore, no current flows through N7 and N8. At the time, the voltage at the output nodes of the sense amplifier (node A and node B) are equal to the power

supply voltage, the input nodes are at zero volts, and the latch nodes (the drains of N5 and N6) are discharged to low-level. Hence, in the standby state, no DC current flows in the sense amplifier.

During the read operation, both WL and CL lines are activated. The "SENB" is at low-level, and so turns off N3 and N4, and the "SEN" is at high-level turning on the separated flip-flop. When a particular memory cell is accessed, a differential current signal appears at the DL and DLB of the common data-lines. N5 has a lower V_{GS} than N6, so the voltage at node A exceeds the voltage at node B. Moreover, the amplifier with cross-coupled configuration implies that the source to gate voltage of P2 is less than that of P1. The current that flows into node A will therefore be much higher than the current that flows into node B. The voltage at node A then increases further and the voltage at node B decreases. The separated flip-flop is a positive feedback loop, which regenerates the voltage to full swing and latches the voltage, and the response time of the flip-flop is very short, since the capacitance of the output node is very small.

3.2 Simulation results and comparisons

Extensive circuit simulations, using HSPICE, were performed to confirm the operation of circuit and characterize its performance. The simulation results are based on rise and fall times of 1ns. The simulated waveform during the read operation is shown in Fig. 2. The voltage differences at the bit-lines and data-lines are indeed very small (about 50mV) and close to the ground level, thus reducing the power dissipation. The positive feedback effect of the proposed current-mode sense amplifier very rapidly amplifies the differential voltage between nodes A and B to the CMOS logic level.

The performance of the proposed circuit is evaluated and compared with that of the hybrid current-mode sense amplifier [2] and the cross-coupled current-mirror sense amplifier [4] based on 3V 0.35um technology. The simulations were carried out on the proposed current sense amplifier circuit, by sizing the transistor compared to the previous circuits. Fig. 3 shows the effect of bit-line capacitances on both sensing delay and average power consumption at a frequency of 100 MHz and data-line capacitances of 1pF. Here, the sensing delay is the interval between the time when a word line becomes high and the time when the memory cell data is read and amplified to the CMOS level. All the circuits are insensitive to the bit-line capacitances, but the proposed circuit senses more quickly. The power consumption is determined from the current drawn by the read data path circuit. The

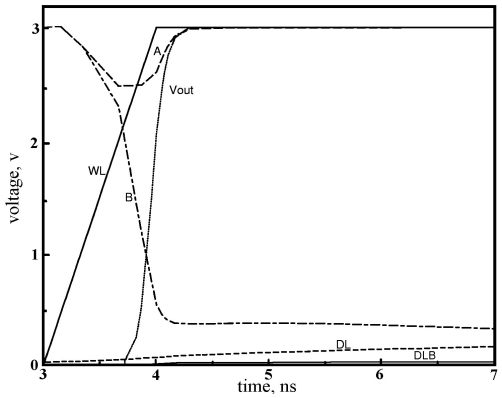

Fig. 2 Simulated waveforms of the new current-sensing data path circuit

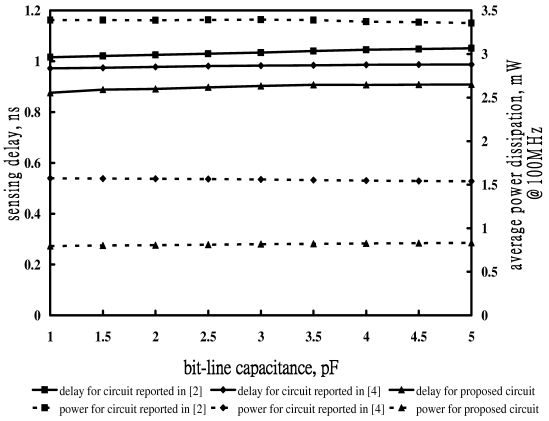

Fig. 3 Sensing delay and average power dissipation versus bit-lines capacitance

average power consumption of the proposed circuit, during a read operation, is also less than that of the circuits in [2] and [4]. Before the read operation, the sense amplifier is in the standby state, and the transistors of the flip-flop in [2] and [4] are all turned on, increasing power dissipation. However, N7 and N8 of the proposed sense amplifier isolate the flip-flop, so no DC current path exists.

Fig. 4 shows sensing delay and power consumption against the data-line capacitances at bit-line capacitances of 1pF. Unlike that of the circuit described in [4], the sensing delay of the proposed circuit hardly changes as the data-line capacitance increases. The proposed circuit also provides the advantages of faster sensing and lower power dissipation. The improvements in speed and power of the proposed circuit are even greater at higher data-line capacitances. In the case in which C_L has a capacitive load of 0.1pF with C_{BL}=1pF, C_{DL}=5pF, the average power consumption of the proposed circuit is 319% and 127% lower than that of the circuits described in [2] and [4], respectively, and the sensing

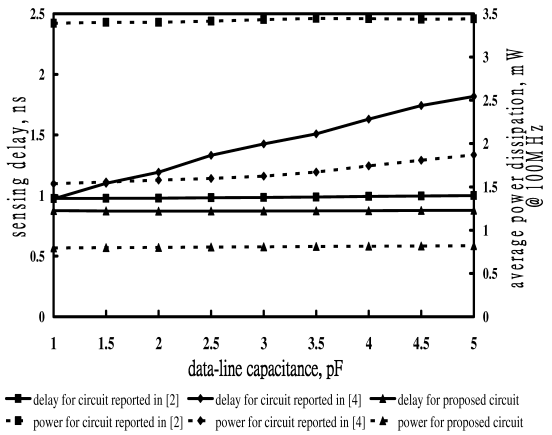

Fig. 4 Sensing delay and average power dissipation versus data-lines capacitance

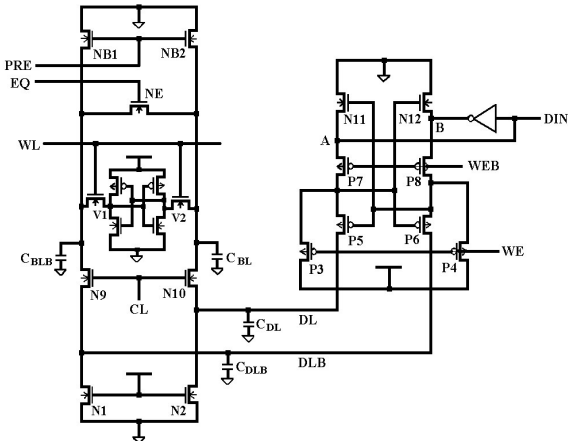

Fig. 5 A current-mode write driver and a simplified data path circuit

speed of the proposed circuit is 13% and 107% faster than that of the circuits reported in [2] and [4]. Hence, the proposed circuit is very suitable for use in high-speed, low-power and high-density SRAMs.

4 Current-mode write driver

4.1 Circuit description and operation

Conventional writing operations need a nearly full supply-voltage swing at the bit-line to overwrite the original cell data during the writing access cycle. However, the bit-line voltage swing dominates the power dissipation during dynamic operation. Hence, the reduction of the bit-line voltage swing at the writing access cycle can reduce the dynamic dissipation of power.

Fig. 5 shows the write data path of a p-type separated flip-flop current-mode write driver. The characteristics of this proposed write driver are quite similar to those of the n-type separated flip-flop current-mode sense amplifier, so no DC current flows in the standby state. During the write operation, as the full swing voltage is applied to the input nodes of the write driver, the separated transistors transport the current to the data-lines. In the new writing mechanism, the bit-line and data-line are precharged to the ground level. Assume that node V1 is at high-level and the node V2 is at low-level. When the word line is turned on, the equalizing transistor remains on, seemingly acting as an extra transistor that equalizes the V1 and V2. This charge redistribution mechanism brings V1 and V2 close to each other since the bit-line capacitance is always much larger than the capacitances of node V1 and V2. At that time, the equalizing transistor is turned off and the column switch is turned on, and the data is driven into the data-line from the write driver. Since

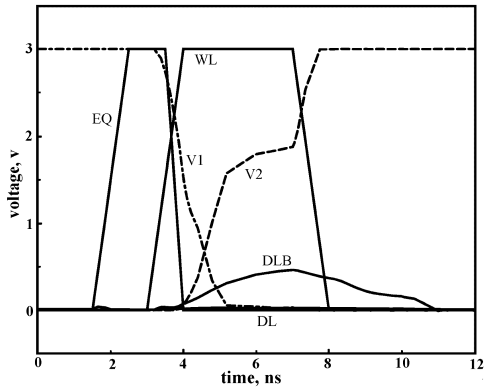

Fig. 6 Simulated waveforms of the new current-writing data path circuit

the voltages of V1 and V2 are close to each other, although the bit-line swing is still very small, the small differential current in the data-line can change the state of the memory cell. The new write driver circuit makes the bit-line and data-line swing lower than 500mV, thus the power dissipation is much less than that of the conventional voltage-mode write driver.

4.2 Simulation results and comparisons

Fig. 6 shows the simulated waveform during the write operation. When the WL and EQ are at high-level, V1 and V2 are close to each other. When the EQ goes low, V1 and V2 change the state rapidly. The proposed current-mode write driver makes the bit-line and data-line swing lower than 500mV, enabling the equalization current of the bit-line and the equalization time to be reduced. Hence, not only the power dissipation is reduced, but also the speed of the writing access cycle is improved.

All three circuits (the conventional input buffer circuit, the circuit described in [5] and the proposed circuit) were simulated together with a simplified

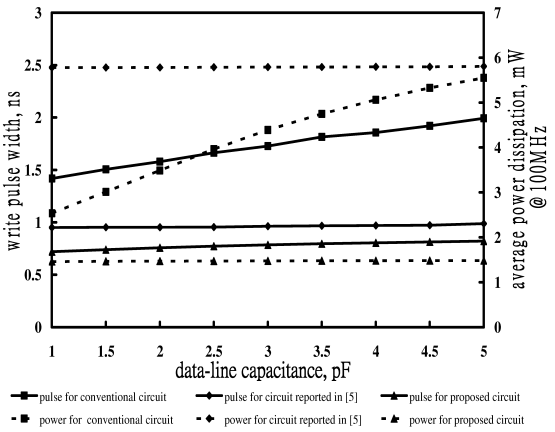

Fig. 7 Write pulse width and average power dissipation versus data-lines capacitance

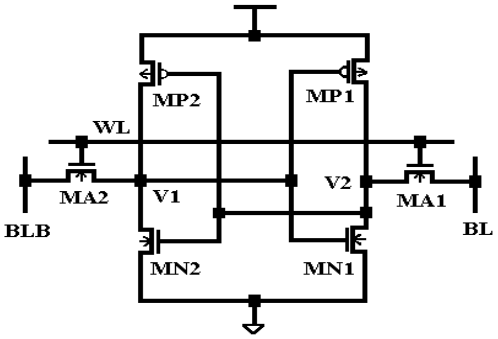

Fig. 8 Schematic of the memory cell

write-cycle-only memory system. They are compared in terms of the write pulse width and average power dissipation with various data-line capacitances at a bit-line capacitance of 1pF, as shown in Fig. 7. Here, the write pulse width means the interval between the time when a word line becomes high and the time when the data is written into memory cell. The figure indicates that the proposed circuit and [5] are independent of the data-line capacitances, and that the conventional voltage-mode input buffer is sensitive to the data-line capacitance. The proposed circuit has the smallest write pulse width. The power dissipation is measured from the current drawn by the write data path circuit. The average power dissipation of the proposed circuit is also less than that of the conventional circuit and the circuit in [5]. For example, at a load (C_L) of 0.1pF, at a frequency of 100MHz, and with C_{BL}= C_{DL}=1pF, the average power dissipation of the proposed circuit is 73% and 295% lower than that of the conventional circuit and that described in [5], and the write pulse width of the proposed circuit is 97% and 32% shorter than that of the conventional circuit and the circuit in [5], respectively. The data-line loading increases with the memory size increases, so the conventional design

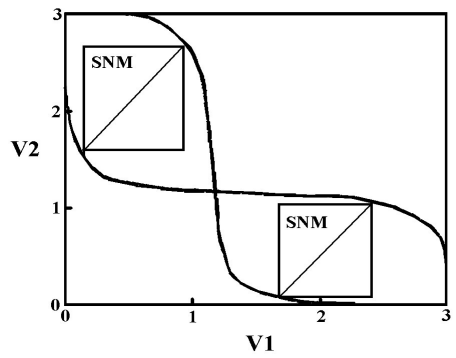

Fig. 9 The static transfer characteristics of the memory cell

always uses a larger input buffer to drive data into the cell. However, the power dissipation of the driver increases with the size of the transistor. For the same buffer, the conventional design can write data into the cell only when the data-line loading is small. As the data-line loading increases, the data driving ability does not suffice. The proposed current-mode write driver can write data into the cell, even though the data-line loading is high.

5 Description and operation of new memory cell

In a conventional SRAM, the bit-line voltage swing during writing must be large, normally at the full CMOS level, to toggle the cell. The reason is that the sufficient noise margin during read is accomplished by using much weaker access than inverter transistors. Instead, this work presents a cell with almost equally sized access and inverter transistors, which can be toggled with a small differential bit-line voltage.

Fig. 8 shows the proposed memory cell, which consists of MA1-MA2, MN1-MN2 and MP1-MP2. The configuration of proposed memory cell is the same as that of the conventional memory cell. Since the bit-line voltage is pulled down to ground, the PMOS transistors in the cell act as driver transistors and the NMOS transistors in the cell work as load transistors. Contrary to the conventional method of operating SRAM cells, in which bit-lines are precharged to high-level, cell stability here depends not on the β_N/β_A ratio, but on the β_P/β_A ratio, which is defined as the cell ratio. The static noise margin (SNM) of an SRAM cell is defined as the minimum dc noise voltage required to change the state of the cell. The SNM of the new memory cell is around 1.0V as shown in Fig. 9.

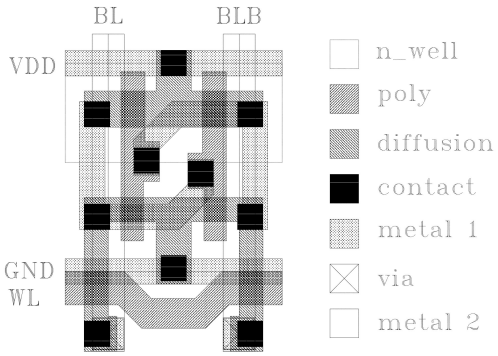

Fig. 10 Layout of the memory cell

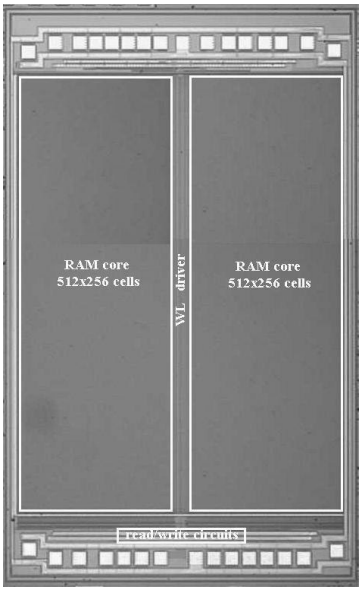

Fig. 11 A photomicrograph of 32Kx8 SRAM

During read operation, node V1 is assumed to be at a low voltage and V2 to be at a high voltage. The low bit-line voltage does not affect V1. The voltage of V2 falls by an amount that depends on the cell ratio. As long as this drop is less than the threshold voltage of the PMOS, the cell is clearly stable, because MP2 will not turn on. During the write operation, the word-line is raised to the high-level. Based on the current-mode write driver, bit-lines are driven to 0V and 0.5V. Despite the low cell ratio, writing can fail if β_N is much stronger than β_A. In the new memory cell, the size of MN is designed using the minimum device size and is almost the same as that of MA, not only making the safe write operation but also reducing the layout area below that of the conventional memory cell. Both read and write operations are performed in the current mode so a small differential current from the cell can be detected by the current-mode sense amplifier, while a sufficiently small differential data current can overwrite the content of the cell.

Table 1 Comparison to conventional SRAM cell

	proposed SRAM cell	conventional SRAM cell
β_P	93 $\mu A/V^2$	46 $\mu A/V^2$
β_N	115 $\mu A/V^2$	327 $\mu A/V^2$
β_A	131 $\mu A/V^2$	131 $\mu A/V^2$
power dissipation (read)	1.2 mW	4.47 mW
power dissipation (write)	1.5 mW	2.88 mW

Fig. 10 shows the layout of the proposed memory cell whose size is 3.9um*5.85um. Table 1 compares this cell to a typical conventional SRAM cell. Both cells are designed using the same standard 0.35um CMOS technology. The conventional cell was operated with precharged high bit-lines, a conventional sense amplifier and a CMOS-level bit-line swing during the write operation to overcome the high cell ratio. The new memory cell was operated as described above with a bit-line swing of no greater than 0.5V. In both cases, the bit-line load was equivalent to 512 cells. The read and write power dissipation given in Table I is the total power consumed by the memory cell, the bit-line precharge, the sense amplifier and the write driver during an operation cycle.

6 Experimental results

A 32Kx8 SRAM chip was designed and fabricated to evaluate the new current-mode techniques. The 32Kx8 SRAM was fabricated using the TSMC 0.35um 1P2M CMOS logic process. Fig. 11 displays a photomicrograph of the fabricated 256Kb SRAM. The SRAM is externally organized as 32Kx8 and internally as two banks that each contains 512 rows and 256 columns. The designed read/write circuit operates in current-mode and the capacitive loading of the data lines only slightly affects performance, so eight read/write circuits are commonly used for the two banks, and located in the bottom region. Fig. 12 shows the measured waveforms of the address input and the data output at 25℃ with a 3V supply voltage. The typical access time is 9ns at an output load capacitance of 30pF and the active current is 28mA at 100MHz. A shmoo plot of the address access time versus power supply

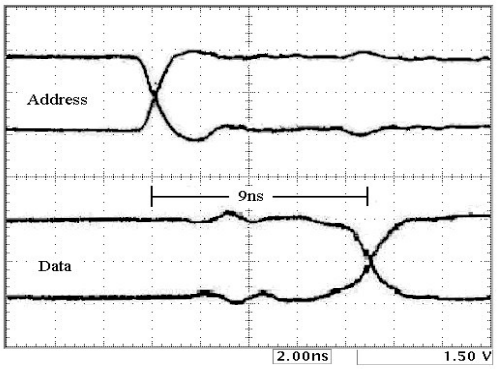

Fig. 12 Typical address and output waveforms

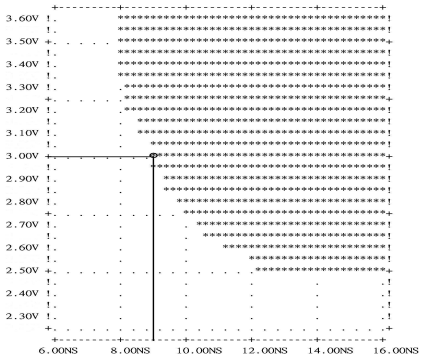

Fig. 13 Shmoo plot of address access time versus power supply voltage

voltage is shown in Fig. 13. The operating voltage ranges from 2.5V to 3.6V. The maximum access time of 9ns was achieved at 3V, the target operating voltage. Table 2 lists the features of the process and the typical characteristics of the SRAM.

7 Conclusions

Current-mode techniques for high-speed low-power SRAM's were described. These presented techniques were demonstrated to be useful by evaluating an experimental 32Kx8 SRAM chip using 0.35um process technology. Based on new current-mode techniques for read and write operation, the sensing speed and the write pulse width are insensitive to the bit-line capacitances. The average power consumption of the proposed circuits is lower than that of the conventional circuits. A new SRAM cell operation mode, with significantly reduced power consumption and layout area but with a good maintained speed, is demonstrated. The SRAM has a low power dissipation of 84mW at 100MHz under typical conditions. The typical access time is 9ns at a supply voltage of 3V and an output load capacitance of 30pF. The new current-mode techniques are suitable for realizing high-speed and low-power SRAM's.

Table 2 Process and SRAM characteristics

Technology	0.35um 1P2M CMOS Logic Process
Gate length	0.35um
Gate oxide	7.5nm
Configuration	32Kbx8
Cell size	3.9x5.85 um^2
Chip size	2.38x3.76 mm^2
Supply voltage	3V
Address access time	9ns (30pF, 3V)
Active current	28mA (100MHz, 25°C)

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