The Low Trigger Voltage and Low Capacitance ESD Protection Device For High Frequency Application

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Abstract

Using the asymmetric source/drain GGNMOS to minimize the device capacitance increasing, a SCR-based low-trigger voltage and low-capacitance ESD protection device (LVCESD) was developed successfully. Combining the secondary ESD protection device and resistor, the LVCESD can effectively protect the thin oxide (19Å) for RF input and I/O pads.

I. Introduction

Electrostatic discharge (ESD) had became the major challenge at high frequencies since the inclusion of the ESD device in the design would affect the high frequency pad performance adversely. Under normal operation condition, the protection device is acted as a passive loading (capacitor series a resistor). Thus, it will increase the noise, cause the signal reflection, and reduce the power transfer between the signal pin and the core circuit. The SCR had became a important device for high frequency ESD protection since the ESD performance of the SCR is much better than the grounded-gate NMOS (GGNMOS) and the N-Well to P-Well junction capacitance is much smaller than the N+ to P-Well junction capacitance. There are two SCR-based ESD protection devices (Fig. 1) had been introduced to protect the high-frequency pad [1] by using 0.18um CMOS process. One is the LCESD that pad does not connect the GGNMOS drains (A1 and A2 in Fig. 1), and one is the ESCR NMOS that pad connects the GGNMOS drains (A1 and A2 in Fig. 1). The parasitic capacitance of the LCESD is 50fF and had been putted in the products (2GHz-5GHz) to protect the radio-frequency (RF) input pads that are designed by 3.3V devices with gate-oxide thickness of 70Å. Containing the LCESD, the products had been proven that could sustain 1.5KV HBM zapping events (+ESD/Vs., -ESD/Vss, +ESD/Vcc and –ESD/Vcc).

Currently, the circuits for high frequency applications, including the first stage of the input and I/O buffers, are all designed by the core devices. However, the trigger voltage of the LCESD is too high (~10V in Fig. 2) to protect the oxide of the core device. The solution to reduce the SCR trigger voltage is using LVTSCR [2] that pad connects to a GGNMOS drain. Although using the GGNMOS as the trigger source can reduce the SCR trigger voltage (ESCR NMOS in Fig. 2), it also causes the device capacitance increasing significantly. In this work, a low-trigger voltage and low-capacitance ESD protection device (LVCESD) was developed successful. The LVCESD using 130nm technology has the low trigger voltage (~4.5V) and low junction capacitance (<100fF).

As the technology shrunk to nano-meter, the core-power had decreased below 1.2V. For a typical SCR device, the hold voltage is higher than core Vcc (1.2V). Thus, using the SCR as the ESD protection device becomes no latch-up risk in nano-meter technologies. The SCR can be used as the primary ESD protection device for output pads and input pads. For most high frequency applications, it is impossible to use the silicide block device to design the output transistor since the silicide block will degrade the device performance. It is well known that silicide NMOS is very vulnerable to ESD stress if it does not design the additional ESD protection device to protect the output transistor. However, whether or not the ESD protection device can protect the output transistor depends on what element in the circuit, ESD protection device or output transistor, can dominate the ESD event. If the output transistor turned on firstly, most of ESD current would flow through the output transistor to deteriorate the output transistor. In this work, the methodology, how to integrate the resistor, secondary ESD protection device and LVCESD to prevent the output transistor damage and oxide damage before the ESD protection turned on, is also presented.

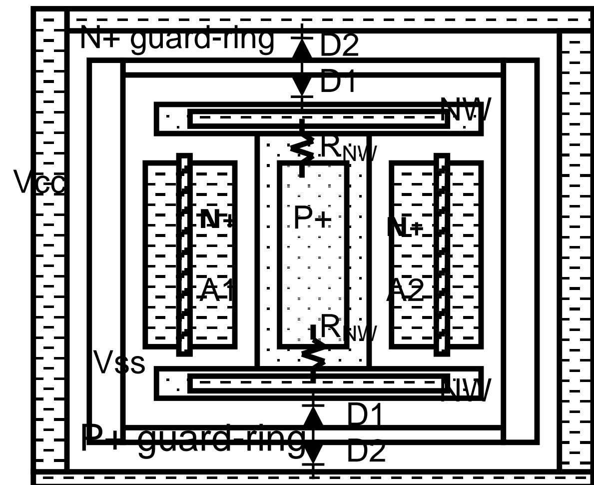

Fig. 1 The top view of the LCESD.

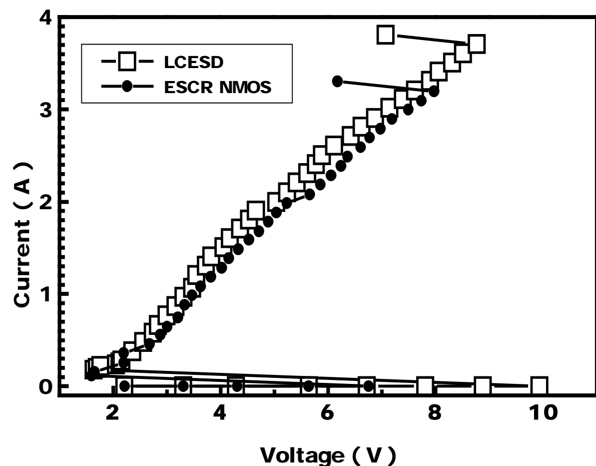

Fig. 2 The high current IV curves of the LCESD and ESCR NMOS under TLP.

II. Experiments

The LVCESD used in the study was fabricated using 130nm technology. The protected devices were 1.2V device with gate-oxide thickness of 19 Å.

A. Test Setup Configuration

The IT-2 measurement was performed on the Barth Transmission-line pulse (TLP) system. It applied a 100nsec current pulse to the device and increases the stress current level continuously until the device fail. The voltage and current waveforms of the device during the current pulse stress are measured simultaneously by the oscillator. And, the voltage and current values before the end of the current pulse 20nsec are recorded. Based on the recorded values in each stress level, the IT2 I-V characteristics of the device is determined. The IT2 value is the maximum current before the device fail. It is determined by the DC leakage current measurement after each stress level not by the transient I-V curve of the device under the TLP. The failure criterion is the device leakage current ≥1uA at Vd 1.2V.

The HBM and MM ESD tests were performed on the Key-Tek ESD tester. A series of 3 positive +ESD/Vss were applied to the test device and the stress voltage level increases continuously until the device fail. After each zapping event, the device leakage current is measured. The failure criterion is the drain leakage current ≥1uA at Vd 1.2V.

B. Device Structure

Fig. 3 shows the top view of the LVCESD and the equivalent elements of the LVCESD under ESD zapping event. The two NW/PW diodes (D1) were used to protect the negative ESD, and the SCR was used to protect the positive ESD. Unlike the LCESD in Fig. 1, the middle N-Well of the LVCESD does not connect to the top N-Well and bottom N-Well. And, there is no left any N+ diffusion in the middle N-Well for the connection. For the LVCESD, there is only a P+ diffusion in the middle N-Well. Thus, the vertical bipolar pnp of the SCR is an open base bipolar. The main purpose of this layout change is to improve the negative ESD performance of the LCESD in Fig.1. Unlike the LCESD in Fig. 1, the P+ diffusion of the LVCESD in Fig. 3 can surround the NW/PW diodes completely since the middle N-Well does not connect to the top N-Well and bottom N-Well. Thus, we expect the current distributions of the NW/PW diodes of the LVCESD in Fig. 3 should be more uniform than that of the LCESD in Fig.1.

It is well known that using GGNMOS as the trigger source can reduce SCR trigger voltage [2]. However, connecting the N+ drain to the pad also causes the device capacitance increasing. Thus, an asymmetric source/drain (S/D) NMOS was proposed to implement a low-trigger voltage and low-capacitance ESD protection device. For the asymmetric S/D NMOS, the drain finger width is much smaller than the source finger width. Using the asymmetric S/D GGNMOS, the device capacitance contributed by the N+ junction can be minimized and the dimension of the SCR can be kept the same.

During ESD zapping event, the GGNMOS drain needs to provide the enough substrate current to trigger the SCR on and can not be damaged by the ESD before the SCR turned on. However, the device ESD performance is proportional to device total width. Thus, it is hard to sustain the ESD stress by using such small width GGNMOS. For preventing the GGNMOS damage, the GGNMOS ESD performance should be enhanced. The layout solution to enhance device ESD performance is using the silicide block to forbid the silicide formation on the drain junction. But even using the silicide block drain, whether or not the GGNMOS can sustain the ESD stress is still unknown. For preventing the GGNMOS damage, the passing current of the GGNMOS should be limited. In CMOS process, the resistor can be used to limit the stress current. The resistor becomes a high resistance resistor to limit the stress current if the stress current is close to the resistor saturation current. Fig. 4 shows two layout splits for this study. One is that pad connects to GGNMOS drain directly (Fig. 4a), and another one is using a silicide block resistor to connect the pad and GGNMOS drain (Fig. 4b).

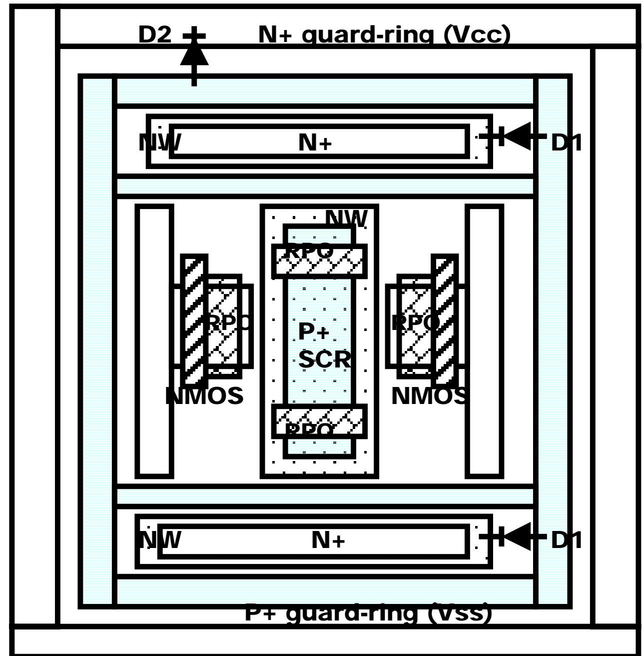

Fig. 3 The top view of the LVCESD.

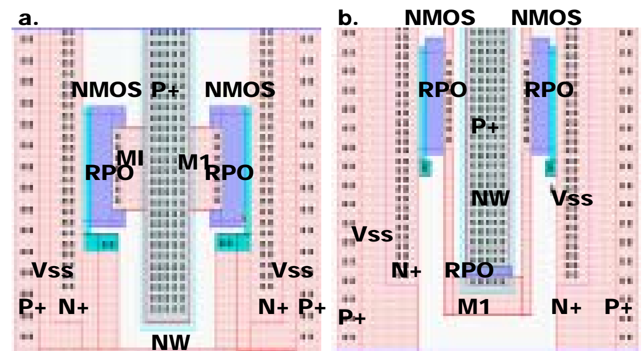

Fig. 4 The GGNMOS connection splits for LVCESD in Fig. 4.

C. ESD Test Results and Analysis

Fig. 5 shows the high current IV curves of the two LVCESD devices (Fig. 4) under the TLP. Table I shows the IT2, HBM passing voltage and MM passing voltage of the two devices in Fig. 4.

Comparing the previous published ESD test results [1], the negative ESD performances of the two LVCESD devices in Fig. 4 are apparently much higher than the LCESD in Fig. 1. The HBM passing voltage can be improved form –2KV to –6KV and the MM passing voltage can be improved from -200V to –400V. Because the layout of the NW/PW diode of the LVCESD in Fig. 3 is symmetric, the current can distribute the LVCESD uniformly. For the LCESD in Fig. 1, however, the current will be localized in the regions nearby the P+ guard-ring since one side of the NW/PW diode is lack of the P+ strap. The effective area for discharging negative ESD of the LVCESD in Fig. 3 is apparently larger than that of the LCESD in Fig. 1. Thus, the two LVCESD devices in Fig. 4 all have the better negative ESD performances than the LCESD in Fig. 1.

From Fig. 5, we can observe that trigger voltages of the two LVCESD devices in Fig. 4 are nearly the same. It implies that adding a small resistor does not cause the device trigger voltage increasing. However, the IT2 and the positive ESD passing voltages of the structure without a resistor (Fig. 4a) is much smaller than the structure with a resistor (Fig. 4b). It implies that the GGNMOS of the LVCESD will dominate the ESD zapping event if the device does not have a resistor to clamp the current to flow into the GGNMOS.

Fig. 6 shows the simulated IV and current flowing lines of the structure without a resistor under 1E-3A/um current stress event. Fig. 6a shows that snapback voltage of the device is only 1.5V. Under the high current stress event (1E-3A/um), we can observe that the current can flow from the P+ diffusion to NMOS source and P-substrate pick-up (Fig. 6b). It implies that SCR had turned on and the device was driven into the latch-up state. For a GGNMOS, the snapback voltage is higher than 3.0V. From this point view, the parasitic npn bipolar of the GGNMOS could not turn on as the LVCESD gone into the latch-up state. However, the P-substrate to N+ source junction was forwarded to result in the N+ source injecting the electrons into the P-substrate when the SCR turned on. And then, these electrons injected from the source would be collected by the high potential regions of the device. In this device, there are two high potential regions. One is the GGNMOS drain, and another one is the P+ diffusion of the SCR. Thus, we can observe that current does not flow through the SCR but also can flow through the GGNMOS drain. From the layout, we see that the space between the GGNMOS drain and GGNMOS source is shorter than the space between the SCR anode and GGNMOS source. Therefore, the electrons are more easily flowing into the GGNMOS drain than flowing into the SCR anode. We can observe that the number of the current-flowing lines in the GGNMOS drain is no less than the number of the current-flowing lines in the SCR anode. Because part of ESD current discharged by the SCR anode and the snapback voltage of the LVCESD in Fig. 4a is smaller than a single GGNMOS, the power dissipated at GGNMOS of the LVCESD should be smaller than that of a single GGNMOS. Thus, the ESD performance of the LVCESD in Fig. 4a is much larger than a single GGNMOS. However, the higher voltage ESD still can damage the GGNMOS if the current is out of the GGNMOS that can dissipate. Thus, the LVCESD in Fig. 4a only can pass 2KV HBM and 100 MM.

To improve the ESD performance of the LVCESD device in Fig. 4a, the current flowing through the GGNMOS should be limited. It is well known that resistor can be used to clamp the stress current. Fig. 7 shows the high current IV curve of a silicide block P+ diffusion resistor (W/L 2/10) under the TLP. Because of the self-heating, the resistor became a high resistance resistor and goes into saturation region as the stress current is close to the resistor saturation current (~19mA). Based on large width GGNMOS test result, the maximum current density of a silicide block GGNMOS is nearly 10mA/um. In Fig. 4, the total width of the GGNMOS is nearly twice of the total width of the silicide block resistor. Thus, the maximum current of the silicide block GGNMOS is nearly a half of the saturation current of the silicide block GGNMOS. Because the saturation current of the resistor is smaller than the GGNMOS maximum current, the stress current of the GGNMOS will be limited below the current that GGNMOS can dissipate. In addition, it would induce an IR drop across the resistor when the current flown through the resistor. From these results, the resistor during the ESD zapping event does not clamp the current to flow through the GGNMOS but also can reduce the voltage drop across the N+ drain of the GGNMOS. Thus, it can reduce the power dissipation at the GGNMOS to decrease the Joule-heating generation induced the device temperature increasing. As the GGNMOS temperature is kept below the thermal run-away turnover point [3], it can prevent the GGNMOS damaged by the ESD. Because the GGNMOS was not damaged by the ESD, the positive ESD performance of the LVCSCR with a resistor (Fig. 4b) is more robust than the LVCSCR without a resistor (Fig. 4a).

Table I :

Stru.	IT2/Vss	+HBM/Vss	-HBM/Vss	+MM/Vss	-MM/Vss
Fig. 4a	1.25A	+2.0KV	-6.0KV	+100V	-400V
Fig. 4b	2.9A	+5.0KV	-6.5KV	+350V	-400V

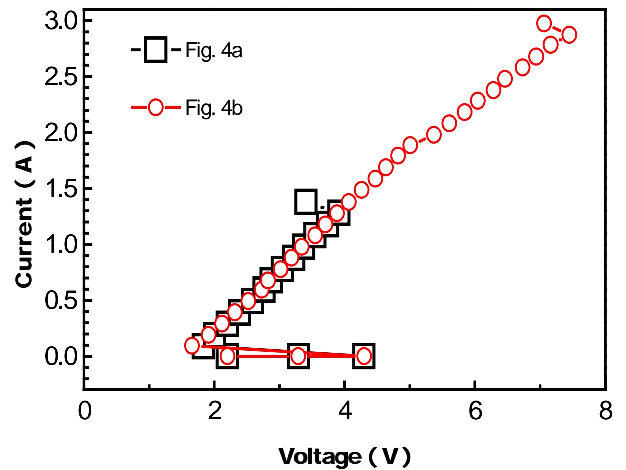

Fig. 5 High current IV curves of the LVCESD devices (Fig. 4) under the TLP.

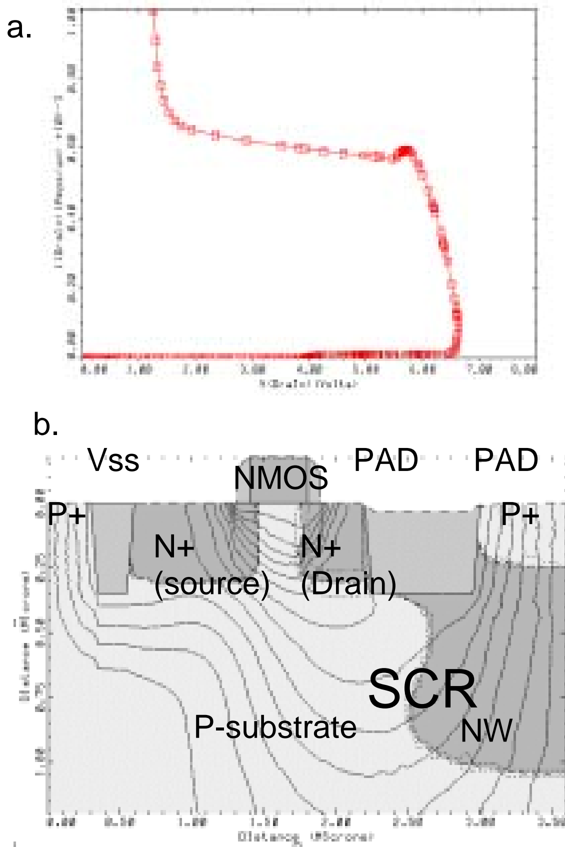

Fig. 6 (a) The simulated IV of the LVCESD in Fig. 4a, (b) The current flowing lines of the LVCESD in Fig. 4a under a 1E-3A/um stress current.

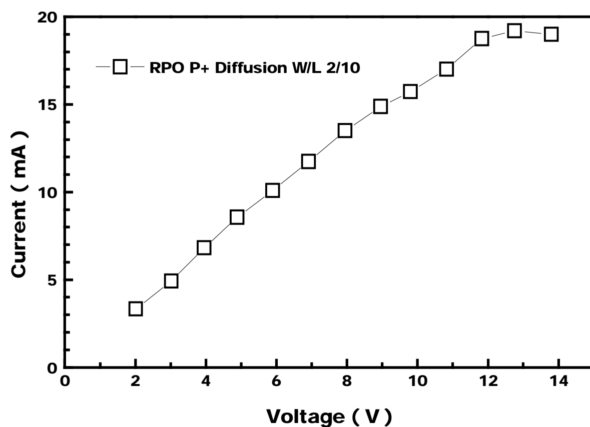

Fig. 7 The high current IV of a silicide block P+ diffusion resistor under the TLP.

D. LVCESD ESD Capability for Input pads and I/O pads

Although the ESD performance of the LVCESD in Fig. 4b is very robust, whether or not the device can protect the gate oxide of the input pad and the transistor of the I/O pad is still unknown. Fig. 8 shows the test structures used for this study. For most RF products, they can not use the silicide block device to design the output transistor. The used transistor N1 (Fig. 8c and Fig. 8d) is a small width pure silicide NMOS. And, the used resistor (Fig. 8b and Fig. 8d) is a small width silicide N+ poly resistor.

Fig. 9 shows the high current IV curves of the structures in Fig. 8. Table II shows the IT2, HBM passing voltage and MM passing voltage of the test structures in Fig. 8. From these results, we find some interest results : 1. Although the trigger voltage had been reduced to 4.5V, the LVCESD still can not effectively protect the thin oxide (19Å) oxide if it does not have a secondary ESD protection device and a resistor, 2. Add a small resistor can improve the device oxide protection capability a little (HBM 1KV and MM50V) since the resistor can clamp the current to flow through the gate oxide, 3. The LVCESD still can not effectively protect the output transistor if the output transistor is the pure silicide device, 4. Adding a small resistor can prevent the output transistor damage if the output transistor is made of the pure silicide NMOS, 5. The LVCESD can effectively protect the thin oxide if it can add a small resistor and secondary ESD protect device between the protected oxide and the new LVCESD.

From these results, we find that resistor and secondary ESD protection device are also very important for ESD protection. Without the two elements, the LVCESD in Fig. 4b still can not effectively protect the protected devices. The main purpose of the resistor is to clamp the current to flow through the secondary ESD protection device (output transistor). The main purpose of the secondary ESD protection device is to clamp the ESD voltage to a safe value in an instant. Thus, whether or not the ESD protection device can work also depends on the resistor and secondary ESD protection device.

Fig. 10 and Fig. 11 shows the high current IV curves of a silicide N+ poly resistor and a silicide GGNMOS under the TLP. From the test results, the maximum current densities for silicide N+ poly resistor and silicide GGNMOS are 30mA/um and 7.2mA/um, respectively. In Fig. 8d, the total width of the secondary ESD protection device is nearly ten times of the total width of the silicide resistor. Thus, the saturation current of the silicide resistor is nearly a half the maximum current of the secondary ESD protection device. During the ESD zapping event, the passing current of the secondary ESD protection device can be limited below the current that secondary ESD protection device can dissipate. Thus, the ESD could not damage the secondary ESD protection device (output transistor) if the LVCESD was not damaged by the ESD. From the result, it provides us a new ESD concept for input and I/O protections. For current input and I/O protections, it often uses a large resistance input resistor (>100Ω) and does not limit the width of the input resistor. However, we found that resistor width is more important than the resistor resistance. Basically, the secondary ESD protection device can effectively protect the thin oxide if it is not damaged by the ESD. But, whether or not the secondary ESD protection device was damaged by the ESD depends on how much current flown through the GGNMOS during ESD zapping event. The criterion to prevent the secondary ESD protection device (output transistor) damaged by the ESD is that maximum current of the secondary ESD protection device should be designed larger than the saturation current of the resistor.

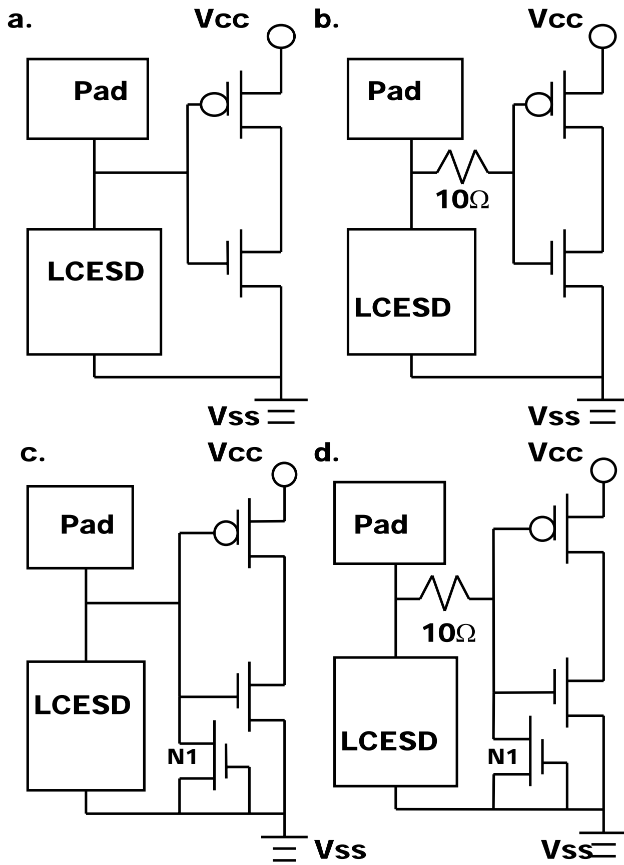

Fig. 8 The test structures for LVCESD protection ESD capability study.

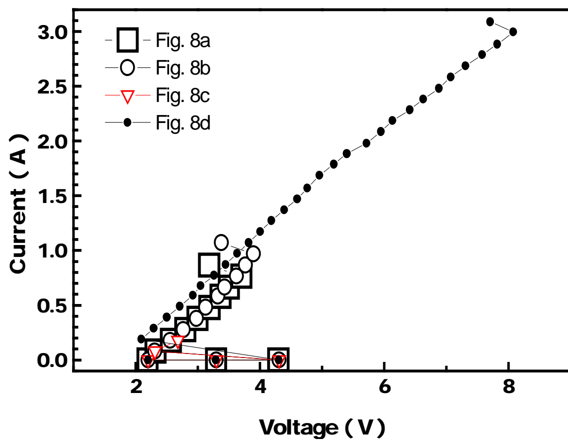

Fig. 9 The high current IV curves of the test structures in Fig. 8.

Table II :

Stru.	IT2/Vss	+HBM/Vss	-HBM/Vss	+MM/Vss	-MM/Vss
Fig. 8a	0.76A	+1.0KV	-6.0KV	+50V	-400V
Fig. 8b	0.968A	+2.5V	-6.0KV	+100V	-400V
Fig. 8c	0.03A	+0.25KV	-6.5KV	+25V	-425V
Fig. 8d	2.99A	+5.5KV	-6.0KV	+400V	-400V

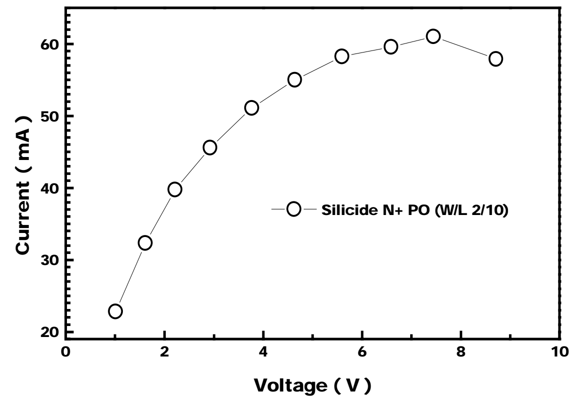

Fig. 10 The high current IV curves of the silicide N+ poly under the TLP.

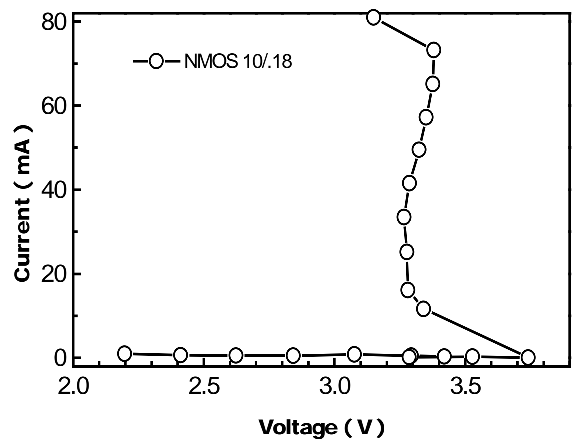

Fig. 11 The high current IV curves of the silicide 1.2V GGNMOS under the TLP.

III. Conclusion

Combining a resistor and the secondary ESD protection device, the LVCESD can effectively protect the thin oxide (19Å) and output transistor. The criterion to design the secondary ESD protection device and the resistor is that the maximum current of the secondary ESD protection device should be designed larger than the saturation current of the resistor. The saturation current of the resistor and the maximum current of the secondary ESD protection device can be evaluated from the TLP measurement.

Reference :

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