Design and Implementation of a dual mode digital APC Algorithm for an APON burst-mode Laser driver

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Abstract: - A dual mode digital Automatic Power Control (APC) circuit was designed and integrated in a burst-mode laser driver for 155Mb/s APON applications. The chip can drive most commercially available FSAN compliant laser diodes in almost any circumstances. The optical output power of the laser transmitter can be regulated within 2.6µs after a power up or a first connection to the network, which is unprecedented among competitors. This paper illustrates the digital control algorithm and its implementation, focusing on the high-speed and low-power constraints present. Finally, high performance is demonstrated by experimental results.

Key-Words: - PON, access network, laser driver, Dual mode APC algorithm

1 Introduction
In the continuing endeavor towards broadband network access, FTTx (Fiber-To-The-Cabinet/Building/Business/Home) is an effective solution to enable new multi-media services such as interactive video, voice, image, audio and fast internet. A suitable technology for offering a mixture of distributive and interactive services to a large number of subscribers, with guaranteed QoS (Quality of Service), is the Passive Optical Network (PON). It implements a very high bit-rate continuous downlink, and a burst-mode uplink, on a passive star fiber plant [1].

The burst-mode transmitter located in the subscriber ONT (Optical Network Termination) is a key building block of a PON system [2]. The design concept should be simple, and optimized for low cost, low power consumption, and high reliability. The performance requirements are high, and the functionality is substantially more complex than usual, due to the bursty nature of the operation. The burst-mode behavior and multiple upstream access require fast power level stabilization within the short time slots allocated to a specific subscriber. No upstream data communication is possible unless the transmitter level stabilization and ONT ranging (propagation delay measurement) have been performed. A burst-mode transmitter must not send upstream light in timing windows allocated to other ONT's, as this would disturb the upstream traffic of operational services. As the OLT (Optical Line Termination) cannot perform a proper ranging on an unleveled ONT, the system must reserve long upstream time windows for leveling an ONT after power up or first connection to the network. So the time needed to level a burst-mode transmitter must be restricted to an absolute minimum.

During ONT startup a fast regulation algorithm levels the optical power as fast as possible to the
target value. During ONT operation (data traffic) a slow fine-tuning occurs, compensating for temperature changes.

2 Chip Architecture

Fig. 2 shows the block diagram of the burst-mode transmitter. Apart from the actual laser driver, most circuitry on the chip is related to the Automatic Power Control (APC) mechanism. The bit stream and cell envelope both pass through an 18-bit digital delayline before being sent to the actual laser driver. This is a 12 bit programmable current source that can drive up to 120mA with a resolution of 0.5mA. The laser current is controlled by the digital algorithm core, optimized to bring both the high (bit 1) as the low (bit 0) laser current towards a correct optical setting in the least possible number of subsequent adaptations (regulations).

One regulation includes the following steps: the bit pattern is monitored [4] to detect a long series of consecutive 1’s or 0’s. While this series passes through the laser, a reference current for the "1" or "0" setting is subtracted from the back facet photocurrent and the result is integrated over the back facet capacitance [3].

This builds up a positive or negative error voltage, the polarity and growth rate of which is detected and passed to the digital algorithm core. Finally an intelligent algorithm adapts the laser current. After approximately 15 regulations (worst case) both low and high laser current are regulated to less than ±3 and ±1 dB (electrical) of the target value respectively. See Fig. 3 for an overview of the control loop mechanism.

This mechanism involves two digitally programmable current references, a high-gain low-offset voltage amplifier chain and accompanying comparators. After each regulation the back facet capacitance is reset to a default value by a voltage reference and a reset switch. When both "1" and "0" - optical level are found to be close enough to the target level, an interrupt signal (Level_OK) is generated to an external ASIC.

The external digital ASIC can access ample control and configuration registers through a generic SPI-interface high speed data and configuration registers through a generic SPI-interface high speed data and configuration registers through a generic SPI-interface high speed data and configuration registers through a generic SPI-

3 Pattern Detection

The number of consecutive bits required for a single regulation cycle is calculated using the maximum allowed optical power error, the back facet capacitance and responsivity and the amplifier characteristics.

During fast regulation, when the optical power error is big, the error voltage on the back facet capacitance will build up faster, so first only 4 consecutive bits are looked for, afterwards 6, 8, 10 and finally 12. "0" - regulation starts at 6 consecutive bits, followed by 8, 10, 12, 14 and 16. So the pattern length being searched for is dynamically adapted by the algorithm to improve speed and accuracy. During fine regulation, the integration can last up to 31 bits, to fine-tune the laser setting to a much more precise setting value, and to track temperature shifts.

The pattern detection block monitors the bits inside the delay lines and triggers a regulation when a useful pattern is detected. Thus, no external time-critical control signals are required to initiate a regulation cycle. This simplifies the interface with the ASIC providing data and clock signals, and makes the chip more autonomous and easier to test.

Finally, the ability to regulate power by detecting the valid pattern (consecutive 1’s or 0’s) keeps the door open to packet based transmission, where the
chunks of data sent by a user have a size much bigger than 56 bytes, increasing the importance of tracking the output power variations inside a burst. The occurrence of the necessary bit patterns is guaranteed through the PLOAM - cells (Physical Layer Operations, Administration & Maintenance), which contain a dedicated Laser Control Field (LCF). During ONT ranging at chip start-up a series of PLOAM - cells are sent, guaranteeing the occurrence of the patterns needed for fast initialization. During ONT operation (slow regulation) the majority of cells are data cells, in which the patterns are guaranteed statistically. Moreover, PLOAM - cells are sent at least once every 105 ms, enough to track the temperature effects the slow regulation is meant for.

It was studied whether the probability of a useful "1"-level pattern (11...11) can be increased by allowing some intermediate zeros (e.g. 1011..11). If the "0" optical level is almost correct, the "0" - back facet current is much smaller than the "1" - back facet current, and would hardly interfere in the "1"-regulation measurement. Unfortunately, this was found unfeasible, because the reference current drivers cannot be switched at data speed (transient effects due to high back facet capacitance).

4 The Algorithm
The algorithm block is responsible for generating the laser driver setting. Overall speed is optimized by making a trade-off between minimizing the number of regulations (by making the algorithm more intelligent), and minimizing the calculation time needed for each regulation.

4.1 Parameter Estimation Algorithms
If one would know the exact relationship between the digital laser driver setting and the photodiode current, measuring the photo current would allow to accurately change the laser current and thus quickly regulate the optical power.

The problem in this approach is the large number of uncertainties in the regulation loop (see Fig.3). The laser characteristic is non-linear, determined by two dominant parameters (threshold current and slope efficiency). This results in two loop constants that need to be estimated. Both are temperature dependent. Back facet capacitance and responsivity are not precisely known and can vary over a large range. The laser driver current is dependent on temperature, supply voltage and chip technology corners.

Asking the user to provide these parameters would make the chip difficult to use. Moreover, the two loop constants can only be calculated when all the parameters are known, so if even only one is unknown or difficult to specify, this regulation approach cannot work.

Another approach involves driving the laser driver with specific, alternating bit patterns, and then measuring the back facet current. Two of such measurements allow the loop constants to be estimated. However, the calculations performed in the digital block would be complicated and the resulting loop constant estimations poor, especially when the optical power error is very big or very small. The overall quality of the search algorithm would be bad: laser setting overshoots, ringing and possible instability. All previous issues have a negative effect on the regulation speed, which can not be predicted accurately. The complicated arithmetic results in increased die size and power consumption, and it slows down the loop speed significantly.

Performing an accurate measurement of the photocurrent error is useless, since this information cannot be used without knowing the loop parameters. A good algorithm should only use the fact whether the photo current is too high or too low, and expect no other information.

4.2 Adapted binary search algorithm
Using a binary search algorithm has many advantages: the algorithm is stable, predictable, easy to implement and requires little arithmetic. It is very easy to calculate the required number of regulation cycles needed beforehand. The only problem remaining is laser safety: laser diodes could be fatally damaged by exceeding the maximum safe optical output. Moreover, lasers generate light more easily and efficiently at lower temperatures, and it is possible for a laser diode to be ruined by a specific current at low temperatures which is a perfectly normal current at higher temperature. To overcome this, three programmable registers have been provided to store the absolute maximum laser current at low, medium and high temperature. An on-chip thermometer is included to deal with the temperature dependence of the laser driver, and assure safe and reliable operation. The temperature is measured by a PTAT (Proportional To Absolute Temperature) voltage source. This voltage is converted into a 4-bit word to control the laser current.

The algorithm starts its search at a programmable preset current, typically the laser current in use when
the ONT was shut down at a previous session. If the optical power turns out to be too high, a downwards binary search algorithm can be used safely. If the optical power needs to be augmented, a secure linear upwards search is started. The step sizes are $\frac{1}{2}$, $\frac{1}{4}$ or $\frac{1}{8}$ of the laser current, small enough not to harm the laser, but significantly bigger than the step sizes usually implemented in laser drivers. If starting from a preset current (e.g. a current level known from previous laser operation), the linear search typically ends after only 2 upward steps, after which the fast binary search comes in. The step size become smaller when nearing the maximum laser current, and can also be programmed by the user via a programmable register.

A huge benefit of this approach is the ability to estimate very accurately the total time fast regulation will take: for the linear part, 4 regulations in total are estimated: 2 for '0' and 2 for '1' regulation. The binary search will take 5 to 6 steps maximally. At every step of the binary search, we know the laser current setting is somewhere within $I \Delta I$ of the optimal setting, which allows the algorithm to generate a control signal "Level_OK" to signal the near completion of the power leveling. The total number of regulations is estimated somewhere around 15 (worst case).

5 Hardware Implementation

The mixed-mode analog and digital microchip is made on a 4.2 x 4.2 mm die in the Alcatel 0.35µm CMOS process. The digital logic counts ± 20K gates (2.25 mm²). Two external clocks are provided to the chip: the 155MHz data clock used for clocking the digital core, and an asynchronous clock with a variable frequency between 0 and 12 MHz, used to access the register bank via an SPI interface. Also the inverse clocks are used, which means we have at least 4 clock domains.

Clocking all non-SPI digital logic at 155MHz would result in 550mW power consumption for the digital circuitry alone, unacceptable considering the battery backup. Both clock division and clock gating are used to reduce overall power consumption. The power consumed by each sub circuit can be calculated using the formula:

$$\text{PowerFactor} \cdot f_{\text{crit}} \left( \text{FFGC} + \text{CGC} / 2 \right)$$

where FFGC and CGC are the Flip-Flop - Gate Count and the Combinatorial Gate Count. Power Factor is a technology dependent parameter quantifying the mean power consumption per gate per Hertz. Early synthesis results of the RTL code yield accurate estimations of the gate count each digital sub circuit will have. A spreadsheet program performs quick recalculations of the overall power consumption when adding new clock domains or moving circuits from one domain to another. Using this simple approach it was decided to add 2 clock domains: a 26 MHz domain and a gated 155 MHz domain. Circuity in the latter clock domain is clocked differently depending on the three operation modes of the chip: fast regulation mode (which occurs infrequently), slow regulation mode (during most of the information bursts), and outside-burst mode. The algorithm calculation core only works full time during fast regulation. During slow regulation it is only switched on when needed. Outside a burst it is never switched on. This approach allows to divide power consumption of the 8K gates calculation core by 16. The SPI register bank works at 26 MHz, thus dividing the power consumption by a factor 6.

As a result of this study, power consumption could be reduced to 100mW outside a burst, 155mW during a slow regulation burst, and 370mW during fast initialization (only a few µs). A considerable amount of this power is introduced by the extra logic required for signals crossing a clock domain. This logic puts some delay on the signal and consumes power. If two clock domains are derived from the same input clock, tweaking the phase relationship between the two clock domains can resolve setup & hold timing problems.

Anti-metastability structures are used for signals crossing asynchronous clock domains, e.g. the signals passing between the SPI - clock domains and
the clock domains derived from the 155MHz clock, or digital signals coming from analog circuitry.

6 Test Results
Fig. 5 and Fig. 6 show two typical measurements of the optical power controlled by the dual mode APC control algorithm. In Fig. 5 the laser driver is fed with bursts of 17 bytes (5 bytes '1' and 12 bytes '0'), followed by a period of no-signal (the laser is turned off outside bursts). The mechanism shown in figure Fig.4 is applied until both '1' and '0' are almost correct and the Level_OK interrupt pin is asserted. The chip continues coarse power regulation until it is switched to slow regulation mode.

Fig. 6 demonstrates another test case. The initial laser setting for bit “1” is increased twice, until the laser current is too high. Then, a binary search algorithm looks for the correct laser setting between the previous and the current laser driver setting. The initial “0” – setting is too high from the start, so the binary search algorithm is started right away.

7 Conclusion
A dual mode digital APC algorithm with pattern detection has been developed and implemented in a laser driver chip, and has been proven very fast and stable. The algorithm is generic, and the presented 155 Mb/s implementation can be adapted to other burst mode laser transmitters, such as required for Gigabit PON systems.

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References:

