

# Optimal Model Parameters Extraction for Semiconductor Device Simulation with a Genetic Algorithm

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*Abstract:* - In this paper we successfully develop an intelligent parameters extraction and optimal TCAD tool for device and circuit modeling and simulation. This novel approach is based on the monotone iterative method as well as the genetic algorithm to solve a set of nonlinear equations. The approach can be applied to automatically extract model parameters with high accuracy and rapid convergence rate. This novel simulation methodology provides various practical applications in electrical engineering, such as nanodevice I-V characterization, RF circuit optimization, and system on chip functional design. Numerical results for a heterojunction bipolar transistor (HBT) circuit are presented to demonstrate the accuracy, efficiency, and robustness of the method.

*Key Words:* - Genetic Algorithm, Device Model, Circuit Simulation, Monotone Iterative Method, Physical Parameters Extraction, and I-V Curves Characterization

## 1 Introduction

The technology computer aided design (TCAD) provides an alternative tool to analyze the intrinsic and extrinsic electrical behavior of MOSFET structures. It has been of great interests that to model the I-V characteristics of submicron devices with the equivalent circuit approach. However, parameters of the circuit model to be extracted for an optimal design of the device I-V characterization is a time-consuming task. The conventional trial-and-error approach for the parameters extraction can be further improved with our computational intelligence approach.

In recent years, the computational intelligence has been of great interests and has provided an alternative for solving, such as the optimization problems arising from science, engineering, and social science. The evolutionary computation is one of the premier approaches in the field of intelligent computing; it covers a quite wide range in real world applications, such as combinatorial and numerical optimizations, supervised and unsupervised learning, co-evolution and collective behaviors, evolutionary design and evolvable hardware, and molecular and quantum computing, etc. Based on the metaphors from biological evolution, genetic algorithm (GA) is a global optimal strategy, which was first proposed by Holland [1]. In genetic algorithms, all unknowns or

variables to be optimized are represented as genes on a chromosome, so-called "string", and a measure for the optimization is given as a fitness function to the surrounding environment. The optimization is realized by the breeding procedure that mimics sexual reproduction and natural selection. Through generations, strings that survive the natural selection pass their genetic code to their offsprings, while strings poorly fit to the environment evolves to adapt more favorably to the environment, which brings the optimized values for maximizing the fitness function. The genetic algorithm has its random, but additional information exchanging for memory components make it explores the vast solution space intelligently.

The GA is an optimization approach, so it has been of great interests and a wide rang of applications [2-5]. Especially, in microelectronics it has been applied to various aspects in the VLSI design area [6-8]. Examples include cell placement, channel routing, test pattern generation and design for test, and signal processing. However, to the best of our knowledge, so far there is no any GAs applied in the I-V curves optimization and model parameters extraction for submicron semiconductor device and VLSI circuit.

In this paper, we for the first time propose a GA optimization technique for semiconductor device I-V curves characterization and model parameters

extraction in the advanced design and applications of submicron semiconductor device and VLSI circuit. According to a specified circuit equivalent model, the KVL or/and KCL circuit theories, a set of governing ordinary differential equations (ODEs) is formulated and solved for device characteristics systematically. Our approach is to solve such nonlinear equivalent equations to obtain the operation of device or circuit behavior with the proposed monotone iterative (MI) method in our earlier works [9-16]. The computed results are further improved and optimized automatically with a genetic algorithm directly. The proposed GA has a good optimization result in the model parameters extraction when the desired specification or function is prescribed. Some dominate weight parameters among lots numerical parameters can be estimated with this intelligent and robust solution methodology.

This paper is organized as follows. In Sec. 2, we state the device model as well as the VLSI circuit equivalent problem, and formulate the corresponding nonlinear equations for a specified HBT device that operates at DC or AC condition. Sec. 3 discusses the MI and GA methods applied in the solution and optimization of nonlinear equations. Sec. 4 presents the computed results for the HBT circuit optimization problem. Comparison result is reported to show the good accuracy of the method. In addition, related criteria including fitness are also demonstrated to show the intelligence and robustness of the method. In Sec. 5, we draw the conclusion and suggest the future works.

## 2 A HBT Circuit Model

As shown in Fig. 1, the simulation model is firstly formulated with circuit nodal equations, where the Gummel-Poon large signal Model is used in the simulation [17-18]. For the HBT device, where the Early effect can be ignored because high doping concentration in the Base of HBT.

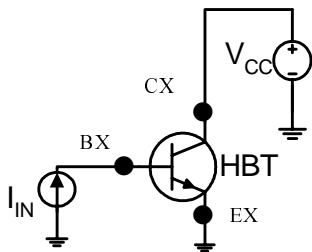


Fig. 1. A HBT circuit for the DC analysis.

The circuit for DC analysis and two-tone AC characteristics simulation are shown in Figs. 1 and 2.

First of all, the DC circuit is simulated to find the DC solutions. The result shows the very good accuracy of the proposed method. The similar method is then can be further applied to simulate the circuit with a two-tone input signal (Fig. 2). The HBT model applied in the DC simulation, as shown in Fig. 3, is so-called the Gummel-Poon large signal model. For node C, we write the corresponding circuit node equation as shown in equation (1). Similarly, we have the following set of equations to be solved both in DC and AC conditions. For nodes E, B, BX, CX, and EX the equations are formulated.

$$C_{J_{CX}} \left( \frac{dV_{BX}}{dt} - \frac{dV_C}{dt} \right) + C_{DR} \left( \frac{dV_B}{dt} - \frac{dV_C}{dt} \right) + C_{J_{CI}} \left( \frac{dV_B}{dt} - \frac{dV_C}{dt} \right) + I_2 + I_{BL2} - \frac{I_{CT}}{q_b} + \frac{V_{CX} - V_C}{R_C} = 0 \quad (1)$$

$$C_{DF} \left( \frac{dV_B}{dt} - \frac{dV_E}{dt} \right) + C_{JE} \left( \frac{dV_B}{dt} - \frac{dV_E}{dt} \right) + I_1 + I_{BL1} + \frac{I_{CT}}{q_b} + \frac{V_{EX} - V_E}{R_C} = 0 \quad (2)$$

$$C_{DR} \left( \frac{dV_B}{dt} - \frac{dV_C}{dt} \right) + C_{J_{CI}} \left( \frac{dV_B}{dt} - \frac{dV_C}{dt} \right) + C_{DF} \left( \frac{dV_B}{dt} - \frac{dV_E}{dt} \right) + C_{JE} \left( \frac{dV_B}{dt} - \frac{dV_E}{dt} \right) + I_1 + I_{BL1} + I_2 + I_{BL2} + \frac{V_B - V_{BX}}{R_B} = 0 \quad (3)$$

$$C_{J_{CX}} \left( \frac{dV_C}{dt} - \frac{dV_{BX}}{dt} \right) + \frac{V_B - V_{BX}}{R_B} + \frac{V_{IN} - V_{BX}}{R_{B2}} = 0 \quad (4)$$

$$\frac{V_C - V_{CX}}{R_C} + \frac{V_{CC} - V_{CX}}{R_{CCS}} = 0 \quad (5)$$

$$\frac{V_E - V_{EX}}{R_E} - \frac{V_{EX}}{R_{EE}} = 0 \quad (6)$$

The equation (1)-(6) forms the nonlinear ODEs for a HBT circuit operating in DC and AC conditions. For the DC analysis, this model becomes a set of coupled nonlinear algebraic equations. The conventional approach to solve this set of nonlinear equations is applied the Newton's method. However, the Newton's method converges only with the initial guess is in the neighborhood of the exact solution. This leads to sufficiently difficult in the practical

implementation of VLSI circuit simulation. Because it is impossible that we can figure out the exact solution of the model, to apply the Newton's method for large scale VLSI circuit simulation often require special treatment for finding a closed solution to approach the final solution iteratively. In this work, we focus here on the DC analysis and optimization.

This approach is applied our proposed MI as well as a GA method. We have successfully applied the MI method for the numerical solution of semiconductor device equation as well as VLSI circuit equations [9-16]. This approach converges globally and has good accuracy for practical applications. With the similar approach, the AC analysis is also can be computed directly. We can find including physical constants there are more than thirty different parameters (partially listed in Tab. 1) should be evaluated when solving both the circuit DC and AC characteristics. As shown in Fig. 3, the model is the Gummel-Poon large signal model. The details of these physical models and quantities can be found, for example in [17-18].

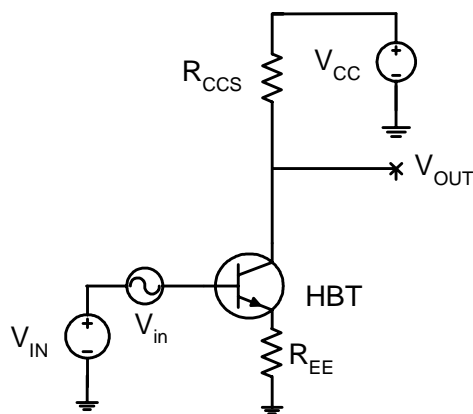


Fig. 2. A HBT circuit for the AC signal simulation.

As shown in Fig. 3, there are current and capacitor terms included in the Gummel-Poon model. These models are rather complicated and have strong nonlinear responses with respect to the input signal. In our numerical experience, the MI method solves the nonlinear circuit model including these nonlinear equations have very good efficiency and robustness.

To obtain the device I-V curve as shown in Fig. 4, we have to solve the above equations (1)-(6) in the DC or AC conditions and then adjust all possible parameters such that the I-V curve of the HBT circuit meets the specified engineering requirement. This task is not only an empirical-based but also time-consuming job. Due to the local and sensitive property, those circuit simulator based on the Newton's method (such as the famous SPICE circuit simulator) have their limitations in practical

applications. The MI and GA methods applied here for the device I-V curves characterization and optimization have a significantly improvement in the development of TCAD and ECAD.

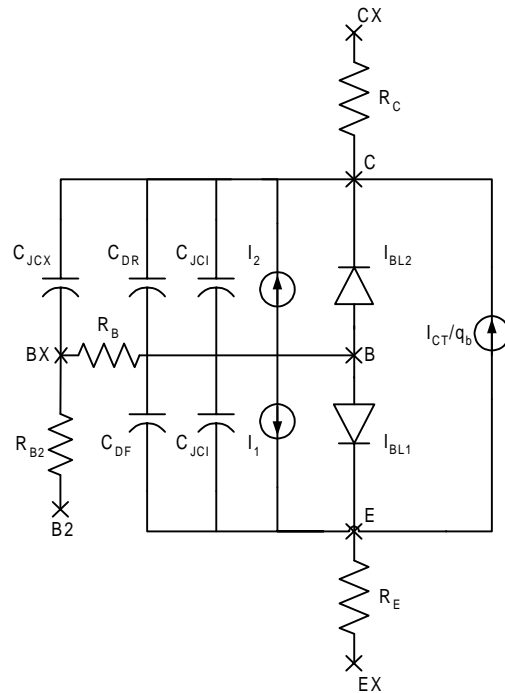


Fig. 3. The Gummel-Poon equivalent circuit model.

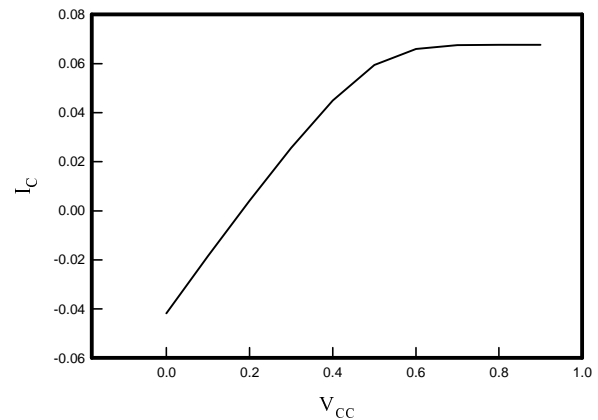


Fig. 4. An illustration of the I-V curve for the HBT device.

### 3 Computational Techniques

In this section, we present the MI and GA methods for the optimization of the model. The MI method is applied for the solution of the nonlinear equations from the VLSI circuit formulation. After the solution procedure, we further use a GA method to optimize the parameters such that the DC I-V characteristics satisfy the desired specification. The GA applied in this work includes some steps: gene encoding, fitness function, selection, reproduction, and mutation.



*Step. 5. Mutation.* When all chromosomes of the next generation are generated, mutation can change factors of some chromosomes directly. The chromosomes and their position of factors will be determined with random. In our work, the chromosome mutation probability constant  $M_C$  and the factor mutation probability constant  $M_g$  will select the number and position of the mutation.

## 4 Results and Discussion

We present the results of the DC I-V curves, where the evolutionary I-V curves are included to show the novelty of the method. The fitness results give the efficiency of this simulation. For a single I-V point evolution, Fig. 8 shows there are more efficient results if we use the proposed GA to find the optimal parameters with 4 variables than it with 15 variables.

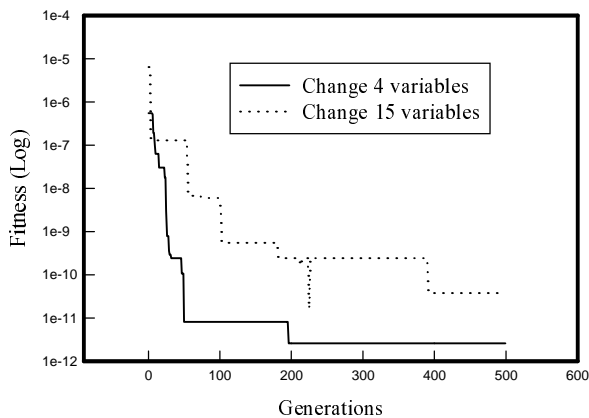


Fig. 8. A plot of the fitness score with various number of evolution variables for the single DC I-V point simulation.

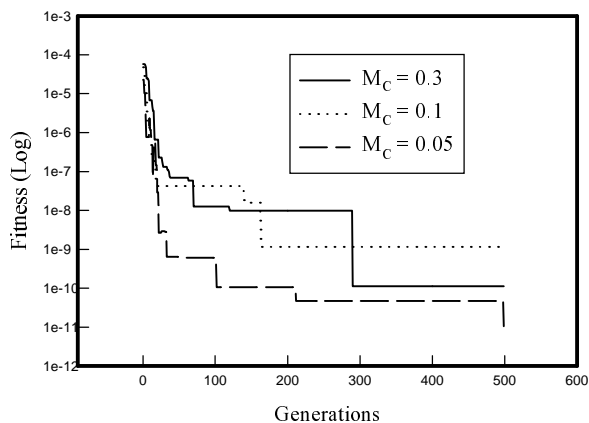


Fig. 9. A plot of the mutation rate and fitness score for the single DC I-V point simulation.

As shown in Fig. 9, when the  $M_C$  equals 0.05, the average fitness score grow up fast, and as long as the  $M_C$  increases, the evolution speed decreases. We can

say that the overhead mutation rate will affect the diversity of this population, and it will not tend to an optimal solution easily. Fig. 10 shows that the fitness score versus the generations. We find the evolution with more variables has larger search domain and hence it has better score after more generations.

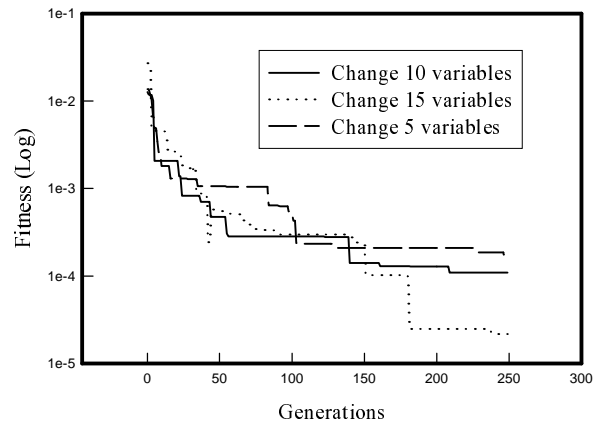


Fig. 10. A plot of the fitness score with various number of evolution variables for the single DC I-V curve simulation.

As shown in Fig. 11, we further present the difference of the fitness score for the single DC I-V curve simulation and evolution that with or without a specified weight function. Our simulation shows that the method with the weight function it better than the other. Fig. 12 shows the evolutions of the I-V curve. We start from an arbitrary I-V curve and our simulator will approach to the desired final I-V curve. Based on the MI and GA methods, the above process, from a given I-V curve to the final optimal I-V curve, is solved and evolved automatically. Compared with the conventional trial-and-error methodology to extract optimal parameters of the circuit model, our novel approach successfully reduces the complex procedures and calculating time.

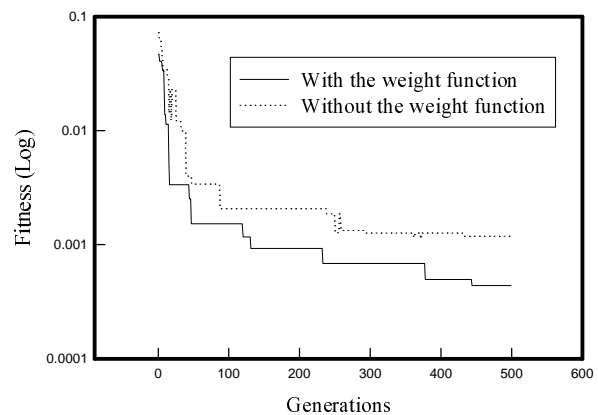


Fig. 11. Comparison of the method with and without the weight function for the single DC I-V curve simulation and optimization.

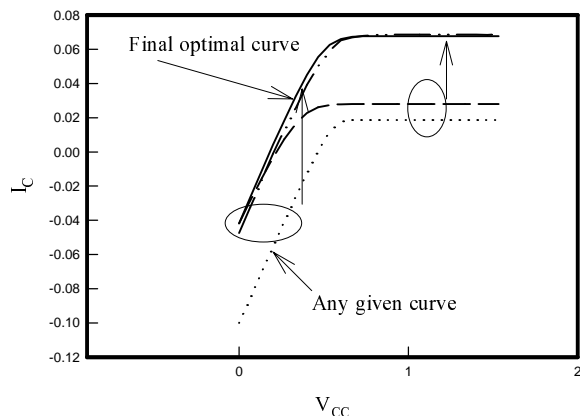


Fig. 12. An illustration of the single DC I-V curve approximation.

## 5 Conclusion

We for the first time have successfully applied the MI and GA methods to solve and optimize the DC I-V characteristics of the HBT device. The VLSI equivalent circuit model is utilized to model the HBT device, where the nonlinear equations are solved with the MI method. The computed results are optimized with our proposed GA method. Numerical results for the HBT device have been presented to show the accuracy, efficiency, and robustness of the method. This novel simulation provides an alternative in the advanced applications of TCAD and ECAD.

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