Substrate Noise Reduction in CMOS Transistors: a methodology definition

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Abstract: Substrate coupling can corrupt low level analog signals and impair the performance of monolithic integrated circuits. Therefore, a characterization methodology able to evaluate the efficiency of the countermeasures against crosstalk, appears very important for designers. In this paper, after the verification that PMOS transistors are more sensitive to substrate voltage fluctuations than NMOS ones, a new method is indicated for the noise reduction

Key-Words: substrate crosstalk, coupling, sensors, small signal model

1 Introduction

Substrate coupling is the phenomenon whereby devices fabricated on a semiconductor die interact with each other through the common conductive substrate. Substrate coupling can corrupt low level analog signals and impair the performance of monolithic integrated circuits [1].

Some circuits, such as low noise amplifier and switching circuits, have traditionally been built on separate substrates in order to minimize parasitic interaction between them,[2], [3]. Circuit designers view the integration of noise generating circuits and low noise circuits on the same substrate as a major challenge.

The modern bent for high levels of integration has many advantages such as the reduced package count (which lead to lowered costs and reduced sizes) and the decrease of the power dissipation as fewer pads and interconnect lines need to be driven. However, the mayor disadvantage of the integration is the increased interaction between circuits that can occur either for the presence of mutual inductance and capacitance between any two bond-wires and pins in a package, or for the presence of the common substrate shared by the circuits having a non-zero dielectric constants and conductivities. Substrate coupling can corrupt low level analog signals and impair the performance of monolithic integrated circuits [4].

In this paper, after the evaluation of substrate noise sensitivity for PMOS and NMOS transistors, a fully DC characterization methodology for shielding structures is presented.

It adopts a resistive network to modelize the substrate and it is able to describe more complex situations.

Section 2 introduces the substrate coupling phenomenon and describes its sources. Section 3 indicates the different approaches for substrate noise quantification Section 4 describes how NMOS and PMOS transistors act as sensors of substrate noise and indicates a new methodology for the characterization of a simple countermeasure. Finally some conclusions are drown out.

2 Mechanisms for current injection

All the currents injected into the substrate cause fluctuations of the substrate voltage that affect other sensitive areas in the circuit (substrate crosstalk). Different mechanisms contribute to the injection of currents and have to be considered in modeling the electrical circuits. The common active and passive devices, such as MOS transistors, bipolar junction transistors, resistors, capacitors, etc., can act as substrate noise injectors and a sufficiently low impedance path must be provided near each component in order to collect the parasitic current. The principal mechanisms for current injection into the substrate in CMOS circuits are the capacitive injection, the impact ionization and the inductive noise.

Every device on an IC die is capacitively coupled to the substrate through its p-n junction depletion capacitancies.

Capacitive coupled substrate current is of significant consequence in mixed-signal circuits, due to the presence both of a large number of switching digital nodes that inject such currents into the substrate and of high impedance path that are affected by these currents.

The *impact ionization* is the generation of electron-hole pairs as consequence of collisions of

thermal generated electrons with atoms, when the p-n junction is under reverse bias. When the electric field in the depleted drain of a MOS transistor becomes large enough to cause impact ionization, the generated electron-hole pairs cause a current flow to the substrate. This current depends on the drain current, the oxide thickness, the drain junction depth and the difference between the drain to source voltage and the drain to source voltage at saturation [5]. The nature of current injection due to capacitive coupling and avalanche induced currents is different because hot electron induced currents are always injected into the substrate in the same direction. For instance, in a CMOS inverter the hot electrons induced current will be injected into the substrate during both the low-high and the high-low transitions, while the capacitive component of the current will reverse direction during the two edges. Therefore, hot electrons induced currents will possess large even harmonics of the fundamental switching frequency and a DC component, while capacitive currents will have large odd harmonics and no DC component.

The effect of non ideal inductive power supplies has a great effect on the amount of substrate coupled switching noise in an IC design. When the chip is placed inside its package, bondwires and pins associated with the substrate supply have finite and often large inductances. Hence, any substrate current picked up by this supply can cause large glitches in the substrate supply bias. This phenomenon is referred to as *inductive noise*. The presence of additional parasitic inductances in the substrate supplies can make this phenomenon worse.

A fraction of noise generated by all the mechanisms previously seen, is picked up by sensitive circuitry and can limit its accurancy (pick up mechanism). Substrate noise can be collected by passive devices through parasitic resistors, capacitors, inductors, by transistors through the body effect and by the whole circuit through ground to ground coupling.

3 CMOS transistors as sensors of substrate noise

Considering a MOS transistor as a linear, time independent, concentrated parameters component, it can be modeled as a three port device and the drain current I_{DS} in the operative point Q is expressed as:

$$I_D^Q = I_D(V_{GS}^Q, V_{DS}^Q, V_{SB}^Q) \qquad (1)$$

where V_{GS}, V_{DS} and V_{SB} are gate-source, drain-source and source-bulk voltages, respectively.

If small variations occur in the three bias voltages, than the corresponding change i_d in the drain-source current can be evaluated by a linearization of the function in (1) around Q. Therefore:

$$i_d = \Delta I_D = g_m v_{gs} + g_d v_{ds} + g_{mb} v_{sb} \qquad (2)$$

where $g_m = (\partial I_D/\partial V_{GS})_Q$ and $g_{mb} = (\partial I_D/\partial V_{SB})_Q$ are the small signal gate transconductance and the small signal substrate transconductance, respectively.

The small signal transconductance for several MOS transistors has been measured on wafer using a control process monitor unit composed of p-transistors in n-well and n-transistors in p-well (fig.1).

Fig. 2 shows measured values of $|g_{mb}|$ as a function of V_{GS} and V_{BS}, considering a threshold voltage of about 0.4V when the substrate-source bias voltage is zero and the maximum allowed V_{GS} is 2.5V.

From a physical point of view, if V_{BS} is made increasingly negative and V_{GS} is kept constant, the dimensions of the depletion region increase both around the drain and the source diffusions. Since in this technology an additional doping on the surface is used, channel punch-through is avoided. However, neutral region reduction between source and drain provides a high resistivity path between the channel and the substrate that shields the current to bulk bias voltage variations. Hence, $|g_{mb}|$ reaches a quasi-constant value for V_{BS} = -0.5V or lower. This result can be confirmed using a mathematical model for the device [6].

Simulations show that $|g_{mb}|$ is about two times greater for a PMOS than for an NMOS with the same dimensions and the same bias conditions. Hence, even if PMOS transistors are often used in low-gain input stages of baseband amplifiers because of their lower flicker noise generation, a higher amount of substrate noise related disturbs is picked up and can be amplified in the successive high gain stages.

Moreover, the dependence from V_{DS} is analyzed for an NMOS transistor with V_{GS} = 2.5V (fig.3). It shows that in every biasing conditions, small signal substrate transconductance strongly increases as soon as the bulk is made more positive than the source. This consideration is very important for those applications in which each of the transistors is not included in a separate well or is not protected by a well at all. In such a

case, the DC component of substrate noise can be strong enough to give a positive bulk-source voltage causing the NMOS transistors to be very sensitive to substrate voltage variations.
Fig.4 shows the dependence from the transistor width keeping its length constant, as it happens after the definition of a CMOS technology pattern.
From equation (2), neglecting V_{DS} variations, the current i_d can be thought as the sum of two component:

- the output signal, represented by small variations of the gate-source bias voltage amplified by the small signal gate transconductance $g_m v_{gs}$;
- the substrate noise signal, represented by small variations of the bulk-source bias voltage amplified by the small signal substrate transconductance $g_{mb} v_{bs}$

Assuming equal small variations in the gate-source and bulk-source voltages, it is possible to define a signal to noise ratio benchmark as:

$$\frac{S}{N} = \frac{g_m}{g_{mb}} \qquad (3)$$

which measures the relative control of the gate and the substrate on the drain current variations.
Fig.5 shows measured values of $g_m / |g_{mb}|$ for an NMOS transistor with $V_{DS} = 2.5V$.
Moreover for the signal to noise benchmark is more convenient to have a thinner oxide. In this case, the gate gets closer to the channel and its control stronger, thus the influence of the substrate is smaller.
From fig.6 it is evident that a PMOS has a relative influence of the substrate on the channel about four times larger than an NMOS.

4 Methodology definition

Designers employ a number of techniques to ensure the noise immunity of their design and to control the substrate noise problem. They can be divided in three groups:

- the use of guard rings;
- the use of technology options for increasing the resistivity of the path between the injection and the sensitive point;
- a combination of the two previous solutions.

Two different test chips, named Core and Subc has been adopted to obtain a characterization of the different technology options. The first one has been produced on an epy substrate in BiCMOS technology while the Subc test chip has been built on a no-epy substrate in fully CMOS technology. For the test chips, the array of substrate contacts used to inject either a voltage or a current into the substrate is indicated as source contacts. The substrate diffusion of the source contact has width and length equal to 6μm. With the term sensor contacts is indicated a matrix of contacts each of them equal to a source contact but surrounded by a different technological option.
In order to perform measurements on Core and Subc, each wafer has been placed in a probe station including a microscope and a variable number of probing needles. These can connect peripheral pads and each contact belonging to the contacts matrix on the chip to external equipment. Because of the extremely small dimensions of the contacts matrix (30μm width and length), the tip radius of the used needles is 0.5μm.
The wafer is supported by a golden plate usually named chuck that can be left at a floating potential or can be connected to a bias unit.
To evaluate the effectiveness of the contact between the wafer backside and the chuck, its I-V characteristic has been measured, putting the chuck bias potential to ground (fig.7). The current flowing through the substrate-chuck junction does not vary linearly vs the bias voltage applied to the guard rings. Hence, the back plane-chuck contact is a Schottky contact with two unwanted properties that can affect severely a characterization procedure:

- no current can flow through the junction if the voltage drop at its terminals is lower than the built-in potential,
- above the built-in potential the incremental resistance varies, depending on the bias condition.

Moreover, changing the injection point on the wafer, by choosing another chip or changing the position of the wafer itself on the chuck, the slope of the I-V characteristic changes. This means that the contact resistance between wafer and chuck change, depending on the local roughness of the two contacting surfaces.
In fig.8 a substrate contact is used as an input node for the noise source, voltage or current, and another one, surrounded by a grounded by p^+ guard ring, as a sensor of perturbation injected into the substrate. Due to the resistive and dielectric properties of the substrate, the signal path between input and sensor nodes can be modeled as a distributed network composed of capacitate – resistive impedances.
Considering the parallel between the capacitance and the resistance of a cube of material, with unitary height, width and length, the substrate cut-off frequency f_c is expressed as:

$$f_c = \frac{1}{2\pi\varepsilon\rho} \qquad (4)$$

where f_c represents the frequency at which the attenuation given by the bare substrate is reduced by 3 dB, with respect to the maximum attenuation achievable by a DC bias.

From equation (4), $f_c \cong 150$ GHz and 75 GHz for Core and Subc substrates respectively. Both of the previous values are outside the applications range that goes up to 20 GHz. Therefore, in the application range attenuation is frequency independent so substrate can be modeled as a purely resistive network.

In the previous structure, the guard ring ground node can be considered as a common reference node for both the voltages applied to the source and the sensor nodes. Hence, the substrate distributed resistive network can be seen as a two port resistive network, which will be referred to as Guard Ring Two Port (GTP). The GTP characterization is done by determining the dependence of the attenuation of a signal injected into the source node and measured at the sensor node on the guard ring width and spacing and on the distance between the two contacts and the guard ring. This model has the following benefits:

- the possibility to extract a full characterization of one countermeasure without using the wafer backside contact, skipping its intrinsic unreliability;
- the reliability, feasibility and repeatability of the DC measurements. On chip, DC measurement structures are compact and occupy less area than high frequency ones, so test chips for investigating new substrates adopting this method is cheaper than the ones containing high frequency measurements structures;
- the possibility to be used in circuit level simulators as a conventional circuit element belonging to the simulator device library.

Fig.9 shows how it is possible to use the GTP for evaluating crosstalk effects in more complex configurations. Inductive noise causes variation of the drain voltage in transistors of the digital circuitry. This disturbance couples to the substrate by means of drain-substrate capacitance and propagates into the substrate itself. It is modeled by the GTP. The disturbance reaches a sensitive device (transistors that belong to analog circuitry) and is shielded by a grounded p^+ guard ring coupling with its drain through the drain-substrate capacitance and with its bulk.

The model for the coupling mechanisms between each device and substrate is indicated as Device Substrate Interface Model (DSI). The two diodes represent the drain-substrate capacitance and take into account the coupling mechanism dependence on the frequency. Hence, introducing GTP and DSI as the only additional elements for simulation, the coupling through the substrate phenomenon is considered.

The GTP two port circuit can be fully characterized adopting the Z parameters matrix. Therefore, it is possible to express the current or the voltage I/O attenuation as a function of Z parameters.

5 Conclusions

In this paper, it has been shown that PMOS transistors are more sensitive to substrate voltage fluctuations than NMOS ones. Moreover, a new methodology has been presented for performing a fast and reliable characterization of the transmission path, modeling the substrate as a resistive network.

By means of this simple DC model, it has been shown it is possible to describe more complex situations, like the coupling between two active devices through the substrate.

Finally, as DC measurements are adopted, the test structure is simpler than that necessary for high frequency measurements. This is due to the complexity of RF measurement technique which requires normally the extraction of S- parameters and consequently the higher cost of the test chip.

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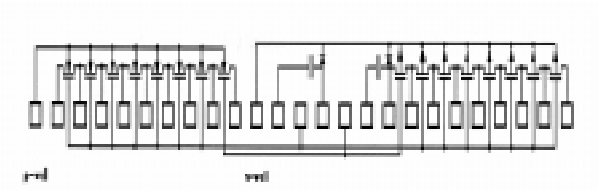
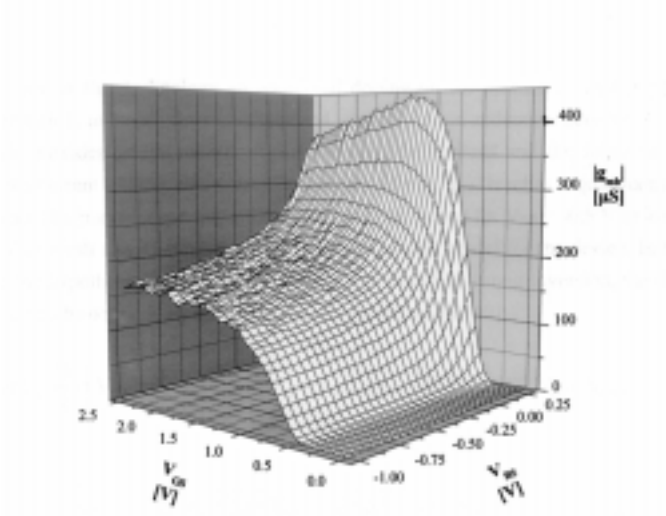
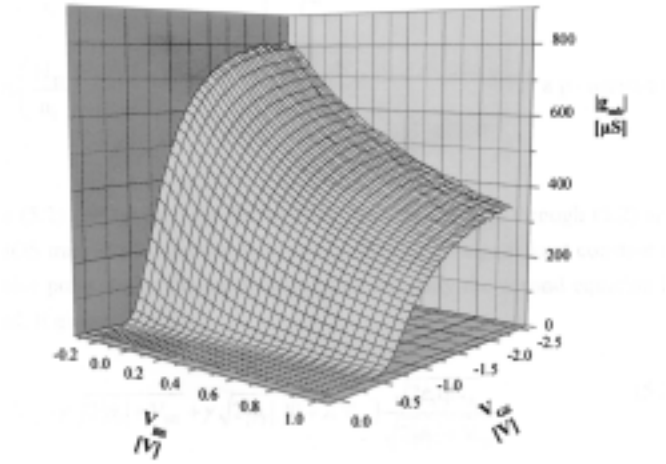


Fig.1 Process control monitor unit



NMOS



PMOS

Fig.2 Measured value of $|g_{mb}|$ for transistor having W=20μm and L=0.25 μm

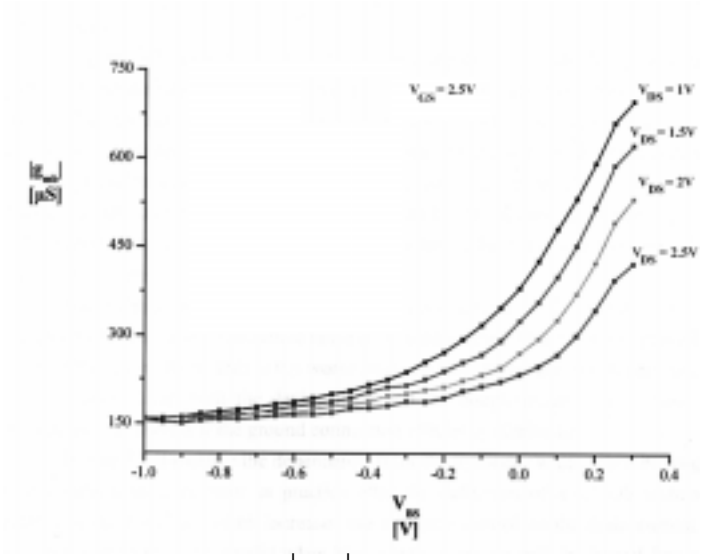


Fig.3 Measured value of $|g_{mb}|$ for an NMOS having W=20μm and L=0.25 μm

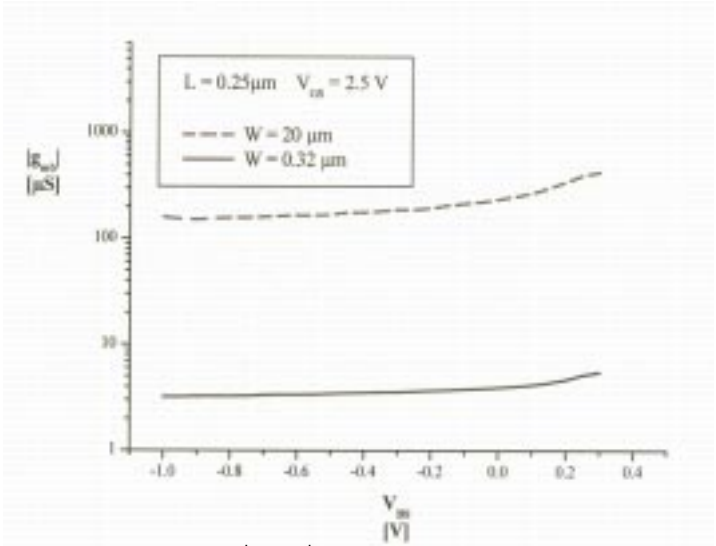


Fig.4 Dependence of $|gmb|$ from the transistor width

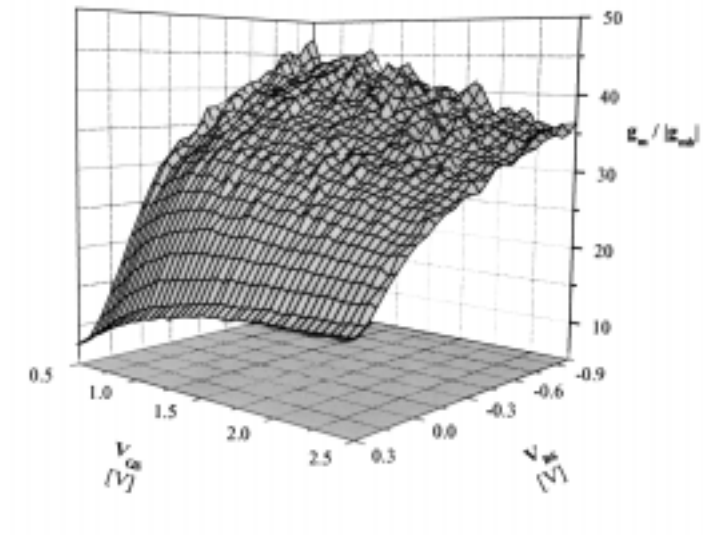


Fig.5 Measured value of $g_m/|g_{mb}|$ for an NMOS having W=20μm and L=0.25 μm

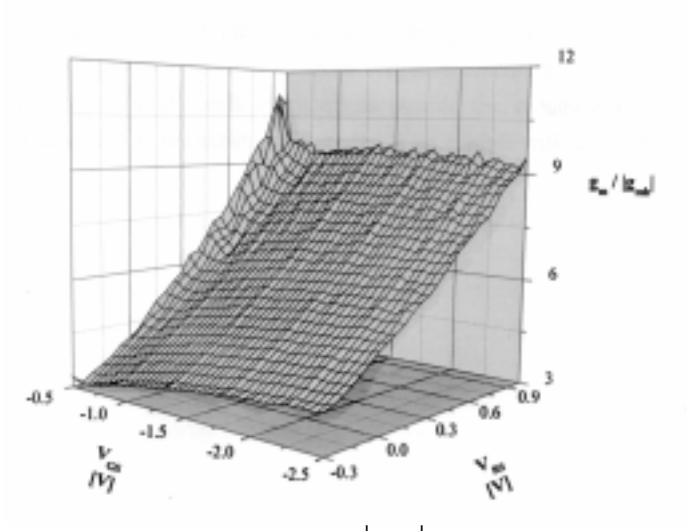


Fig.6 Measured value of $g_m/|g_{mb}|$ for an PMOS having W=20μm and L=0.25 μm

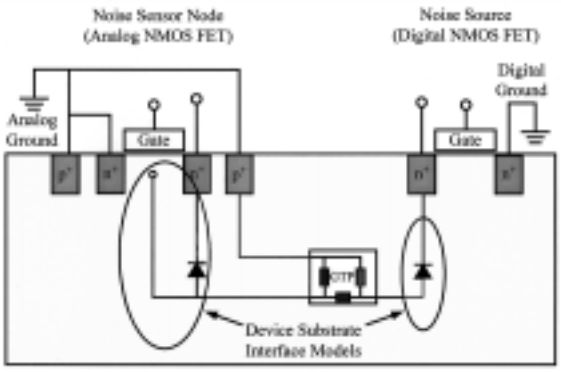


Fig.9 A simple model for the propagation of noise inside the substrate

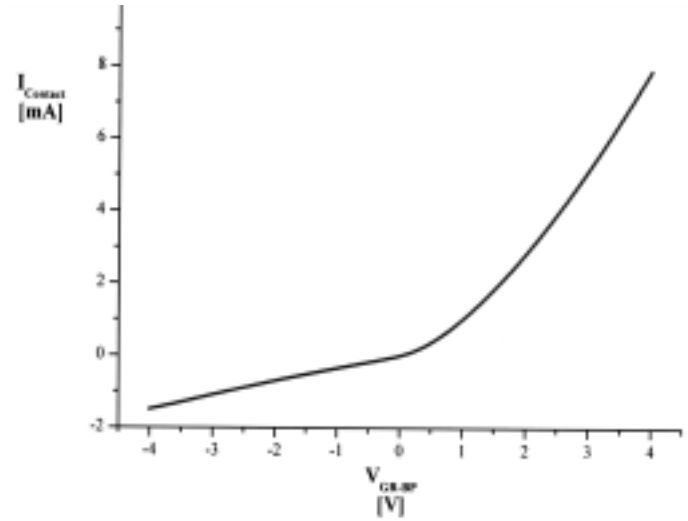


Fig.7 I-V characteristic of the substrate-chuck junction

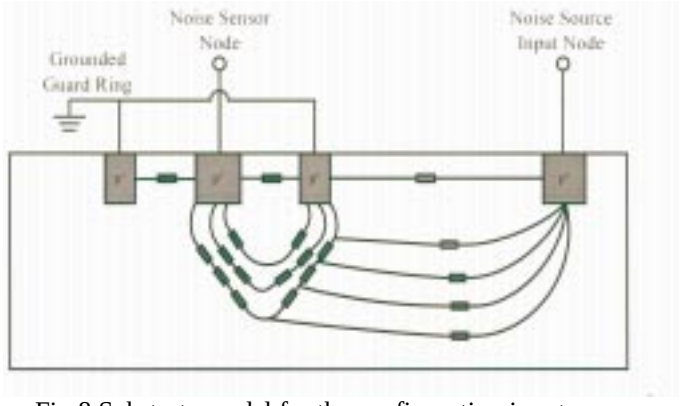


Fig.8 Substrate model for the configuration input node-grounded guardring –sensor node