COMPUTING SYMBOLIC TRANSFER FUNCTIONS FROM SPICE FILES USING NULLORS

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ABSTRACT

A MAPLE^{TM}-based program focused on transforming SPICE circuit-models to nullor-based models in order to compute symbolic transfer functions (TFs), is described. It is shown that by transforming all SPICE circuit-models to nullor-based models, the circuit analysis ends in a pure nodal analysis (PNA), i.e. avoiding the computation of stamps as it is done in the MNA and the *Tableau* formulations. Most important is that the system of equations is reduced in one order for each nullor when using the properties of the nullator-norator pairs. To show the computational advantage of the proposed method, several illustrative examples are given.

1. INTRODUCTION

Nowadays, the design automation of electronic circuits is moving towards the use of hardware description languages (HDLs). The HDLs use different abstraction levels where the more detailed the structure, the less abstract the description. In the analog domain, analog HDLs use a top-down approach to design from systems-to-circuits and a bottom-up approach to synthesize from circuits-to-systems [1]. Additionally, all HDLs permit the inclussion of analysis-techniques in the DC, AC and time domain. In the AC domain, circuit analysis can be performed using linear techniques, implying that circuit responses are independent of the signal amplitudes [2]. That way, a circuit simulator, e.g. SPICE [3], predicts the performance of linear circuits where, ideally, a single frequency input produces the same frequency output; while the amplitude and phase can be changed. During the last three decades SPICE has been the most-used circuit-simulator [3], it can be classif ied within the circuit abstraction level. Furthermore, circuit-to-system simulators are very much needed [2]. Additionally, it is required by the designer to have a program oriented to compute symbolic TFs [4], in order to get more insight about the behavior of the circuit. That way, using MAPLE [5], a MAPLE-based method focused on computing fully-symbolic TFs is described herein.

Symbolic analysis results in equations relating circuit performance in which the best mathematical approach is based on the modeling capabilities. In this work, all analog circuits are modeled using the nullor concept in order to improve the computation of symbolic TFs using MAPLE [5]. As shown along the paper, when modeling analog circuits using nullors, the analysis ends in the application of a PNA method [9, 6, 7]. The main idea is oriented to transform all non-NA-compatible elements, i.e. avoiding the use of stamps [1, 3, 2], to be NA-compatible ones using the nullor properties. Additionally, it is shown that by applying the nullator-norator properties, the system of equations is reduced in one order for each nullor. The matrix-reduction process is related with the handling of the columns and rows associated to the properties of the nullators and norators, respectively.

2. MODELING SPICE CIRCUITS USING NULLORS

The design automation environments of modern analog and mixed-mode systems tends more to a top-down approach using libraries and macrocells [1]. Linked to this, an analog modeling approach based on the circuit and macromodel abstraction levels, is described along this section using nullors.

The nullor can be represented as a two-port device as shown in Fig. 1. It is composed of two elements: the nullator connected at its input-port, where $v_1 = i_1 = 0$, and the norator connected at its output port where $v_2 = i_2 = \infty$.

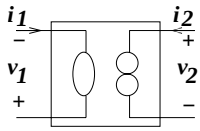

Fig. 1. The two-port nullor element

2.1. Modeling the four controlled sources

The four controlled sources can be modeled by applying a unified approach as that made in [6, 7], they are shown in Fig. 2. The gain k associated to each SPICE controlled-source model, is given as a function of the conductances associated to each nullor-based controlled-source model. The bias references of the nullor-based models have been established through considering the bias references from the SPICE models, this should be taken into account during the transformation process.

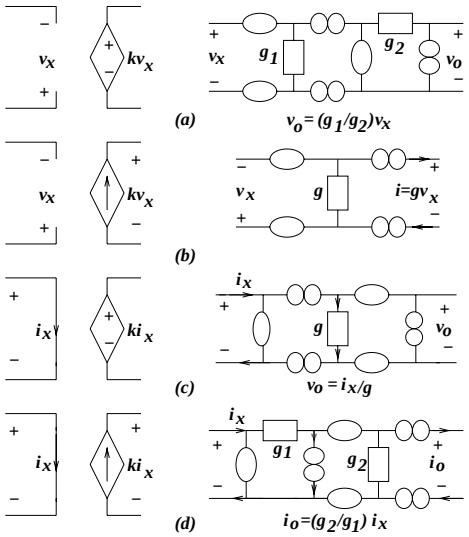

Fig. 2. The four controlled sources

In an abstraction level higher than the circuit one, the four basic amplifiers also can be represented by the four controlled sources, however, the nullor-models shown in Fig. 2 are not suitable for a synthesis process [9].

2.2. Modeling the MOS transistor

Although the MOS transistor (MOST) is a nonlinear device, when it is biased operating in the active region, its behavior can be modeled by a voltage-controlled current-source, as shown in Fig. 2b, where the gain k models its transconductance g. The parasitic capacitances, e.g. C_{gs}, C_{gd}, can be easily added to its nullor-based model as shown in Fig. 3.

3. TRANSFORMING SPICE CIRCUIT-MODELS TO NULLOR-BASED CIRCUITS

A SPICE-circuit net-list is transformed into a nullor-circuit net-list by applying the transformation procedure sketched in Fig. 4. The first step consists of two procedures:

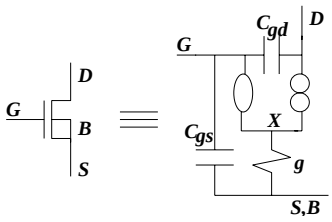

Fig. 3. The MOS Transistor

1. Searching the maximum node-number (max-node) and

2. Reading and saving the SPICE net-list into a data-structure

by saving the elements into a data-structure containing the name, nodes and values of the file *.cir. The second step consists of:

1. Replacing each SPICE circuit-model using its nullor-based circuit-model. For the case of a MOST, as that shown in Fig. 3, its nullor-based circuit-equivalent requires the addition of a node labeled by X. The value of X equals to the value max-node+1.

2. When all SPICE circuit-models have been replaced by their corresponding nullor-based model, the program writes an output-text file *.txt.

The file *.txt is used furtherly to formulate the system of equations modeling the nullor circuit in order to compute symbolic TFs using the technique given in [6, 7].

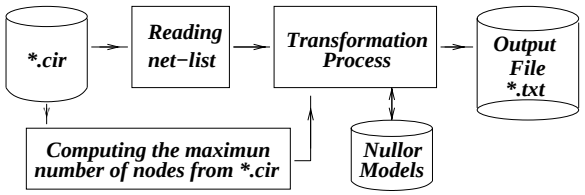

Fig. 4. Transforming SPICE-circuits to nullor-circuits

4. COMPUTING A SYMBOLIC TF

The computation of a symbolic TF requires a higher computational effort to handle symbols instead of numbers. SPICE uses the modified nodal analysis (MNA) method which requires the computation of the stamp associated to every non-NA-compatible element. In [6, 7], it is shown that by modeling all non-NA-compatible elements using nullors, the resulting nullor-circuit contains

NA-compatible elements only. This transformation procedure leads us to apply a PNA method which avoids the computation of stamps and reduces the CPU-time.

To compute the TF of a given circuit, one must obtain f irst the small-signal equivalent by short-circuiting all DC independent voltage-sources and open-circuiting all DC independent current-sources. However, in order to let a connected graph, it is necessary to connect a conductance between the nodes associated to an independent DC current-source.

Since an independent voltage-source is non-NA-compatible, however, using nullors it can be transformed to be NA-compatible, as shown in Fig. 5. By transforming an independent voltage-source to a nullor-based current-source, one should to add one node and three elements more. Besides, when applying the PNA method, the nullor-based current-source is quite appropriate than the independent voltage-source alone, this fact has been demonstrated in [6, 7].

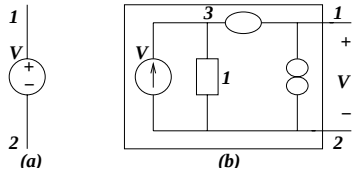

Fig. 5. Transforming a voltage-source to current-source

In order to compute the symbolic TF associated to a nullor circuit, by applying the PNA method, one must compute the following steps:

1. Compute the small-signal nullor circuit-equivalent
2. Compute equation (1), where **i** represents the excitation vector, Y_{NA} represents the linear nodal admittance-matrix, and **v** represents the voltage-variables vector.

$$i = Y_{NA} v \tag{1}$$

3. Use the nullator-norator properties in order to reduce the order of the matrix Y_{NA} in one for each nullor, as established in [6, 7]. This process leads us to compute a compacted matrix called Y_{PNA}, which is given by:

$$i = Y_{PNA} v \tag{2}$$

4. Compute the output-variable given in vector **v**, and handle the expression, using Ohm's law when necessary, in order to obtain the desired symbolic TF.

In short, the proposed computational approach for symbolic circuit analysis consists of three main stages:

1. The formulation of the system of circuit-equations
2. The reduction of the system of equations using the nullator-norator properties, and
3. The solution of the system of equations

The MAPLE-based implementation of the PNA method is summarized in Fig. 6.

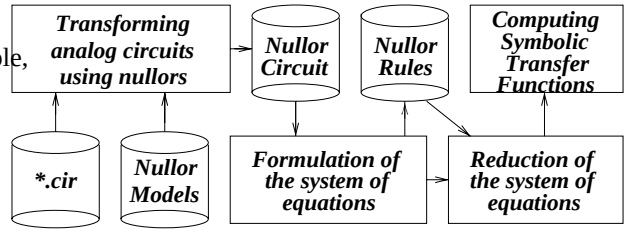

Fig. 6. Symbolic Circuit Analysis

5. THE FORMULATION STEP

Lets consider the opamp-circuit shown in Fig. 7a. It is well-known that the symbolic TF of this circuit becomes $\frac{V}{I} = -Y^{-1}$.

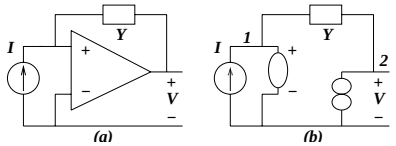

Fig. 7. Modeling an opamp using the nullor

The formulation of the circuit-equations begin by macro-modeling the opamp using the nullor [9], as shown in Fig. 7b. For the nullor-circuit, the NA formulation is done according to equation (1). The matrix Y_{NA} is formulated by considering equations (3) and (4), where i and j denote a node and n the number of nodes.

$$y_{ii} = \sum_{i=1}^{n} y_i \tag{3}$$

$$y_{ij} = -(y_{ii} \cap y_{jj}) \tag{4}$$

That way, the formulation of the circuit-equations of the nullor-circuit shown in Fig. 7b, becomes:

$$\begin{bmatrix} I \\ 0 \end{bmatrix} = \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{5}$$

6. THE REDUCTION STEP

The reduction process is based on the following nullator-norator properties [9, 6, 7]:

1. Since the voltage across a nullator becomes zero, in Fig. 8, the nodes 1,2,3,4 become virtually connected so that the resulting admittance is the sum of all the admittances located at *columns* 1,2,3,4 in the matrix Y_{NA}. The column 1 is maintained while columns 2,3,4 become deleted.

Fig. 8. Floating nullators

Fig. 9. Floating norators

Fig. 10. Grounded (a) nullator and (b) norator

2. Since the current through a norator circulates from node+ to node-, in Fig. 9, the nodes 1,2,3,4 become virtually connected so that the resulting admittance is the sum of all the admittances located at *rows* 1,2,3,4 in the matrix Y_{NA}. The row 1 is maintained while rows 2,3,4 become deleted.

3. For a grounded nullator, as shown in Fig. 10a, node X is virtually connected to ground, so that the column X is deleted in the matrix Y_{NA}.

4. For a grounded norator, as shown in Fig. 10b, node X is virtually connected to ground, so that the row X is deleted in the matrix Y_{NA}.

By applying this rules, equation (5) is reduced in one column associated to the nullator connected to node 1, and in one row associated to the norator connected at node 2. The resulting equation is given by

$$I = -Yv_2 \tag{6}$$

Since $v_2 = V$, the desired symbolic TF becomes

$$\frac{V}{I} = -Y^{-1} = -Z \tag{7}$$

7. EXAMPLES

7.1. Low-voltage MOS current amplif ier

The advantage of this method, focused on improving the computation of symbolic TFs, is demonstrated herein by transforming the low-voltage MOS current-amplif er shown in Fig. 11 [8], into a nullor-based circuit.

7.2. The transformation process

The current-amplif ier has the SPICE net-list given in Table 7.2. From the SPICE net-list, the transforming process is done as follows:

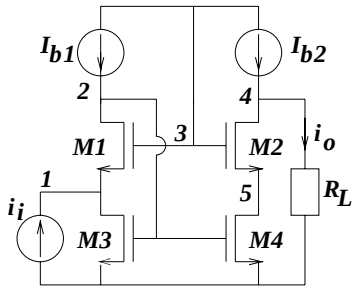

Fig. 11. Low-voltage MOS current-amplif ier

Table 1. SPICE-circuit net-list

...					
ii	1	0	AC	1	
Ib1	3	2	10u		
Ib2	3	4	10u		
M1	2	3	1	1	MOSN
M2	4	3	5	5	MOSN
M3	1	3	0	0	MOSN
M4	5	2	0	0	MOSN
RL	4	0	10k		
...					
.end					

1. The computation of the maximum node-number equals to max-node=5.

2. The reading process leads us to save the name, nodes and values of each SPICE circuit into a data-structure.

3. Using the nullor-based MOST model shown in Fig. 3, the max-node value, and the data-structure, the transformation process ends in the nullor circuit shown in Fig. 12. Note that the nodes associated to each MOST do not change, while the additional nodes are added from the max-node value, i.e. 6,7,8,9. Since the symbolic TF is computed from the small-signal equivalent, node 3 is short-circuited and each DC bias current-source is open-circuited but connecting a conductance g_b between its nodes in order to maintain the connectivity of the network.

4. Finally, the MAPLE-based program ends writting the output-f ile given in Table 7.2, from which the

symbolic TF is computed furtherly in a post-processing step.

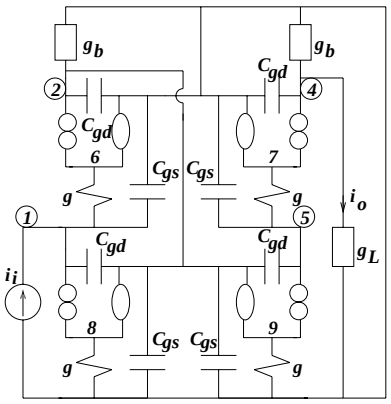

Fig. 12. Nullor-based current-amplifier

To compute the symbolic TF of the low-voltage nullor-based current-amplifier, using the technique given in [6, 7], the following steps are done:

Table 2. Nullor-circuit net-list

ii	1	0	AC	1
gb1	0	2		
gb2	0	4		
NM1	6	0	2	6
gM1	6	1		
CgsM1	0	1		
CgdM1	0	2		
NM2	7	0	4	7
gM2	7	5		
CgsM2	0	5		
CgdM2	0	4		
NM3	8	2	1	8
gM3	8	0		
CgsM3	2	0		
CgdM3	2	1		
NM4	9	2	5	9
gM4	9	0		
CgsM4	2	0		
CgdM4	2	5		
gL	4	0	1E-4	
.end				

1. The computation of the matrix Y_{NA} is given as:

$$\begin{bmatrix} g2+s\,Cg2 & 0 & -g2 & 0 & 0 & 0 & 0 & 0 \\ 0 & g1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -g2 & 0 & g2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & gb+s\,(Cg1+Cg2) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & g3 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & s\,Cg4+g4 & -g4 & 0 \\ 0 & 0 & 0 & 0 & 0 & -g4 & g4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & gb+gx \end{bmatrix}$$

2. Using the nullor properties, the reduced matrix Y_{PNA} is given by:

$$\begin{bmatrix} g2+s\,Cg2 & g1 & 0 & 0 \\ -g2 & gb+s\,(Cg1+Cg2) & 0 & 0 \\ 0 & g3 & s\,Cg4+g4 & 0 \\ 0 & 0 & -g4 & gb+gx \end{bmatrix}$$

3. Finally, by considering that the four MOST being equal, the fully-symbolic TF of the current-amplifier is given by the following equation:

$$\frac{i_o}{i_i} = -\frac{g^3}{2C_{gs}^3 s^3 + 4gC_{gs}^2 s^2 + 3g^2 C_{gs} s + g^3} \qquad (8)$$

By replacing the symbolic-variables with their numerical values, a rational function in the **s** domain can be obtained from which the well-known bode-diagrams can be easily computed in a post-processing step.

7.3. BJT current amplifier

Lets consider the circuit shown in Fig. 13 [9]. By modeling the BJT by a nullor joining the bottom terminals of the nullator and norator, the resulting nullor-based circuit is shown in Fig. 14.

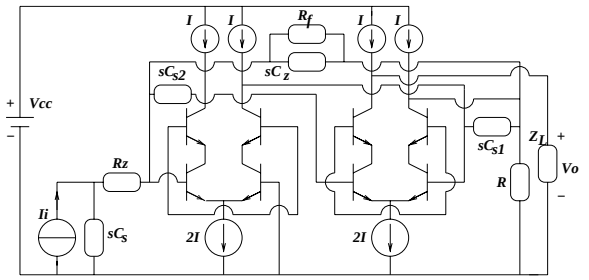

Fig. 13. BJT-based current amplifier

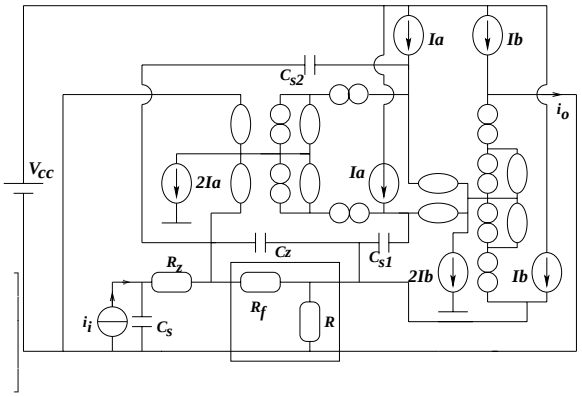

Fig. 14. Nullor-based current amplifier

As one sees, the nullor-based circuit has eight nullors, that way, the matrix Y_{NA} is reduced in eight orders!. The final symbolic TF becomes:

$$\frac{i_o(s)}{i_i(s)} = -\frac{g_z(g+g_f+sC_z+sC_{s1})(C_{s1}+C_{s2})+sC_{s1}^2}{(g_z+sC_s)[(g_f+sC_z)(C_{s1}+C_{s2})+sC_{s1}C_{s2}]} \quad (9)$$

8. CONCLUSION

A MAPLE-based program focused on computing the symbolic transfer function (TF) of an SPICE circuit using nullors, has been described. It was shown that when the given SPICE-circuit is transformed to a nullor-circuit, the circuit analysis ends in a PNA method. The main advantage of transforming SPICE-circuits to nullor-circuits is that the application of the PNA method avoids the computation of the stamps associated to every non-NA-compatible element, leading to an improvement in the CPU-time.

It has been shown that the system of equations of any nullor-circuit can be formulated using the NA method, this ends in the computation of equation (1). By applying the nullator-norator properties, the system of equations has been reduced in one order for each nullor by handling the columns and rows of the admittance-matrix Y_{NA}. Finally, from the reduced matrix called Y_{PNA}, the computation of the fully-symbolic transfer function (TF) has been easily done. From the examples given in section 7, we can conclude on the suitability and appropriateness of the MAPLE-based method to be used as a symbolic circuit-simulator.

The program for computing symbolic TFs using MAPLE from SPICE-circuits can be solicited to the CAD-group at INAOE. The contact email is e.tlelo@ieee.org

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