GENERATING GAUSSIAN FUNCTIONS USING LOW-VOLTAGE MOS-TRANSLINEAR CIRCUITS

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Abstract: - The design of a gaussian function (GF) implemented in a CMOS standard technology, is presented. The proposed design is based on the Translinear Principle (TP) using MOS transistors (MOSTs) biased in weak-inversion. Simulation results using HSPICE for a 0.6um technology of AMS, demonstrate the suitability and appropriateness of the proposed design to be used in low-voltage and low-power applications, e.g. in wavelets processing.
Key-Words: - **Analog Design, MOS Translinear Circuits, Low-Voltage, Wavelets.**

1 Introduction

The demand of portable systems have been made possible the development of new design-methodologies for low-voltage applications [1]-[3], using the TP [4]-[8]. The main advantage of Translinear Circuits (TCs), is that they inherently present a very-low sensitivity to temperature variations. MOS-TCs have several advantages with respect to BJT-TCs, namely: they do not present finite current-gain, they present low saturation-voltages, which is quite convenient for low-voltage applications, and they have an extra-dependence on the drain-current [6]. Besides, the body-effect (BE) represents a serious limitation, it can be reduced by connecting the Bulk and Source together using a technology of two-wells [2]. In this manner, the design of a MOS-circuit for generating GFs, based on the TP, is presented.

The mathematical representation of a GF, is given in section 2. Several implementations are listed in section 3. A technique for offset and BE compensation, is introduced in section 4. The proposed design and its simulation results using HSPICE, are given in section 5. Finally, the conclusions are listed in section 6.

2 Mathematical Representation

The behavior of a GF [7]-[8] is given by:

$$h_{s,\tau}(t) = \frac{1}{\sqrt{S}} e^{-\frac{1}{2}\left(\frac{t-\tau}{S}\right)^2} \quad (1)$$

S represents a scale-factor, τ represents the translation in time. Equation (1) represents the behavior of a normalized GF which associates the optimum time-bandwidth product.

3 Translinear Circuits

There exist a plethora of circuits based on the TP using BJTs [4]. That circuits can be realized using a CMOS standard technology biasing the MOSTs in weak-inversion. In this manner, the drain current of an NMOS is [2]-[3]

$$I_D = \frac{W}{L} I_{DO} e^{\frac{(n-1)V_{BS}}{nVt}} e^{\left(\frac{V_{GS}-V_{TH}}{nVt}\right)} \left(1 - e^{\frac{-V_{DS}}{Vt}} + \frac{V_{DS}}{V_0}\right) \quad (2)$$

V_{BS} is the bulk-source voltage (BE), V_{TH} the threshold voltage, V_t the thermal voltage, V_0 the Early voltage, and n the slope factor, usually less than 2, and 1 for large values of V_G. I_{D0} is a current associated to the transconductance parameter K' by [3]:

$$I_{D0} \cong \frac{2K'(nVt)}{e^2} \quad (3)$$

Minimizing the BE, equation (2) is reduced to:

$$I_D \cong \frac{W}{L} I_{DO} e^{\left(\frac{V_{GS}-V_{TH}}{nVt}\right)} \quad (4)$$

3.1 Circuit of Quadrature

A MOS-based quadrature-circuit, realized by M1-M5, is shown in Fig. 1. Equation (4) is used to minimize the BE, but satisfying (5).

$$Iy + I\alpha > 0 \quad (5)$$

Using the TP it can be demonstrated that

$$I_o = \frac{I_{d1} * I_{d2}}{I\alpha} \quad (6)$$

By applying KCL through M1-M2 one get

$$I_{d1} = \frac{I\alpha - Iy}{2} \qquad I_{d2} = \frac{I\alpha + Iy}{2} \quad (7)$$

[1] **Sánchez-López holds a scholarship from CONACyT.**

Since $Iy = (Ix - Iu)$, equation (6) results in

$$Ir = \frac{(Ix - Iu)^2}{4I\alpha} \quad (8)$$

M6-M7 mirror Ir to M7, they form a basic Translinear Loop [4]. Ir is used to develop the exponential realization of equation (1).

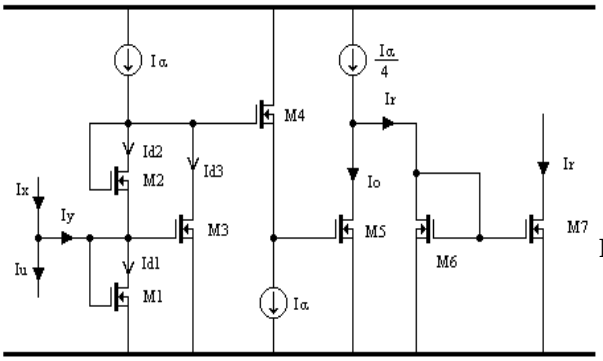

Figure 1. A current-mode quadrature-circuit.

3.2 Circuits for Realizing GFs

Several topologies based in BJTs has been presented in [4]. That topologies can be replaced by MOSTs, as shown in Fig. 2. As one sees, Ir flows through the resistor where:

$$Vg = Rg * Ir \quad (9)$$

Then, Vx is: $Vx = V_{GS1} - RgIr$ (10)

$$V_{GS1} = V_{TH1} + nVt * Ln\left(\frac{I_G}{\left(\frac{W}{L}\right)_{M1} I_{DOM1}}\right) \quad (11)$$

M2 converts Vx into a current expressed by

$$I_0 = \frac{\left(\frac{W}{L}\right)_{M2} I_{D0M2}}{\left(\frac{W}{L}\right)_{M1} I_{D0M1}} I_G e^{\left(\frac{V_{TH1} - V_{TH2} - RgIr}{nVt}\right)} \quad (12)$$

If M1=M2, equation (12) is reduced to

$$I_0 = I_G e^{\left(\frac{-RgIr}{nVt}\right)} \quad (13)$$

Using (8) in (13) it results in

$$I_0 = I_G e^{\left(\frac{-Rg}{4nVt}\left(\frac{(Ix-Iu)^2}{I\alpha}\right)\right)} \quad (14)$$

An implementation using a grounded resistor, is shown in Figure 3. Ir flows trough R, M2 converts this voltage into a current given by (13). Using (8), one get (14) again. Equation (14) is modeling a gaussian-window with parameters controlled by current sources. I_G and Iu control the peak-gain and mean-value or translation-parameter. $I\alpha$ controls the scale or standard deviation.

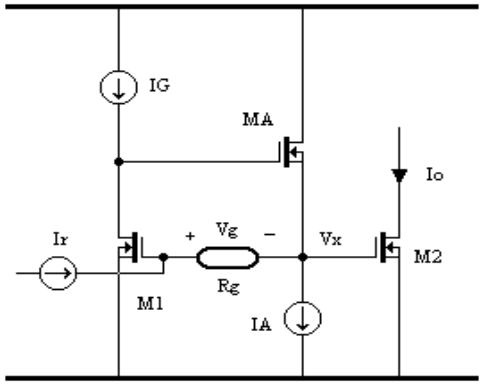

Figure 2. GF using a floating resistor.

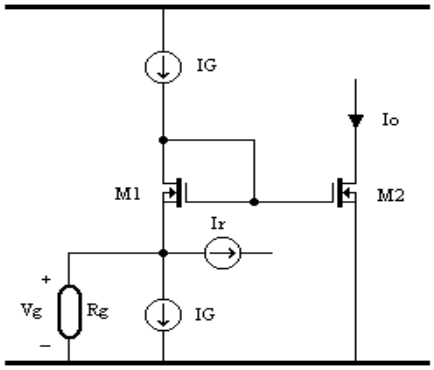

Figure 3. GF using a grounded resistor.

3.3 Active Resistors.

Using the TP, one may design active resistors, as shown in Figure 4. The input-signal is extended through the differential-pairs, reducing the unbalanced voltage. The input resistance is:

$$R_{in} = \frac{4nVt}{I_B} \quad (15)$$

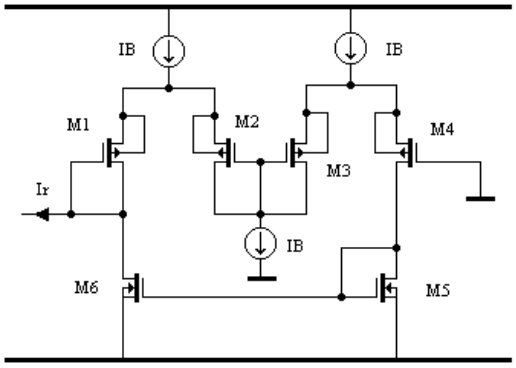

Figure 4. Active Resistor with high linearity.

Using (15) in (14), one get the current of the GF. If I_B is proportional to the scale control-current

$\left(IB = \frac{I\alpha}{4}\right)$, one get: $I_0 = I_G e^{-\left(\frac{2*(Ix-Iu)}{I\alpha}\right)^2}$ (16)

3.4 Energy Normalization

To preserve the energy of the gaussian-window, the output-current is adjusted by varying the scale factor stated in equation (1); then I_G must be proportional to $\frac{1}{\sqrt{I\alpha}} = \frac{1}{\sqrt{S}}$. An efficient scheme for low-voltage applications is shown in Figure 5 [4]. The resulting GF normalized in current-mode is represented by

$$I_0 = \sqrt{\frac{I_1^3}{I\alpha}} e^{-\left(\frac{2*(Ix-Iu)}{I\alpha}\right)^2} \quad (17)$$

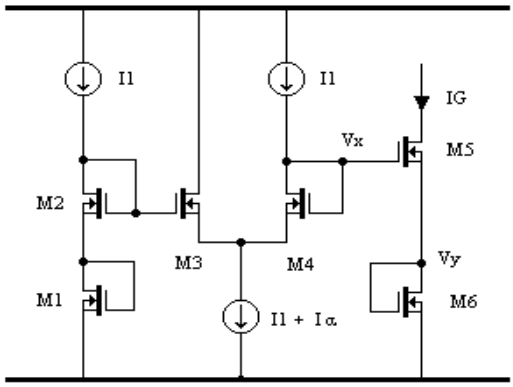

Figure 5. Generating I_G at low-voltage.

4 Body Effect

The circuit shown in Figure 1, presents higher deviation due to the BE. An improved design is shown in Figure 6. The offset generated by the BE is reduced by adding a current-controlled current-source in the gate of M5. Since Iy varies according to (5) the current in M4 also varies, and the offset is reduced.

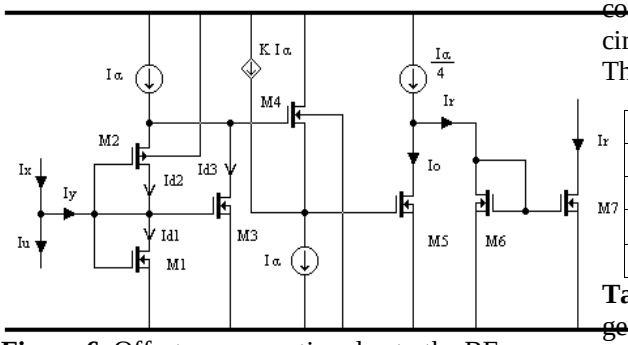

Figure 6. Offset compensation due to the BE.

M2 is changed by a PMOST but keeping the TP, because the NMOST produces a nonlinearity in the output-current. The drain current of the MOSTs that do not suffer the BE are modeled using equation (4), the ones presenting the BE are modeled by

$$I_D = \frac{W}{L} I_{DO} A_{BS} e^{\left(\frac{V_{GS}-V_{TH}}{nVt}\right)} \quad (18)$$

$A_{BS} = e^{\frac{(n-1)V_{BS}}{nVt}}$ increments the drain current due to the BE, tending to 1 when $V_{BS} \to 0$.

Another circuit minimizing the offset is shown in Figure 7. From the offset presented at the output current, the voltage at node x is varying when Iy takes values according to (5). MA stabilizes node x as Iy becomes varying.

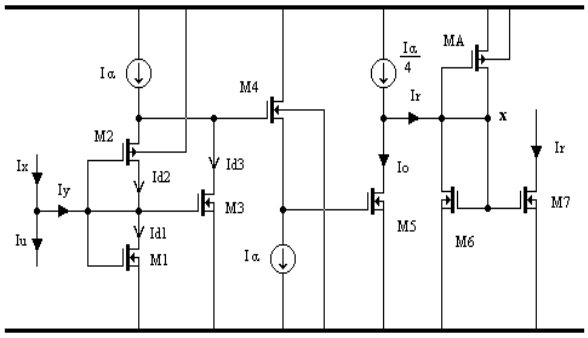

Figure 7. Modification of the quadrature circuit

5 GAUSSIAN FUNCTION

The proposed design of the circuit generating GFs, implemented in a standard CMOS technology, was realized using a technology of a single-well for 0.6um of AMS.

5.1 Implementation

In Figure 8 it is shown the circuit generator of the GF, while in Table 1 are shown the ranges of the input current. The proposed circuit is composed of three basic blocks, namely: The circuit of quadrature, The active resistor, and The circuit generator of the GFs.

VDD	1.5V
Power Consumption	0.843uW
I_G	10n-60n
Iα	40n-80n
Iy	(-80n)-(+80n)

Table 1. Biasing conditions for the circuit generator of a GF.

In Figure 9 is shown the circuit generator of the GF being normalized, while in Table 2 are shown the ranges of the control-currents. This

circuit is composed of four blocks: The three blocks listed above plus a generator for I_G.

V_{DD}	1.5 V
Power consumption	1.534 μW
Iα	40n -- 160n
Iy	-160n -- 160n
I1	40n

Table 2. Biasing conditions for the circuit generator of the normalized GF.

5.2 Simulation Results

In Figure 10 are shown the simulation results of the circuits shown in Figures 6 and 7. As one sees from Figure 10.b, while the proposed configuration does not reduce completely the offset, it is controlled within an acceptable range. The simulation result of the GF being normalized, is shown in the Figure 11. Finally, the result by making a translation by varying Iu is shown in Figure 12. The ranges of the control currents are listed in Tables 1 and 2. Ix and Iu must be kept within the range imposed by Iy.

6 CONCLUSIONS.

Along the paper it was discussed the design of a low-voltage circuit suitable for the realization of GFs by applying the TP, using MOSTs biased in weak-inversion. The proposed design was realized using a standard CMOS technology of 0.6um of AMS having a single-well. To realize the quadrature function, a circuit oriented to compensate the offset due to the BE of the MOSTs, was proposed.

The two proposed circuits, to normalize the energy in the implementation of the normalized GF, are fully-programmables using control-currents which are listed in Tables 1 and 2. Finally, simulation results using Hspice validate theoretical developments.

7 REFERENCES

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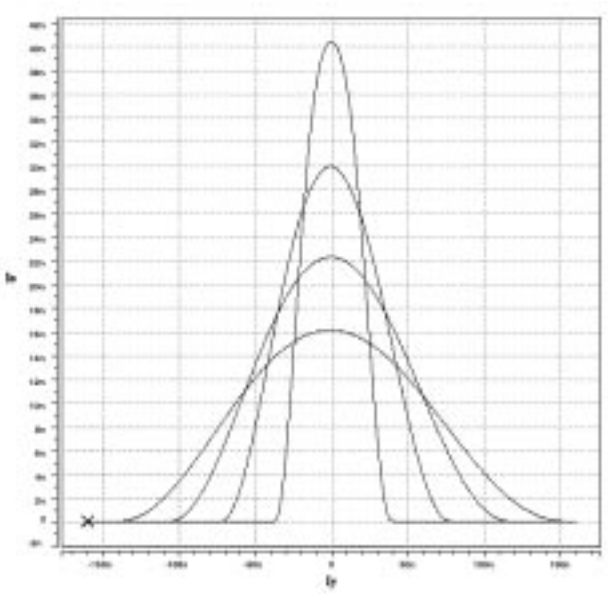

Figure 11. Simulation results of the normalized GF

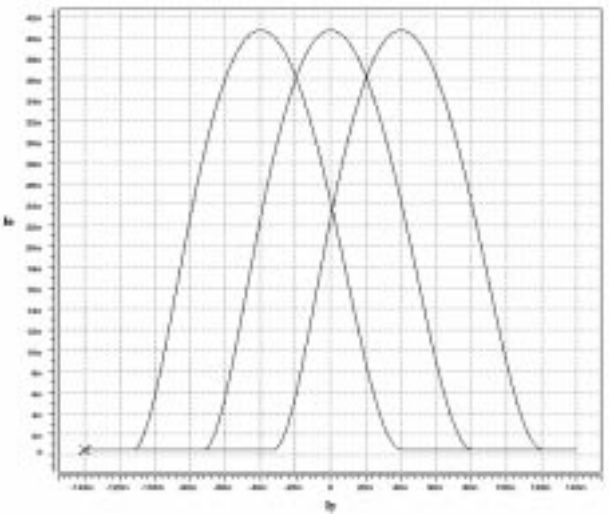

Figure 12. Simulation results due to the translation

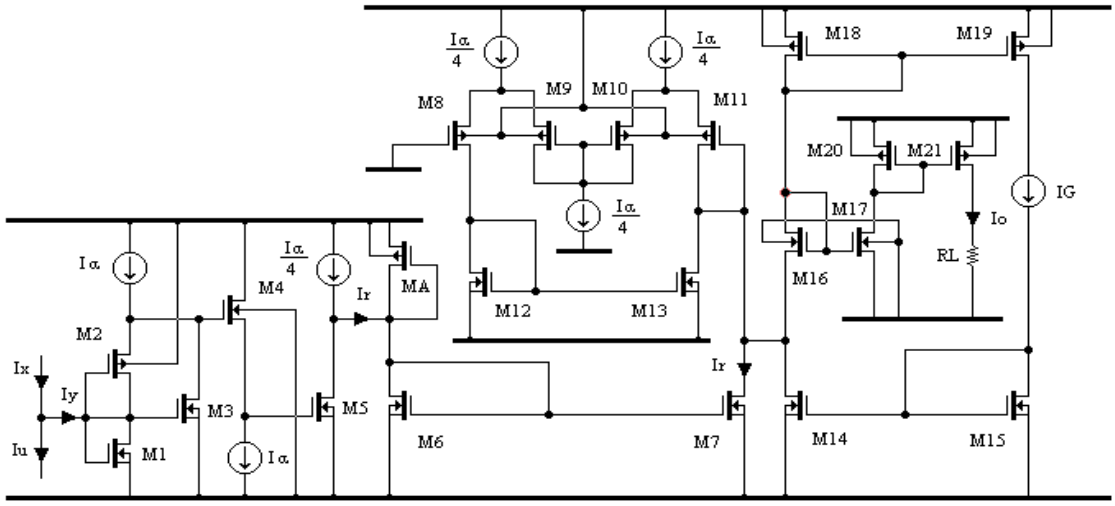

Figure 8. Proposed circuit for the realization of a GF implemented in a standard CMOS technology.

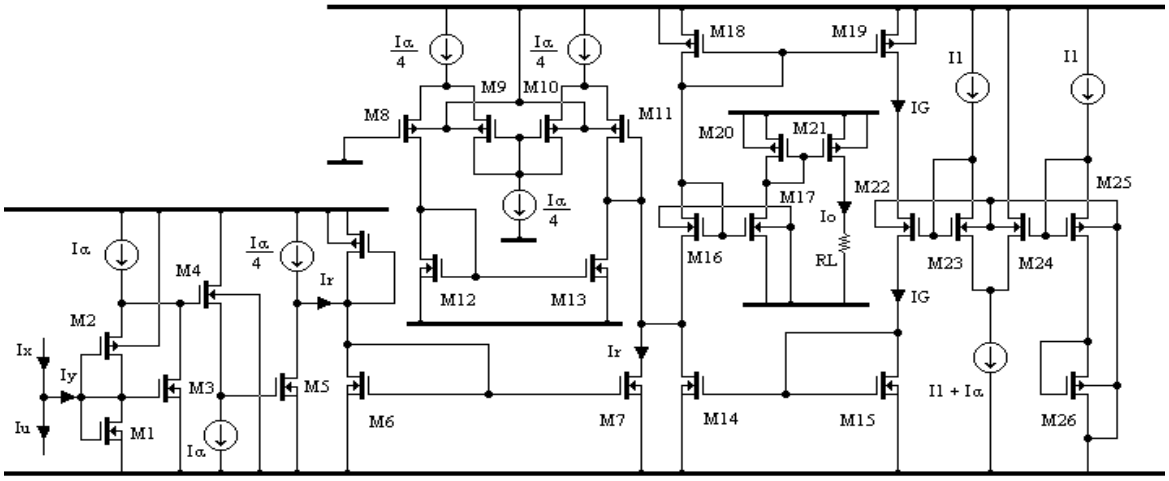

Figure 9. Proposed circuit for the realization of a normalized GF.

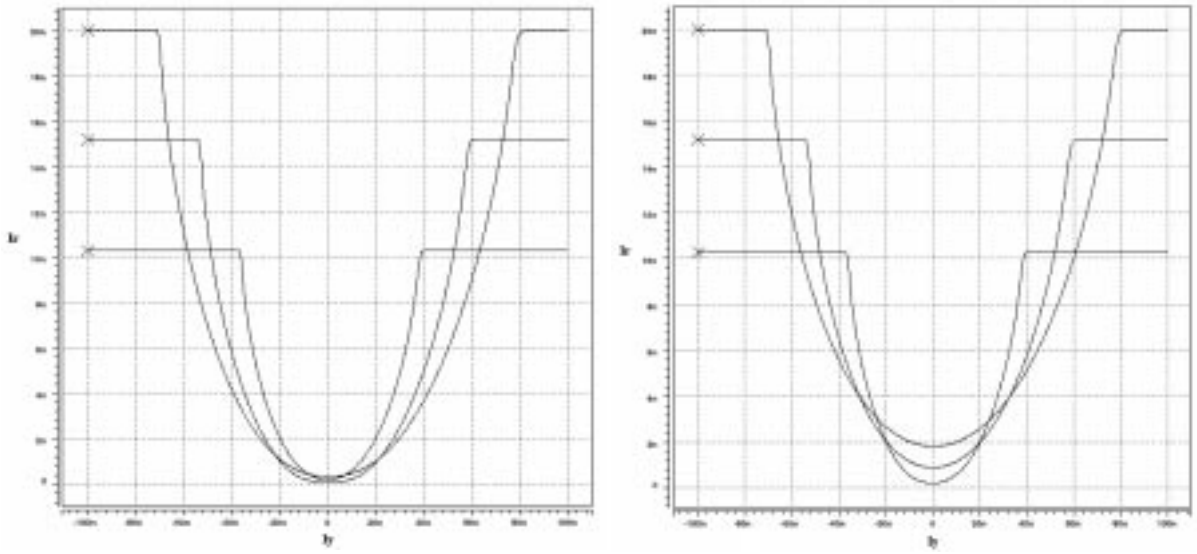

Figure 10. Circuit of quadrature: (a) Compensating the offset and (b) Controlling the voltage at the drain of M5.