A Fully Integrated CMOS PLL for Frequency Synthesizer using Gm-C Filter

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Abstract: - This paper describes a fully integrated CMOS phase-locked loop (PLL) with a transconductance-C (Gm-C) filter. This PLL is used in consumer implemented in the 0.5 μm CMOS technology without the need of any external component. The resulting layout area and the power dissipation of the whole PLL are mm^2 and mW respectively.

Key-Words: - Phase-Locked Loop, Operational Transconductance Amplifier, Gm-C Filter.

1 Introduction

Due to the rapid development of the microprocessor and computer industries in the past years, the digital CMOS process becomes very mature. Compared to other available processes, the digital CMOS process has the strong advantages of low cost and high density. Standard digital CMOS process is more attractive over other technologies because of the possibility to offer the lowest cost solution. Moreover, CMOS technology has the potential to realize the addition of digital function with the front-end circuit. Owing to the serious high-frequency parasitic effects and high noise of standard digital CMOS process, all-CMOS transceivers were only recently implemented. However, the fully integrated CMOS solution of some systems such as GSM and DCS is still an active research topic. Due to the close separation between the channels in wireless communication systems, RF synthesizers employed in wireless transceivers have very stringent accuracy specification and have restrictive phase noise requirements to reduce the effect of other large blocking signals. The high frequency operation and the stringent requirements pose big design challenges on the design of on-chip CMOS synthesizers. The growing density and performance of the sub-micro CMOS process make the process to be a very attractive candidate for the radio-frequency integrated circuits.

Electronic filters are used in virtually all communication and signal processing circuitry. There are two main techniques for realizing integrated analog filters. One technique is the use of switched-capacitor, the second approach is continuous-time filter. Switched-capacitor filters are unsuited to process high-frequency signal. As a result, the more popular for realizing integrated analog filters is continuous-time filtering[1]-[4].

2 Architecture

Fig. 1 shows the block diagram of a conventional Phase-Locked Loop. The PLL consists of a phase frequency detector (PFD), a voltage controlled oscillator (VCO), a programmable divider, a charge pump and a loop filter. The VCO output frequency f_{vco} is divided by the frequency divider. This divided signal is compared to the reference signal, f_{Ref}, in the PFD, which gives output signals, UP and DN, equal to the phase difference between its two inputs. Through the charge pump circuit and loop filter, the signals are low-pass filtered by the loop filter, and are converted to be the controlled input of the VCO, adjusting the VCO output frequency. When the loop is locked, the two inputs of the phase detector have a constant phase relationship and thus equal frequency.

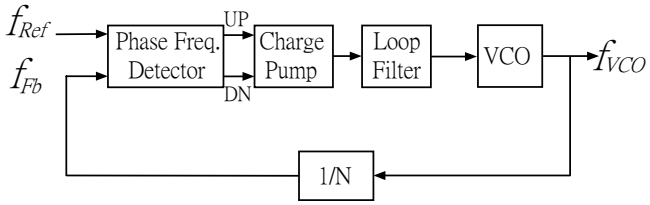

Fig.1 Block diagram of a conventional PLL.

We proposed a novel PLL structure, additionally adding a signal path of the PLL shown in Fig. 2 The idea is that the Path 1 is established by the loop filter and the Path 2 is a provision for the Gm-C filter.

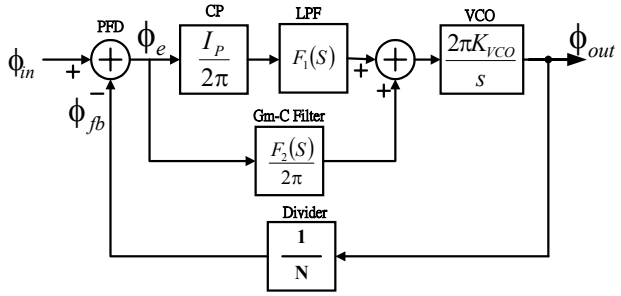

Fig.2 Linear model of PLL with Gm-C filter.

The open-loop transfer function can be represented as

$$G(s)=\left[\frac{I_p}{2\pi}\cdot F_1(s)+\frac{1}{2\pi}F_2(s)\right]\cdot\frac{2\pi K_{vco}}{s}\cdot\frac{1}{N} \qquad (1)$$

Here, $F_1(s)$ is the transfer function of the passive filter and $F_2(s)$ is the one of the Gm-C filter. In this design, we employ a capacitor to be the first-order loop filter. In order to make sure the loop will be stable under the first-order filter, we must analyze the open-loop frequency response; the simulation result is shown in Fig.3.

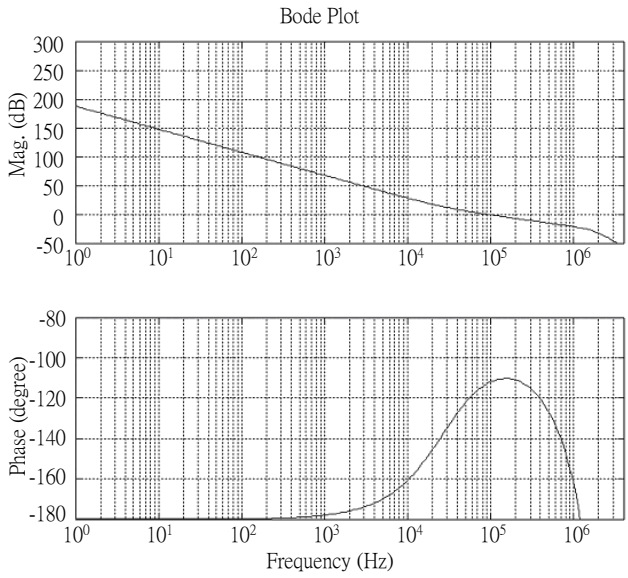

Fig.3 The PLL corresponding open-loop response.

3 Gm-C Filter Design

The main circuit building blocks of Gm-C filters are transconductor. A transconductance (Gm) cell is voltage to current converter, which converts input AC voltage to output current variation. An OTA is a voltage controlled current source. High-order filters can be obtained by cascading biquads and either with or without a first-order section depending on whether the order of the filter is even or odd. In this design, a 3rd-order lowpass Gm-C filter is implemented. This filter achieves a 40-dB/decade in the stopband. Also, the frequency response is maximally flat in the passband for this filter. The fully differential third-order lowpass Gm-C filter is shown in Fig. 4 [5][6]. The transfer function of this Gm-C filter is given by:

$$\frac{V_{out}}{V_{in}}=\frac{Gm_1Gm_4Gm_6}{F_2(s)} \qquad (2)$$

where

$$F_2(s)=C_1C_2C_3s^3 + (C_2C_3Gm_2+C_1C_2Gm_7)s^2 + (C_1Gm_5Gm_6+C_2Gm_2Gm_7+C_3Gm_3Gm_4)s + (Gm_2Gm_5Gm_6+Gm_3Gm_4Gm_7)$$

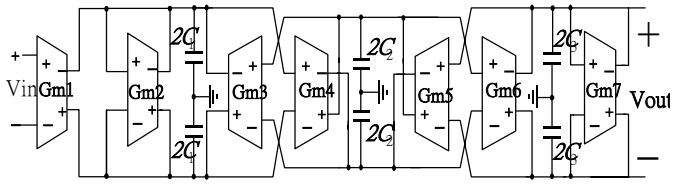

Fig. 4 The configuration of 3rd-order lowpass Gm-C filter.

Parasitical capacitances in our filter may cause linearity problems since these capacitances are partially nonlinear. Besides, the parasitic input and output capacitances of the transconductor are no longer negligible compared with the integrating capacitors that we adopted in the filter. This parasitic effect will affect the transfer function of the filter and change the locations of the poles. To reduce the effects of these parasitic capacitances, two approaches are used.

One approach to solve this problem is estimating these parasitical and taking them into account in designing the values of capacitors of the gm-C stage. Yet, the problem with this approach is that the parasitical depend on process parameters and temperature, so their values are difficult to be predicted accurately. Another approach is to make all the capacitances of all the nodes the same by construction, including parasitic capacitances, by adding appropriate dummy devices. However, this method needs different transconductances for each OTA. And it needs more chip area and consumes more power. In this design, we will use the second approach.

In this design, all the C's are the same (i.e. C1 = C2 = C3 = C), and equation (2) becomes below:

$$\frac{V_{out}}{V_{in}} = \frac{Gm_1 Gm_4 Gm_6}{F_2'(s)} \qquad (3)$$

Where $F_2'(s) = C^3 s^3 + C^2(Gm_2+Gm_7)s^2 + C(Gm_3Gm_4+Gm_5Gm_6+Gm_2Gm_7)s + (Gm_2Gm_5Gm_6+Gm_3Gm_4Gm_7)$

We can decrease the capacitance in order to increase the pole frequency. Therefore, for realizing high-frequency poles and zeros, the integrating capacitors are small. We may increase the transconductance to achieve the same result, but higher Gm is usually associated with larger input device. Here, in this design, the total current consumed by the filter is 80μA. The total power dissipation of the third-order Gm-C lowpass filter is 410μW. Fig.5 show the frequency response of the Gm-C filter in HSPICE simulations.

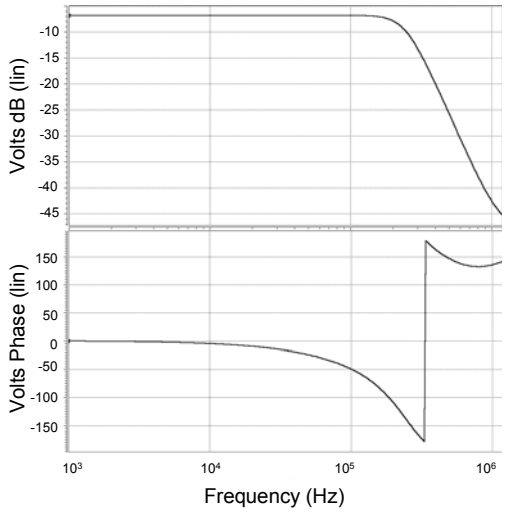

Fig.5 The magnitude phase response of the Gm-C filter.

4 Simulation and Discussion

The discrete-time characteristic and some other effects such as pull-in process of a charge-pump PLL can be observed through this behavior model for the complete PLL is implemented in *Simulink*[7]. Fig. 6 shows a typical simulation result by this model.

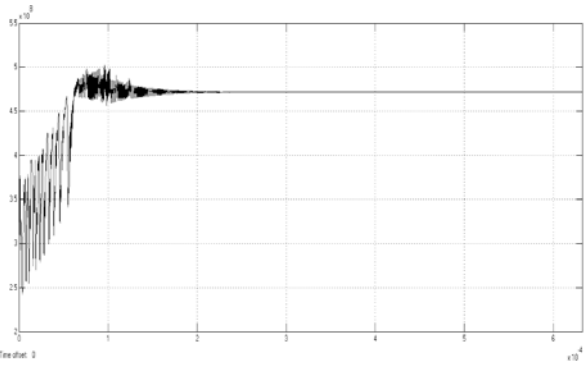

Fig. 6 Simulation result by *Simulink*.

5 Conclusion

In this work, we proposed a fully integrated CMOS Phase-Locked Loop (PLL) with transconductance-C (Gm-C) filters. The PLL architecture contains two loop filters, one is passive filter and the other one is Gm-C filter. The PLL was realized in a 0.5 μ m CMOS technology, and the layout topology as shown in Fig.7, the operation frequency is 434MHz, and the core circuit dissipates 150mW from a 5-V power supply. This PLL LSI is suitable for consumer electronics, such as wireless headset or wireless audio equipment, to help minimize the number of external components.

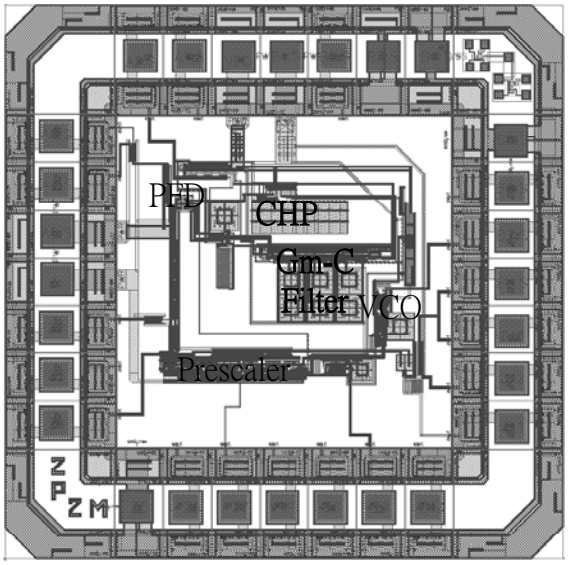

Fig. 7 The layout of the PLL.

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