A ZVS PWM Inverter With Voltage Clamping Technique Using Only a Single Auxiliary Switch

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Abstract: - This paper presents a zero-voltage (PWM) inverter with active voltage clamping technique using only a single auxiliary switch. The structure is particularly simple and robust. It is very attractive for single-phase high power applications. Conduction and switching losses are reduced due to implementation of the simple active snubber circuit, that provides ZVS conditions for all switches, including the auxiliary one. Its main features are: Simple control strategy, robustness, lower weight and volume, lower harmonic distortion of the output current, and high efficiency. The principle of operation for steady-state conditions, mathematical analysis and experimental results from a laboratory prototype are presented.

Key-Words: - Single Phase Inverter, Soft Commutation, Voltage Clamping Technique

1 Introduction

Many efforts have been made by the researchers all over the world, in the attempt to reduce the harmonic distortion and the audible noise in the output of the inverters. These objectives have been attained with the increase of the inverter commutation frequencies and an appropriate modulation strategy. These measures give some benefits like the reduction of the weight and volume of the magnetic elements; nevertheless they cause some difficulties due to the high commutation losses in the switches and the electromagnetic interference appearing. These factors occur mainly in inverter topologies that use the bridge inverter configuration. At the moment that the main switch turns on, the anti-parallel diode of the bridge complementary switch begins its reverse recovery phase. During this stage the switches are submitted to a high current ramp rate \( (di/dt) \) and a high peak reverse recovery current \( I_r \). Both contribute significantly to the increasing of the commutation losses and produce electromagnetic interference.

To solve this problem, diverse works had been developed by the scientific community in the last years and can be divided in two groups: Passive Techniques and Active Techniques. The passive techniques are characterized for the absence of controlled switches in the circuit of aid to the switching, while the active techniques are characterized for circuits that use controlled switches. Amongst the passive solutions, perhaps the most known and spread out it is of Underland snubber [1]. This snubber presents a good performance in the majority of its applications, but it is not capable to regenerate the lost energy in the switching. To try to minimize these losses, some works consider modifications in the snubber of the Underland aiming at the regeneration of the lost energy in the switching [2], [3], [4] and [5]. Already, the active solutions distinguish by the use of controlled switches to obtain soft commutation. The main ones are that use conventional modulation PWM without the necessity of special circuits of control. One of these works is the inverter ARDPI [6]. This topology matches the use of modulation PWM with the attainment of the soft switching through a relatively simple circuit. On the other hand, it needs a high current circulating in the circuit, about 2.5 times the load current, raising the current stress in the switches. A very similar topology to the previous one is ARPI (Auxiliary
Resonant Pole Inverter) [7]. Theoretically this circuit reduces the necessary current levels to get the switching, but it implies in a complex strategy of control. Another circuit found in literature is the ARCPI (Auxiliary Resonant Commutated Pole Inverter) [8], [9] and [10]. This inverter have auxiliary switches who are only turned on when the load current is not enough to effect the soft switching, becoming the control circuit very complex and dependent of the sensors.

Recently, some researches were made using the reverse-recovery energy from the diodes to obtain soft commutation in the switches of the pre-regulated rectifiers with high power factor [11] and [12]. In this paper a ZVS PWM inverter with voltage clamping across the switches, using only a single auxiliary switch, is presented. The proposed structure uses the diode reverse recovery energy technique to obtain soft commutation in all switches, such as the rectifier shown in reference [12].

2 Proposed Circuit

The proposed circuit is shown in Fig. 1. It presents a half bridge inverter configuration, where \( Q1, Q2 \) are the main switches.

The snubber circuit is formed by one switch \( Qa \), one small center-tapped inductor \( Ls1, Ls2 \) and one capacitor \( Cs \). \( C1, C2 \) and \( Ca \) are the commutation capacitors. The capacitor \( Cs \) is responsible for the storage of the diode reverse recovery energy and for the clamping of the voltage across the switches. The inductors \( Ls1 \) and \( Ls2 \) are responsible for the control of the \( di/dt \) during the diode reverse recovery time.

![Fig. 1. Proposed Circuit.](image)

3 Operation Stages (For The First Half Cycles)

To simplify the analysis, the following assumptions are made: the operation of the circuit is steady state; the components are considered ideal; the voltage across the capacitor \( Cs \), and the current in the output inductor \( Lout \) are considered constant during the switching period.

In the following paragraphs the operation stage of the first positive half cycle of the output current is described in detail.

First stage (t0-t1): During this interval the output current \( Iout \) is increasing, and delivering energy to the source \( V2 \) via diode \( D2 \). At the same time, the additional current \( i_{Ls1} \) flows around the mesh, formed by \( Ls2, Qa, Cs \), and \( Ls1 \).

Second stage (t1-t2): This stage starts when the auxiliary switch \( Qa \) is blocked. The current \( i_{Ls1} \) charges the capacitor \( Ca \) from zero to \( E+V_{Cs} \), and discharges \( C1 \) from \( E+V_{Cs} \) to zero.

Third stage (t2-t3): At this stage the voltage across \( C1 \) reaches zero, and it is clamped by diode \( D1 \). At this moment, the voltage \( E = V1+V2 \) is applied across the inductors \( Ls1 \) and \( Ls2 \), and the currents \( i_{Ls1} \) and \( i_{Ls2} \) decrease linearly.

Fourth stage (t3-t4): It begins when the current \( i_{Ls1} \) inverts its direction and flows through the switch \( Q1 \). The current \( i_{Ls2} \) continues to decrease until inverting its direction, and begins the reverse recovery phase of the diode \( D2 \). The inductor \( Ls2 \) limits the \( di_{Ls2}/dt \).

Fifth stage (t4-t5): This stage starts when the diode \( D2 \) stops conducting. The current \( i_{Ls2} \) begins the charge of the capacitor \( C2 \) from zero to \( E+V_{Cs} \) and the discharge of \( Ca \) from \( E+V_{Cs} \) to zero.

Sixth stage (t5-t6): At this stage the voltage across the capacitor \( Ca \) reaches zero, and is clamped by diode \( Da \). The currents \( i_{Ls1} \) and \( i_{Ls2} \) increase, due the application of the voltage \( V_{Cs} \) across the inductors \( Ls1 \) and \( Ls2 \).

Seventh stage (t6-t7): This stage begins when the current \( i_{Ls2} \) changes its direction and flows through switch \( Qa \). The current \( i_{Ls1} \) continues to increase linearly.
Eighth stage (t7-t8): At this stage the switch $Q1$ is blocked, and the current in $Cs$ inverts its direction and flows through the diode $Da$. The capacitor $C1$ charges itself from zero to $E + V_{Cs}$ and the capacitor $C2$ discharges from $E + V_{Cs}$ to zero.

Ninth stage (t8-t0): It begins when the voltage across the capacitor $C2$ reaches zero, and is clamped by the diode $D2$. The current $i_{Ls1}$ continues increasing. This stage finishes when $i_{Ls1}$ inverts its direction, and flows through the auxiliary switch $Qa$, restarting the first operation stage.

For the second half cycle the operation stage is analogous and can be described in an identical way. The main operation stages are show in Fig.2. The Fig. 3 shows the main waveforms.

4 Mathematical Analysis of the Commutation

To guarantee ZVS conditions, it is necessary, in the second stage, that the stored energy in the inductor $Ls=Ls1+Ls2$ be sufficient to discharge the capacitor $C1$ and to charge $Ca$. Thus, by inspection of Fig. 3 (Interval t1-t2) the following condition can be formulated:

$$Ls \cdot I_{fs}^2 \geq (Ca + C1)(E + V_{Cs})^2$$  \hspace{1cm} (1)

where $I_{fs}$ is the maximum current in $Ls2$. $V_{Cs}$ is maintained constant during a switching period. Assuming $V_{Cs} \ll E$ we have:

$$I_{fs} \text{min} \geq E \sqrt{\frac{Cl + Ca}{Ls}}$$  \hspace{1cm} (2)

It is necessary to know the clamping voltage behavior for the design of the switches and capacitor $Cs$.

In steady state conditions, the clamping capacitor average current must be zero. Thus:

$$i_{Cs_{av}} = \frac{1}{T_s} \int_0^{T_s} \left[ \frac{V_{Cs}}{Ls} \cdot t - Ir \right] dt + \int_0^{T_s} \left[ \frac{V_{Cs}}{Ls} \cdot t - I_{out} - Ir \right] dt$$  \hspace{1cm} (3)

where $T_s$ is the switching period.

Solving the integral equation, and considering:

$$D = \frac{t1}{T_s}$$  \hspace{1cm} (4)

$$t1 = Ts$$  \hspace{1cm} (5)

$$i_{Cs_{av}} = 0$$  \hspace{1cm} (6)

We have:

$$V_{Cs} = \frac{2Ls}{Ts} \left[ Ir + I_{out} \cdot (1 - D) \right]$$  \hspace{1cm} (7)

Let us take the load current in shape to a sinusoidal function and in phase with the output voltage. Thus:

$$I_{out} = \frac{E \cdot ma}{2 \cdot Z_{out}} \cdot \sin \omega t$$  \hspace{1cm} (8)

where $Z_{out}$ is the load impedance.

The duty cycle $D$ can also be defined by expression 9:

$$D = \frac{ma \cdot \sin \omega t}{1}$$  \hspace{1cm} (9)

where $ma$ represents the amplitude modulation factor.

Combining Eqs. 7, 8 and 9 we obtain the expression of the $V_{Cs}$ voltage, given by (10):

$$V_{Cs}(t) = \frac{2Ls}{Ts} \left[ Ir + \frac{E \cdot ma}{2 \cdot Z_{out}} \cdot \sin \omega t \cdot (1 - ma \cdot \sin \omega t) \right]$$  \hspace{1cm} (10)

where $Ir$ is the peak reverse recovery current of the anti-parallel diode, which can be given by (11).

$$Ir = \sqrt{\frac{4}{3} \cdot Q_{rrr} \cdot \frac{E}{Ls}}$$  \hspace{1cm} (11)

$Q_{rrr}$ represents the Reverse Recovery Charge of the diode.

From the analysis of the current behavior in the capacitor $Cs$, the expression of the current $I_{fs}$ can be obtained :

$$I_{fs}(t) = \frac{V_{Cs}}{Ls} \cdot Ts - I_{out} - Ir$$  \hspace{1cm} (12)

Combining Eq. 10 with Eq. 12 and making some simplifications we obtain the expression that represents the evolution of the current $I_{fs}$. 
To guarantee ZVS condition in all load range the minimum value of the current $I_f$ obtained from Eq. 13 must be bigger than the value obtained from Eq. 2.

$$I_f(t) = I_r + \frac{E \cdot ma}{2 \cdot Z_{out}} \sin \omega t - \frac{E \cdot ma^2}{Z_{out}} \sin^2 \omega t$$ (13)

5 Design Example

5.1 Input Data

$E = 400V$ \hspace{1cm} Bus Voltage

$V_{out} = 127$ V \hspace{1cm} RMS Output Voltage

$P_{out} = 1000$ VA \hspace{1cm} Output Power

$I_{out} = 7.88$ A \hspace{1cm} Output Current

$f_s = 20$ KHz \hspace{1cm} Switching Frequency

$f = 60$ Hz \hspace{1cm} Output Frequency

$L_{out} = 2.5$ mH \hspace{1cm} Load Inductance

$R_{out} = 16$ $\Omega$ \hspace{1cm} Load Resistance

$ma = 0.9$ \hspace{1cm} Modulation Factor
5.2 Calculation of the Auxiliary Inductor

The auxiliary inductors are responsible for the $di/dt$ limit during the turn off of the main diodes. The $di/dt$ is directly related with the peak reverse recovery current $I_r$ of the anti-parallel diodes. A “snappy” $di/dt$ produces a large amplitude voltage transient and contributes significantly to Electromagnetic Interference.

In the design procedure it is chosen a $di/dt$ that is usually find in the diode data book. This is a simple way to obtain the diodes fundamental parameter for the design of the inverter. In such case the $di/dt$ chosen for this example was 40A/$\mu$s. We know that the external circuit determines the current ramp rate, thus:

$$L_s = \frac{E}{\frac{400V}{40 \frac{V}{\mu s}}} = 10 \mu H$$

The auxiliary inductors are given by:

$$L_{s1} = L_{s2} = \frac{L_s}{2} = 5 \mu H$$

5.3 Load Impedance

The load impedance is obtained from Eq. 16.

$$Z_{out} = \sqrt{40^2 + 40^2} = 40 \sqrt{2} \approx 56.6 \Omega$$

5.4 Diode Choose

For the performance of the inverter it is important to choose a slow diode. So, we opt to use the body diode of the MOSFET IRFP460, which has the following characteristics:

- $V_{dss} = 500V$  Maximum Reverse Voltage
- $I_s = 20A$  Diode Average Current
- $Q_{rr} = 5.7\mu C$  Reverse Recovery Charge

5.5 Switching Period

$$T_s = \frac{1}{f_s} = \frac{1}{20 KHz} = 50 \mu s$$

5.6 Reverse Recovery Current

The reverse recovery current is given by the Eq. 11.

$$I_r = \frac{4}{3} \cdot 5.7\mu C \cdot \frac{400V}{10\mu H} = 17.4A$$

5.7 Capacitor Clamping Voltage Behavior

Using a Eq. 10 the curves described in Fig. 4 are obtained.

For $Z_{out}=16\Omega$ and $ma=0.9$, the maximum clamping voltage is 8V.

We can observe that the voltage increment across the switches is smaller than conventional inverter.

5.8 Current $If$ Behavior
The current $I_f$ behavior, obtained from Eq. 13 and Eq. 2, can be seen in Fig. 5.

It is observed that the current $I_f$ has a minimum point that is located in $\pi/2$, and the intensity of the current diminishes with the increase of the load. To guarantee ZVS condition in all load range, the minimum value of the current $I_f$, obtained from Eq. 13, must be bigger than the value of the traced straight line from Eq. 2.

![Graph showing current behavior](image)

Fig. 5. Current $I_f$ Behavior.

### 6 Experimental Results

An inverter prototype rated 1.5kVA operating with PWM commutation was built to evaluate the proposed circuit. The main specifications and components are given below:

#### 6.1 Prototype Specifications

- **$P_{out}$** = 1500 W (Output Power)
- **$E$** = 400V (Bus Voltage)
- **$V_{out}$** = 127V (Rms Output Voltage)
- **$f$** = 60Hz (Output Frequency)
- **$f_s$** = 20 kHz (Switching Frequency)
- **$Q_1$, $Q_2$, $Q_a$** (IGBT IRG4PC50W)
- **$D_1$, $D_2$, $D_a$** (Mosfet Body Diode IRFP460)
- **$C_1$, $C_2$, $C_a$** (Components Intrinsic Capacitance $\approx 8nF$)
- **$L_{s1}$, $L_{s2}$** (5uH each; Ferrite Core EE30/7; N=16 turns, 13 wires #20AWG)
- **$C_{s}$** (220uF/35V; Electrolytic Capacitor)
- **$L_{out}$** (2.5mH, Output Inductor)
- **$R_{out}$** (16Ω; Output Resistor)

#### 6.2 Experimental Waveforms

In the figures presented below we can observe the experimental waveforms obtained from the laboratory prototype. Figs. 6, 7 and 8 show the voltage and current in the switches. We can observe that for all the switches, including the auxiliary one, the commutation occurs in ZVS conditions, confirming the theoretical analysis. In Fig. 9 it can be observed the current in the commutation auxiliary inductors for a switching period. We can note a proportionality of values between the currents in both inductors. The difference between them is the load current.

The voltage across the clamping capacitor $C_s$ is shown in Fig. 10. We can note a very low voltage across $C_s$, which represents a little voltage stress across the devices. The output voltage and current are presented in Fig. 11. Fig. 12 shows the efficiency as function of the load range for both hard and soft commutation. The converter efficiency with soft commutation was improved around 5% for all load range.

![Waveforms](image)

Fig. 6. Voltage and current in Q1, D1, C1. (100V/div, 5A/div, 1us/div)
7 Conclusion
A ZVS PWM inverter with voltage clamping using a single auxiliary switch has been developed. The operation stages for steady-state condition, mathematical analysis, main waveforms and experimental e-
results were presented. The experimental results show a low voltage in the clamping capacitor. Conduction and switching losses are reduced due to the implementation of a simple active snubber circuit, that provides ZVS conditions for all the switches, including the auxiliary one. The reduced number of components and the simplicity of the structure increase its efficiency and reliability, and make it suitable for practical applications. The proposed circuit presents soft commutation for all load range, confirming the theoretical studies.

The topology presents some advantages in comparison with the conventional soft commutation inverters studied in the literature, which we can point out:

- Soft commutation in all load range;
- Simple structure with a low number of components;
- Use a classical PWM modulation;
- Auxiliary switch works with constant duty cycle in all operation stages;
- Use of slow and low cost rectifiers diodes;
- Low clamping voltage across the capacitor;
- Low current stress through the main switches;
- Simple design procedure with low restrictions;
- High efficiency.

With these characteristics, the authors believe that the proposed inverter circuit can be very useful for some industrial applications.

References