A Quantitatively Study of Threshold Voltage Fluctuation with Quantum Mechanical Models for Deep-Submicron MOSFETs

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Abstract: - In this paper, the fluctuation of threshold voltage is investigated numerically for deep-submicron n-MOSFET with various gate oxide thicknesses, channel lengths, substrate doping concentration under different bias conditions. Quantum mechanical effects are also discussed in this study. By using the ISE-DESSIS device simulator, two different device transport models, the classical drift-diffusion (DD) model and the Schrödinger-Poisson drift-diffusion (SP-DD) model, are considered to explore the variation of threshold voltage quantitatively for MOSFETs with different dimensions. It is found that there is 10-20 % difference in calculating threshold voltage between the DD and the SP-DD models. The device channel length and oxide thickness cause 2-10 % per 10 nm and 0.3-25 % per nm, respectively, shifts in threshold voltage, respectively.

Key-Words: - Threshold voltage, Quantum mechanical effects, device channel length, gate oxide thickness, doping concentration.

1 Introduction

The scaling of the MOSFET to nanoscale dimensions such as scaling of gate channel length (Lg) and gate oxide thickness (Tox), such as short channel effect, subthreshold slope, I-V characteristics and quantum effects, are the most interesting topics in the recent years. The most important parameter to model a MOSFET is its threshold voltage (VTH). It corresponds to the onset of inversion channel build-up, which means the starting of the MOSFETs operation. Hence, it has to be estimated accurately. Threshold voltage not only determines the MOSFET’s operation characteristics but also judge the function of designed circuit. Therefore, plenty of works focus on studying the definition of VTH, how to extract VTH or model VTH analytically, how to control the VTH or how to design an optimal device according to VTH.

In general, threshold voltage depends on temperature, substrate bias, channel length, drain voltage and oxide thickness [1-4]. Channel length [5, 6] and oxide thickness scaling [7, 8] result in different VTH with long channel device, reliable extraction methods of VTH have to be developed. On the other hand, as oxide thickness scaling down the roughness of the Si/SiO2 interface causes significant oxide thickness variation, which results in VTH fluctuation. Asenov et al. [8] employed a 3-D drift-diffusion (DD) simulator with density gradient (DG) quantum corrections to simulate the VTH fluctuation due to local oxide thickness variations. They mentioned that the VTH fluctuations become comparable to the fluctuations induced by random discrete dopants when devices with dimensions below 30 nm. In the oxide thickness range of 1-3 nm, the VTH fluctuations are particularly independent of the oxide thickness. As mentioned above, VTH depends on doping profiles [9-16], which is designed to avoid leakage and improve short channel effects (SCE). From the well-known VTH expression, VTH is proportional to the \( \sqrt{N_d} \), which is the concentration of dopant. As doping profile becomes more complicated, such as 2-D nonuniformly doping distribution or super halo doping profile, the relation between dopant concentration and VTH needs to be examined and reformulated. Another important aspect of VTH with dopant is the random doping effects [11], which is caused by the discrete nature of the impurity atoms. The random dopant effects also induce VTH fluctuations. Thus, scaling a device or designing a new device with channel engineering, VTH is the most important parameter to optimize the characteristics of it [16]. Besides, quantum effects cannot be ignored as a device is scaling down, it should be considered when VTH of nanoscale devices are studied [17-21].

For device engineering application, a quantitatively investigation of the quantum effects, oxide thickness, channel length, drain voltage and doping concentration on the threshold voltage should be addressed. In this work, MOSFETs with three oxide thicknesses, four channel lengths, three doping concentrations are simulated with the drift-diffusion
(DD) and the Schrödinger-Poisson drift-diffusion (SP-DD) models systematically so as to discuss the variations of $V_{TH}$ quantitatively. All simulated cases will be shown in detail later.

The remaining content of this study is given as follows. Sec. 2 briefly explains the simulation models and the computational method. Sec. 3 shows the simulation results and discussion. Sec. 4 draws the conclusion.

2 Classical and Quantum Mechanical Models

The DD and SP-DD models are employed to simulate and compare the influence of drain current with respect to oxide thickness. The three governing equations of DD model are listed as follows. The Poisson equation is

$$\nabla \cdot \nabla \psi = -q\left(p - n + N_D - N_A\right),$$  \hspace{1cm} (1)

where $\varepsilon$ is the electrical permittivity, $q$ is the elementary electronic charge, $n$ and $p$ are the electron and hole densities, and $N_D$ and $N_A$ are the number of ionized donors and acceptors, respectively. The current densities are given by:

$$J_n = -q\mu_n \nabla \phi_n$$ \hspace{1cm} (2)

$$J_p = -q\mu_p \nabla \phi_p$$ \hspace{1cm} (3)

where $J_n$ and $J_p$ are the electron and hole current density satisfying the continuous equations, $\mu_n$ and $\mu_p$ are the electron and hole mobility, and $\phi_n$ and $\phi_p$ are the electron and hole quasi-Fermi potentials, respectively. The mobility model used herein is Masetti’s model. For the SP-DD model, we include the quantization effects in the classical DD model by considering the 1D Schrödinger equation along the semiconductor substrate ($z$-direction)

$$-\frac{\hbar^2}{2m_{z,v}} \frac{\partial^2}{\partial z^2} \Psi_{j,v}(z) + E_{j,v}(z) \Psi_{j,v}(z) = E_{j,v} \Psi_{j,v}(z).$$  \hspace{1cm} (4)

Together with the 2DEG formula [22] the Eq. (4) is introduced to the self-consistent DD model. $\hbar$ is the reduced Planck constant, $E_C$ is the conduction band energy, $v$ is the band valley, $m_{z,v}$ is the effective mass for valley in quantization direction, $\Psi_{j,v}$ is the $j$-th normalized eigenfunction in valley $v$; and $E_{j,v}$ is the $j$-th eigenenergy. Solving the equations above, the device current can be directly computed. The computing flowchart is illustrated as Fig. 1. After drain current – gate voltage relation is obtained, $V_{TH}$ can be determined.

3 Results and Discussion

In the numerical studies, the influence of quantum effects, oxide thickness, channel length, drain voltage and doping concentration on the threshold voltage for n-MOSFETs are simulated by ISE-DESSIS ver. 8.0.3 [23]. For the convenience of discussion, we change a factor and keep others fixed each time. Therefore, the simulated MOSFETs may not be realistic ones. The definition of threshold voltage employed in this study is the extrapolated intercept of the linear portion of the drain current – gate voltage ($I_{DS}$-$V_{GS}$) curve with the $V_{GS}$-axis. Computational details are discussed as follows.

3.1 Channel length effects

In the simulation, the first influence factor of $V_{TH}$ is channel length. Four channel lengths, which are 90 nm, 130 nm, 180 nm and 250 nm, are considered.
The range of the drain voltage is 0 ~ 1.5 V. The substrate is uniformly doped by Boron, whose concentration is \( 1 \times 10^{18} \text{ cm}^{-3} \) and the Arsenic doping concentration of source and drain are Gaussian distribution with the peak of \( 2 \times 10^{20} \). The oxide thickness is 4 nm. Simulation results are given as Figs. 2 and 3. Figure 2 illustrates the \( V_{TH} \) under different channel length and different drain bias. The comparisons of \( V_{TH} \) between MOSFETs are given in Fig. 3. \( \Delta V_{TH} \) is defined as \( \left[ V_{TH}(L_G = 130, 180, 250 \text{ nm}) - V_{TH}(90 \text{ nm}) \right] / V_{TH}(90 \text{ nm}). \) Channel length scaling causes \( V_{TH} \) decreasing. According to the interval between any two curves, when channel length decreases, the \( V_{TH} \) decreases more rapidly. From the simulated data, \( V_{TH} \) is proportional to \( \log(L_G) \). In average, as \( L_G \) decreases 10 nm, the range of \( V_{TH} \) reduction is in \([2 \%, 10 \%]\) for both classical and quantum cases.

3.2 Oxide thickness effects

The next factor to be argued is the oxide thickness effect. Three oxide thickness are discussed, which are 2 nm, 3 nm, 4 nm. The channel length is 90 nm and the range of the drain voltage is 0 ~ 1.5 V. The substrate is still doped by Boron, whose concentration is \( 8 \times 10^{17} \text{ cm}^{-3} \) and the Arsenic doping concentration of source and drain are Gaussian distribution with the peak of \( 2 \times 10^{20} \). The oxide thickness is 4 nm. Figures 4 and 5 illustrate the simulation results. Figure 4 illustrates the \( V_{TH} \) under different oxide thickness and different drain bias. The comparisons of \( V_{TH} \) between MOSFETs are given in Fig. 5. \( \Delta V_{TH} \) is defined as \( \left[ V_{TH}(TOX = 3, 4 \text{ nm}) - V_{TH}(2 \text{ nm}) \right] / V_{TH}(2 \text{ nm}) \). \( V_{TH} \) decreases as \( TOX \) decreases. From the simulation results, the relation between \( V_{TH} \) and \( TOX \) is almost linear. When \( TOX \) decreases 1 nm, the range of \( V_{TH} \) reduction is in \([0.3 \%, 15 \%]\) for classical cases and in \([10 \%, 25 \%]\) for quantum cases. \( V_{TH} \) shifts with respect to different drain bias is still observed in Fig. 5. Fortunately, the \( V_{TH} \) almost keep the same under various drain bias when \( TOX = 2 \text{ nm} \). The range of \( V_{TH} \) shift becomes smaller with \( TOX \) scaling.

3.3 Doping concentration effects

The third effect on \( V_{TH} \) variation shown in this subsection is doping concentration. Three substrate doping concentration (\( N_A \)) are simulated. They are \( 1 \times 10^{18} \text{ cm}^{-3} \), \( 8 \times 10^{17} \text{ cm}^{-3} \) and \( 6 \times 10^{17} \text{ cm}^{-3} \). As regards the source and drain doping concentration, both of them remain the same. The channel length is 90 nm and the oxide thickness is 4 nm. The range of the drain voltage is 0 ~ 1.5 V. Simulation results are given as Figs. 6 and 7. \( V_{TH} \) increases with \( N_A \). Two relations, which are \( V_{TH} \propto N_A \) and \( V_{TH} \propto \sqrt{N_A} \), are examined. Both relations are acceptable. To identify which relation describes \( V_{TH} \) and \( N_A \) well, more simulation should be investigated. Figure 6 illustrates the \( V_{TH} \) under different substrate doping concentration and different drain bias. \( \Delta V_{TH} \) is defined as \( \left[ V_{TH}(N_A = 1 \times 10^{18}, 8 \times 10^{17} \text{ cm}^{-3}) - V_{TH}(6 \times 10^{17} \text{ cm}^{-3}) \right] / V_{TH}(6 \times 10^{17} \text{ cm}^{-3}) \). As mentioned above, MOSFETs scaling, which means \( L_G \) and \( TOX \) reduce in size, induces small \( V_{TH} \). The shortcoming can be remedied by heavy doping. \( V_{TH} \) increases \( 10 \% \sim 22 \% \), when a
$10^{17}$ cm$^{-3}$ impurity concentration is additionally doped in the substrate.

![Fig. 4. Simulated $V_{TH}$-$V_{DS}$ curves for different $TOX$ by the (a) DD model and (b) SP-DD model.](image)

**VDS [V]**

0.5 1.0 1.5

**VTH [V]**

0.30 0.32 0.34 0.36 0.38 0.40 0.42 0.44

2 nm 3 nm 4 nm

![Fig. 5. Simulated $\Delta V_{TH}$-$V_{DS}$ curves by the (a) DD model and (b) SP-DD model.](image)

**VDS [V]**

0.5 1.0 1.5

$\Delta V_{TH} (%)$

0 10 20 30 40

3 nm 4 nm

![Fig. 6. Simulated $\Delta V_{TH}$-$V_{DS}$ curves for different substrate doping concentration by the (a) DD model and (b) SP-DD model.](image)

**VDS [V]**

0.5 1.0 1.5

$\delta V_{TH}$ [V]

0.00 0.02 0.04 0.06 0.08

2 nm 3 nm 4 nm

3.4 Quantum mechanical model effects

From previous arguments, it is found that the quantum mechanical effect has a significant contribution to $V_{TH}$. To understand the influence of quantum effects on $V_{TH}$, a quantitative discussion is focused on this subsection. From Figs. 8, 9, and 10, when quantum effects are considered, $V_{TH}$ becomes large. It is because the confinement of quantization and the device needs a larger bias to turn on. In the figures, $\Delta V_{TH}$ is defined as $[V_{TH(DD model)} - V_{TH(SP-DD model)}] / V_{TH(DD model)}$ and $\delta V_{TH}$ is defined as $V_{TH(DD model)} - V_{TH(SP-DD model)}$. According to Figs. 8 and 9, quantum effects induce more reduction of $V_{TH}$ in devices with small $TOX$ or $LG$ than large ones. The reduced percentages are illustrated in Figs. 8(b) and 9(b). In an extreme case, a 16.3% roll-off is observed.

![Fig. 8. $\Delta V_{TH}$ between DD model and SP-DD model for $TOX$ where (a) is the difference and (b) is the percentage.](image)

**VDS [V]**

0.5 1.0 1.5

$\Delta V_{TH} (%)$

13 14 15 16 17

90 nm 130 nm 180 nm 250 nm

![Fig. 9. $\Delta V_{TH}$ between DD model and SP-DD model for $LG$ where (a) is the difference and (b) is the percentage.](image)

**VDS [V]**

0.5 1.0 1.5

$\Delta V_{TH} (%)$

14 16 18 20

90 nm 130 nm 180 nm 250 nm

Figure 10 is the simulation results of a device with 90 nm channel length. A heavy doped substrate can improve the phenomenon of $V_{TH}$ roll-off. If $N_A$ is
small, a reduced percentage in [13%, 16%] is found. If \( N_A \) is large enough, the reduced percentage is in the range of [3%, 12%]. Therefore, channel engineering is a good solution to prevent SCE caused by device scaling. In general, a 10% \( \sim \) 20% increment of \( V_{TH} \) is caused by the quantum effects.

\[
\begin{array}{c|c|c|c}
V_{DS} [V] & 0.5 & 1.0 & 1.5 \\
\hline
\Delta V_{TH} (\%) & 0 & 4 & 8 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c}
V_{DS} [V] & 0.5 & 1.0 & 1.5 \\
\hline
\Delta V_{TH} (\%) & 0 & 4 & 8 \\
\end{array}
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If \( N_A \) is large enough, the reduced percentage is in the range of [3%, 12%]. Therefore, channel engineering is a good solution to prevent SCE caused by device scaling. In general, a 10% \( \sim \) 20% increment of \( V_{TH} \) is caused by the quantum effects.

Fig. 10. \( \Delta V_{TH} \) between DD model and SP-DD model for \( N_A \) where (a) is the difference and (b) is the percentage.

Figures 11, 12, and 13 illustrate \( \Delta V_{TH} \) caused by quantum effects with respect to drain voltage under different \( L_G, T_{OX} \) and \( N_A \). From the three figures, when applied voltage increases, the difference of \( V_{TH} \) between classical and quantum cases will tend to a constant pattern. It is also found that \( V_{TH} \) shift depends on the applied bias and as the applied bias is getting large, the step size of shift decreases.

\[
\begin{array}{c|c|c|c}
TOX [nm] & 234 & 234 & 234 \\
\hline
\Delta V_{TH} (\%) & 0 & 5 & 10 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c}
TOX [nm] & 234 & 234 & 234 \\
\hline
\Delta V_{TH} (\%) & 0 & 5 & 10 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c|c}
LG [nm] & 90 & 130 & 180 & 250 & 90 & 130 & 180 & 250 \\
\hline
\Delta V_{TH} (\%) & 13 & 14 & 15 & 16 & 17 & 18 & 19 & 20 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c|c}
LG [nm] & 90 & 130 & 180 & 250 & 90 & 130 & 180 & 250 \\
\hline
\Delta V_{TH} (\%) & 13 & 14 & 15 & 16 & 17 & 18 & 19 & 20 \\
\end{array}
\]

4 Conclusions
In this paper, the threshold voltage fluctuation of n-MOSFETs has been explored by using the DD and SP-DD models with different oxide thicknesses, channel lengths, drain voltages, and substrate doping concentrations. Simulations have been done with ISE-DESSIS device simulator. Quantum effects induce a 16% higher threshold voltage than classical case in maximum. Oxide thickness and channel scaling cause roll-off of threshold voltage. Heavily doped substrate remedies this deficiency. Therefore, channel length, oxide thickness and doping concentration need to be considered simultaneously to design a reliable device with good operation characteristics. Of course, threshold voltage is one of the most important parameters for optimizing device structure and circuit design.

Another important phenomenon is the shift of threshold voltage induced by the applied bias. The fluctuation of threshold voltage not only causes operation characteristics of a device unstable, but also affects the reliability of the circuit comprised by the device. Controlling the threshold voltage shift is necessary when new devices are developed. Furthermore, there are still other characteristics which affect threshold voltage, such as temperature and channel width. They should be included in a further work. Ultra short channel MOSFET devices are currently under fabrication, and are compared to the simulation results.

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