

High Efficiency Sequential Switching HPWM Inverter based UPS

G.VENKATESAN, Dr. R.ARUMUGAM, M.VASUDEVAN and S.BALAMURUGAN
School of Electrical and Electronics Engineering
College of Engineering, Anna University
Chennai-600025, Tamil Nadu
INDIA

Abstract:- This paper presents ‘Sequential Switching Hybrid Pulse Width Modulation (SSHPWM) Inverter based UPS’, which describes a new methodology in the inverter control. In SSHPWM the power switches of a full bridge inverter has to be pulse width modulated at low frequency and high frequency alternatively, in the alternate cycles of operation. This proposed method provides high quality sinusoidal output with less harmonic distortion, reduced switching losses and high efficiency in UPS. In Hybrid Pulse Width Modulation method, two switches are commutated at high frequency and other two switches are commutated at low frequency. This proposed SSHPWM method overcomes the problem of unequal switching losses and equalizes the time duration of voltage and current stresses in the power switches.

Key-words: Uninterruptible Power Supply, Full Bridge Inverter, Hybrid Pulse Width Modulation, Sequential Switching

1. Introduction:

Uninterruptible Power supplies are used to supply clean and continuous power to critical loads. The UPS should provide high quality sinusoidal output voltage with reduced harmonics. The power quality of UPS is mainly decided by PWM inverter control methods. The general block diagram of a conventional UPS is shown in Fig. 1.

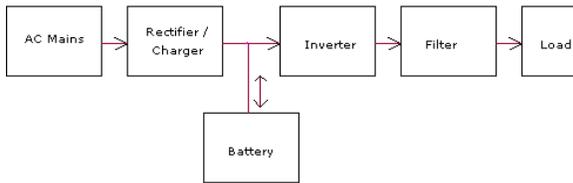


Fig.1. Block diagram for conventional UPS

The full bridge inverter shown in Fig. 2 is widely employed in various

applications, such as photovoltaic utility interface, motor drives and active filters[1]. The inverter comprises switching poles S_1/S_4 and S_2/S_3 . The switching poles are commonly controlled by various PWM techniques [3,4].

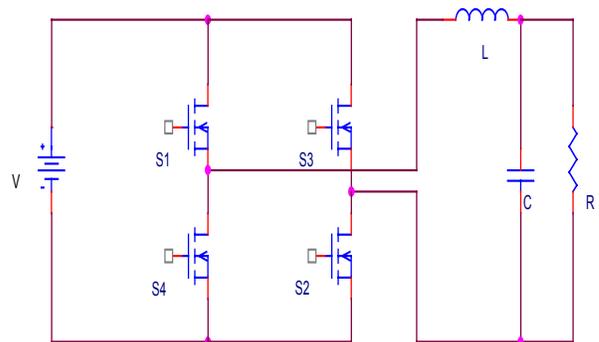


Fig.2. Full bridge Inverter

When the switching frequency is low, the switching losses are low, but

generates lower order harmonics, which are difficult to filter out. To get a high quality output with lesser total harmonic distortion, sinusoidal PWM methods are commonly used in full bridge inverters. In these PWM techniques, all switches are usually commutated at high frequency and it generates higher order harmonics, which can be easily filtered out to produce sinusoidal output.

Soft switching method for full bridge inverter have been proposed in recent years, for decreasing switching losses [5]. This method uses auxiliary switches and diodes with higher rating than the main switches. The HPWM technique is used to obtain high quality output waveforms with reduced switching losses [6]. With this method, only two of the four switches are pulse width modulated at high frequency for high quality output, and the other two are commutated at the low frequency to reduce the switching losses.

To overcome these difficulties a random switching method is used. The switches are commutated at high frequency or low frequency in a random manner. In this method the main drawbacks are the switching losses, heating among the switches and the duration of voltage and current stresses are unequal.

This paper proposed a sequential switching HPWM full bridge inverter based UPS, which provides sinusoidal output with low order harmonics, reduced switching losses and high efficiency. It also equalizes switching losses, voltage stress and current stress among the power switches, thereby improving system reliability.

2. Conventional PWM inverter

The efficiency of the PWM inverter mainly depends upon the switching losses, conduction losses and power losses. The conduction losses are reduced by selecting

low ON state resistance of power devices. The efficiency can be improved by reducing switching losses and harmonic losses, which are reduced by employing sinusoidal PWM methods[1]. Unipolar PWM and Bipolar PWM switching schemes are widely employed for full bridge inverter.

In SPWM with Bipolar voltage switching, the switches S_1, S_2 and S_3, S_4 of Fig.2 are treated as two switch pairs. Switches in each pair are turned ON and OFF simultaneously.

S_1 and S_2 are ON when $V_m > V_c$;

the output voltage $V_o(t) = +V_g$

S_3 and S_4 are ON when $V_m < V_c$

the output voltage $V_o(t) = -V_g$

Where V_m and V_c represents the Modulation and Carrier voltage. The output voltage $V_o(t)$ fluctuates between $+V_g$ and $-V_g$.

In SPWM Unipolar voltage switching, the switches in each inverter leg are controlled independent of the other leg. The inverter legs A and B of the full bridge inverter are controlled separately by independent control signals $v_{control}$ and $-v_{control}$.

S_1 ON when $V_m > V_c$ and $V_{AN} = V_g$

S_4 ON when $V_m < V_c$ and $V_{AN} = 0$

S_3 ON when $-V_m > V_c$ and $V_{BN} = -V_g$

S_2 ON when $-V_m < V_c$ and $V_{BN} = 0$

Output voltage $V_o = V_{AN} - V_{BN}$

In this type of PWM scheme, when switching occurs, the output voltage changes between zeros and $+V_g$ or between zero and $-V_g$ voltage levels.

In the Hybrid PWM technique, the power switch operates with high frequency SPWM in the positive half cycle controlled by positive control signal.

Switch ON when $V_m > V_c$

Switch OFF when $V_m < V_c$

Fig.2 shows the basic full bridge inverter is proposed [2] for the reduction of switching losses. In HPWM, the four switches are operated at two different frequencies, switches S_1 / S_4 are commutated at low frequency and S_2 / S_3 are commutated at high frequency SPWM signal to get high quality output waveform. This arrangement causes the problem of differential switching losses and therefore differential heating among the switches. The proposed SSHPWM method is designed to overcome this problem.

Fig.3 - Fig.5 shows the modulation and carrier waves and output voltage waveforms for Bipolar PWM, Unipolar PWM and Hybrid PWM respectively.

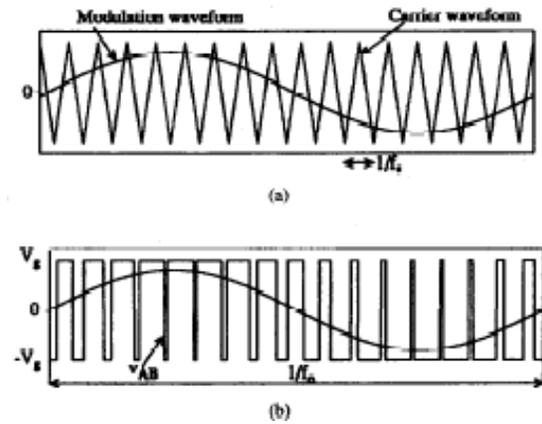


Fig. 3 BPWM switching and output voltage waveform

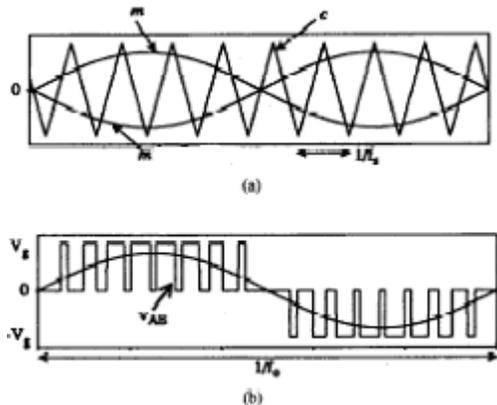


Fig. 4 UPWM switching and output voltage waveform

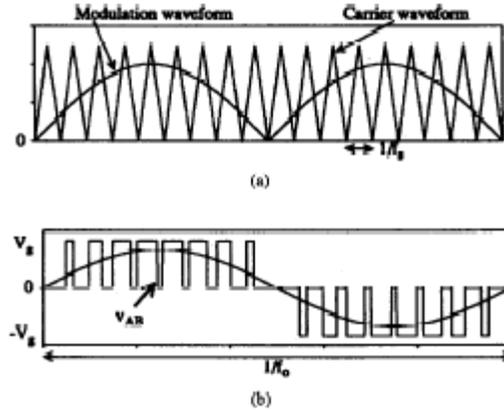


Fig. 5 HPWM switching and output voltage waveform

3. Proposed topology:

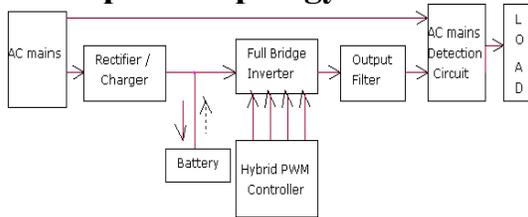


Fig.6 HPWM controller

Fig.6 shows the schematic of a SSHPWM based UPS. The proposed sequential switching HPWM method commutates the power switches at high frequency SPWM or low frequency PWM signals alternatively in the alternate cycles of operation. Fig.5 shows the block diagram for SSHPWM controller. The input signals for combinational logic circuit are A, B and C. The sequential signal (A) is a 25 Hz square wave with 50 % duty cycle. The low frequency PWM signal (B) is 50 Hz square wave with 50 % duty cycle.

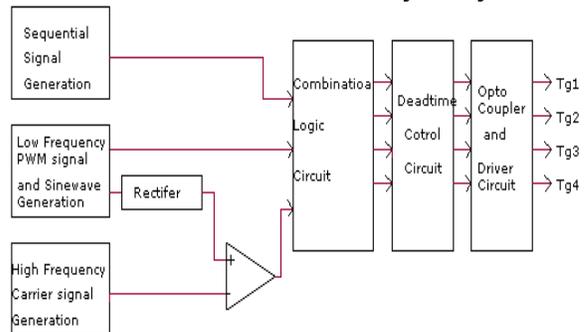


Fig.7 Block diagram for Hybrid PWM controller

The rectified modulated signal compared with carrier waveform that produces high frequency SPWM pulses. The high frequency sine PWM can be expressed as

$$C=1 \text{ when } V_m > V_c \text{ and}$$

$$C=0 \text{ when } V_m < V_c.$$

The combinational logic circuit is serves to integrate low frequency PWM signal and high frequency SPWM signals with sequential signal that produces a SSHPWM gate pulses to the full bridge inverter.

The functions of the combinational logic circuit are expressed as,

$$T_{g1} = ABC + \bar{A}B$$

$$T_{g2} = A\bar{B}C + \bar{A}\bar{B}$$

$$T_{g3} = \bar{A}BC + A\bar{B}$$

$$T_{g4} = \bar{A}BC + AB$$

The gate signals are given to the inverter module shown in the Fig.6. The output of the inverters are filtered and given to the load.

In this scheme, the switching losses among the four switches are equal, also the voltage stress, current stress of four switches are equalized. The SSHPWM scheme allows use of identical power devices and heat sinks, permitting a simpler and more reliable design.

4. Hardware Description:

4.1. Hybrid PWM signal generation

The main function of this circuit is to generate sequential signal, low frequency PWM signal and high frequency sine PWM pulses. XR2206 monolithic function generator IC used to provide 50Hz sine wave, square wave signals and 12.5Khz triangular signal. The triangular signal is used as carrier signal for high frequency sine PWM generation. The control signal rectified using precision full wave rectifier

whose amplitude increased by non-inverting amplifier. The amplitude of the modulation signal should be less than the amplitude of the carrier signal. The rectified modulation signal compared with carrier signal that produces sinusoidal PWM pulses. The negative portions of sine PWM pulses are blocked through IN914 diode that gives high frequency sine PWM signal C.

4.2 Combinational logic circuit and Dead time control circuit

The combinational logic circuit implemented using 74HC series IC's

The dead time control circuit is used to provide the blanking time between one pair of gate pulses with another pair of gate pulses in order to avoid the cross conduction through the same leg of the inverter. The dead time control circuit produces dead time of 1 microsecond between the pair of pulses.

4.3 Isolation circuit & Driver circuit

In the inverter bridge each power device should be gated separately. The upper devices are floating and lower devices operate with ground. Therefore, Isolation and driver circuit is needed to isolate the power circuit from the control circuit. 6N136 high-speed optocoupler used for isolation.

The output of the optocoupler is not capable to drive the transistors present in the totem pole arrangement. So the current carrying capability is improved using buffer 7407 IC.

4.4 DC-DC fly back converter

Optocoupler needs isolated power supplies that provided by DC-to-DC fly back converter. DC-to-DC fly back converter is designed to provide three isolated 5/12V regulated power supplies to the optocoupler and driver circuit. The output becomes semi regulated and by using linear regulated IC's 7812 and 7805, 5/12V regulated voltages are obtained. The high

frequency isolation transformer in the fly back converter used to energy storage, isolation and as current limiting inductance.

4.5 Inverter module:

The full bridge inverter is designed using IRFP150N MOSFETS. The LC filter used to filter out the high frequency components and smoothen the inverter output voltage.

The Low voltage cutoff and over load cutoff protection circuit, AC mains detection circuit, Rectifiers and Battery charger units are designed and implemented.

5. Experimental results:

A 100 W SSHPWM Inverter designed to demonstrate the feasibility of the concept. The inverter specifications are $V_g=40$ V, $M_a=0.8$, $f_s=12.5$ KHz, $f_o=50$ Hz, $R= 40\Omega$, $L= 0.16$ mH and $C=30$ microfarad. The power switches are IRFP 150 N, which has the ratings of 40A, 100 V, less switching speed, low ON resistance and high input impedance.

The UPS remains in a standby mode under normal conditions. When the power supply presents it is directly connected to the load and rectifier and battery charger. When the power failure occurs, the battery supplies power to an inverter whose output connected to the load through change over switch. Hybrid PWM inverter converts DC into pulse width modulated AC output, is filtered by output filter that produces sinusoidal output voltage. The output voltage level is raised to 230V by transformer and connected to the load.

Fig.8 – Fig. 14 shows the various output stages of SSHPWM based UPS. This experiment supports the feasibility of sequential switching HPWM scheme.

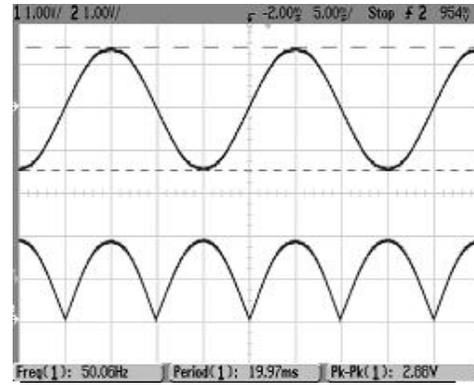


Fig. 8 Rectified Modulation waveform

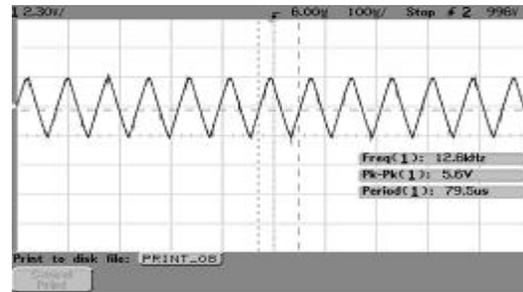


Fig.9 Carrier waveform (12.5 KHz)

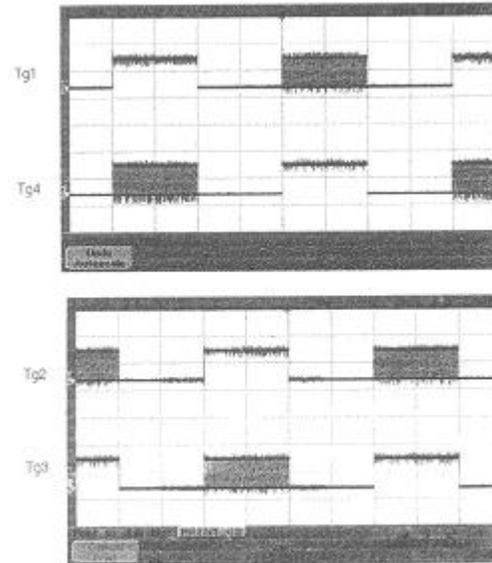


Fig.10 Gate pulses for Power Devices

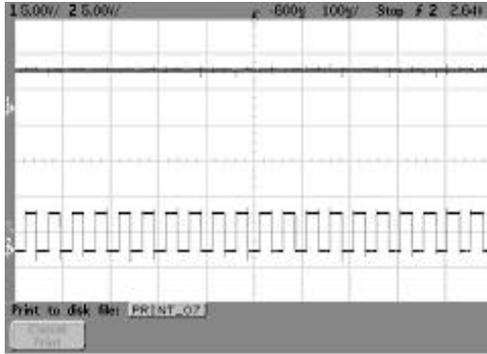


Fig.11 Expanded waveforms

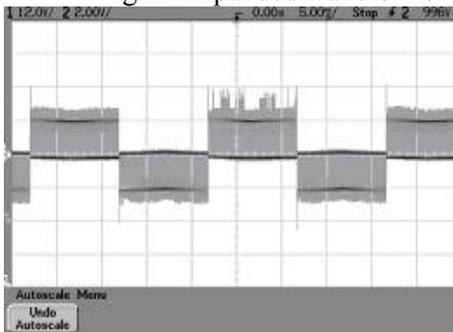


Fig.12 Inverter output without filter

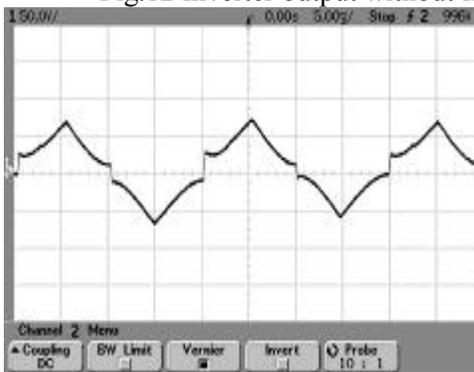


Fig.13 Inverter output with filter

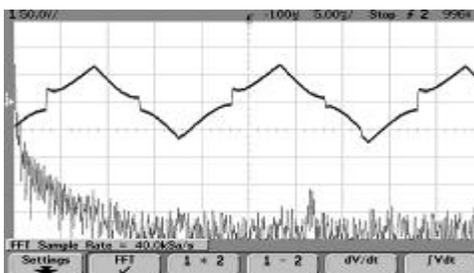


Fig.14 Inverter output with FFT waveform

6. Conclusion

A sequential switching method for HPWM full bridge inverter based UPS is proposed. This method produces sinusoidal output voltage with reduced low order harmonics, reduced switching losses and high efficiency. It also overcomes problem of unequal switching loss, voltage and current stress among the switches. This scheme does not require additional power switches, diodes and reduces the output filter size. The feasibility and practicality of the SSHPWM design is verified by experiment results.

References:

1. F.Z.Peng, H.Akagi, and A.Nabae, "A practical approach to harmonic compensation in power system-series connection of passive and active filter", IEEE Transactions of Industrial Applications, vol IA-19, no.2, pp 254-267, Mar/Apr 1983.
2. R.S.Lai and K.D.T.Ngo, "A PWM method for reduction of switching losses in a full bridge inverter", IEEE Trans. Power Electronics, Vol 10, PP323-332, May 1995
3. Muhammad Quamruzzaman et al, "A New Hybrid PWM scheme for Voltage source inverters", ICECE, Dec 2002
4. N.Mohan, T.M.Undeland and W.P. Robins, Power Electronics: Converters, Applications and Design, New York, John Wiley 1989.
5. J.S.Lai, "Resonant snubber based soft-switching inverters for electric propulsion drives", IEEE Transactions on Industrial electronics, Vol 44, pp.71-80, Feb 1997.
6. TSU-Hua Ai, Jiann-fuh chen, and Tsorng-Jou Liang, "A random switching method for HPWM full bridge inverter", IEEE transactions on Industrial Electronics, Vol.49, No:3, June 2002, PP 595-597.