Low Power Consumption Analog Matched Filter

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Abstract: - A low power consumption AMF (Analog Matched Filter) is proposed which utilizes capacitor Multiply and capacitor Accumulation operations. High speed - high precision A/D converter is unnecessary because the proposed circuit directly samples received analog signal. The code shifting MF structure is used to prevent error from accumulating. A 15-tap AMF circuit was fabricated using CMOS process. Power consumption for 128-tap circuit is estimated as 2.35mW@25MHz 3.3V. The area is estimated as 1.6mm^2 so that the proposed circuit will be applicable LSI for mobile terminals.

Key-Words: - DS-CDMA, Matched Filter, Analog circuit, Weighted-sum operation, Spread spectrum, Multiply and Accumulation operation

1 Introduction

Recently, mobile terminals tend to adopt the DS-CDMA system. This system needs Matched Filters (MF) for aquisition of PN codes and various kinds of MF are realized, such as analog, CCD, SAW, as well as digital. Reduction of power consumption and chip area have been important issues in order that MF is applicable to mobile terminal LSI.

There is a great amount of demand for MF with respect to speed and number of taps, which naturally demand more power consumption and chip area.

In this paper, a low power consumption AMF (Analog Matched Filter) is proposed which utilizes capacitor Multiply and capacitor Accumulation operations. The proposed AMF circuit is designed and fabricated using $0.35mm$ CMOS technology.

2 Problem Description

2.1 Matched Filter

To recover information signal, it is necessary to perform correlation operation on PN codes in the DS-CDMA system. The fundamental operation is described by

$$f(t)=\sum_{i=1}^{n} a(i)r(t-i) \qquad (1)$$

Here, n is the number of taps, $a(i)$ is a PN code and $r(t)$ is a received signal.

This equation indicates that the peak correlation value results only when the timing of a PN code matches that of a received signal. A receiver restores the original information by the detected correlation timing.

2.2 Digital Matched Filter

A block diagram of the conventional DMF (Digital Matched Filter) system is shown in Fig. 1 and Fig. 2.

2.2.1 Data Shifting Matched Filter

Storing a received signal one by one in a data shift register (for received signals), this scheme outputs the correlation value operated with the PN code of each tap. This is an FIR filter where the number of taps is equal to the code length of a PN code. This structure is straightforward and general. However, power consumption becomes large since the data shift registers operate simultaneously.

If the number of quantization bits of an input signal increases, power consumption and chip area will increase further.

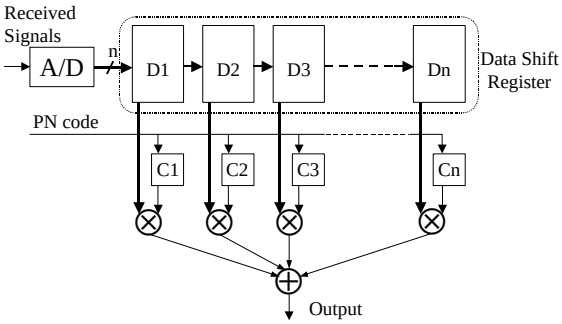


Fig. 1: Operation Block of Data shifting MF

2.2.2 Code Shifting Matched Filter

This filter utilizes the code shift register (for PN codes) instead of the data shift register (for received signals) used in the data shifting MF. Moreover, a received signal is distributed to the register at every sampling. Consequently, it can reduce the power consumption.

Although power consumption of the DMF itself is reduced [1], high speed - high precision A/D converter is needed for quantizing a received signal with sufficient accuracy which naturally increases power consumption as well as chip area.

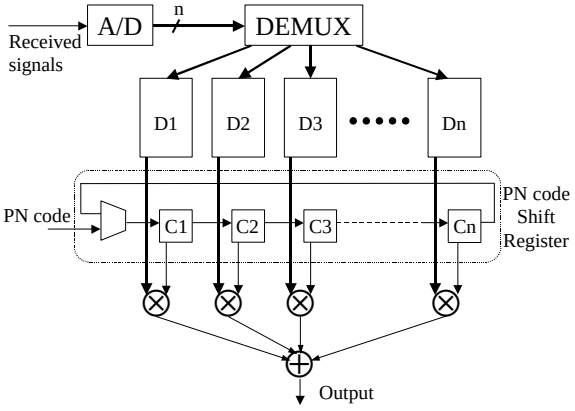


Fig. 2: Operation Block of Code shifting MF

2.3 Analog Matched Filter

Analog MF in [2] [3] is proposed for this reason. The operation block of AMF is almost the same as a digital system. However, the A/D converter described before is unnecessary and low power consumption is realized by using a S/H (Sample-and-Hold) circuit instead of the shift register for received.

Error accumulates in the data shifting analog MF for every transmission so that it is difficult to form large number of taps. On the other hand, MF has an effective structure in an analog MF system since the code shifting analog MF does not produce the error by transmission.

3 Problem Solution

In this paper, a low power consumption AMF (Analog Matched Filter) which utilizes capacitor Multiply and capacitor Accumulation operations [4] is proposed.

The proposed structure of the AMF is shown in Fig. 3, and circuitry for 1-tap is shown in Fig. 4.

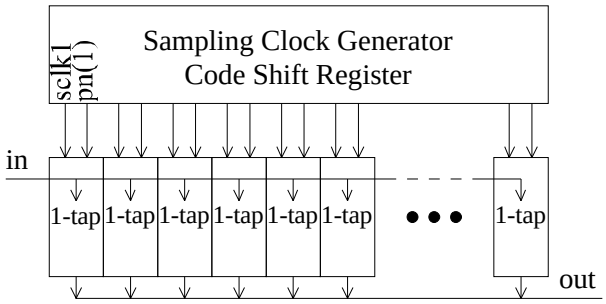
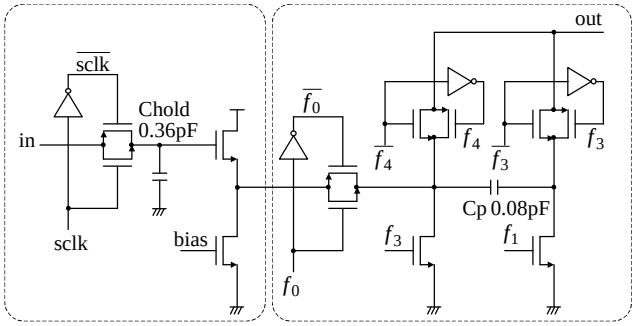


Fig. 3: Proposed AMF



S/H Stage Weighted-sum Operation Stage

Fig.4: Circuitry for 1-tap

Note that a straightforward weighted sum circuit with capacitors can operate on either positive voltages or on negative voltages. The proposed circuit can perform weighted sum operations on signed voltages by changing connection of capacitor nodes.

This proposal circuit for 15-tap was fabricated in a $0.35mm$, 3 metal, 2 poly, 3.3V CMOS process. A chip microphotograph is shown in Fig.5 and Fig. 6.

The chip size of an AMF circuit area is about $0.2mm^2$, so that estimated area for 128-tap is approximately $1.6mm^2$. However, due to the restriction of design rule, capacitor that is an important component has to be designed between Poly-Metal in this chip. For this reason, the circuit area becomes large. By using the capacitor between

Poly-Poly, the chip area is significantly reducible, and the wiring capacitor can also be reduced, thus reduction of the power consumption is also expected.

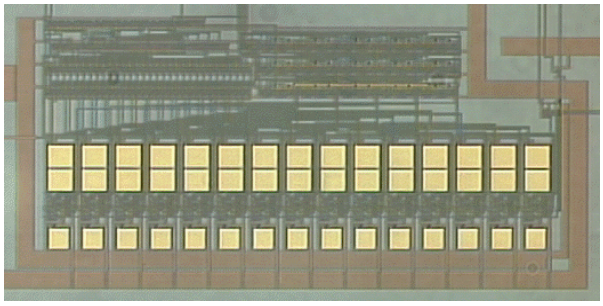


Fig. 5: Microphotograph of the Analog Matched Filter

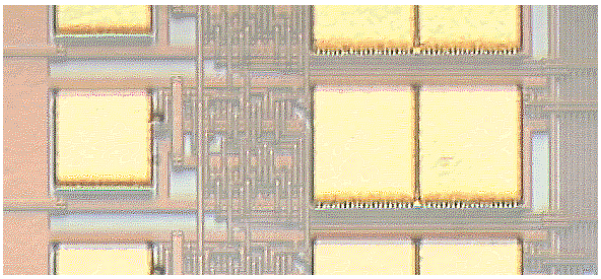


Fig. 6: Microphotograph of the circuitry for 1-tap

4 Result

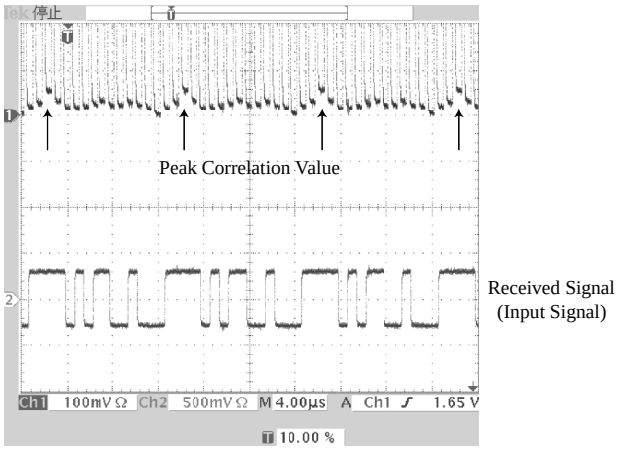


Fig.7: Measurement Result

The measured waveform is shown in Fig. 7. The peak of a correlation value has appeared once for every 15 operations so that the MF is fully functional.

Comparison with other results is shown in Table 1. Although direct comparison cannot be performed due to difference of processes, this proposal circuit may serve as an effective system by smaller chip area and power consumption.

Table 1: Comparison of Each Architecture

	Core area	Power	Technology
$DMF_{[1]}$	$0.300mm^2$	7.48mW 40MHz, 1.8V	0.18*mm*
$AMF_{[2]}$	$91mm^2$	225mW 20MHz, 3.0V	0.8*mm*
Proposed AMF	$1.6mm^2$	2.35mW 25MHz, 3.3V	0.35*mm*

The feature of this proposal circuit is shown in Table 2.

Table 2: Features of the Proposed AMF

Voltage	3.3V
Power Consumption	168*mW* @1.25MHz
Chip Area	$0.2mm^2$ (Circuit Area)
Number of Taps	15
Maximum chip rate	25MHz
Process	0.35*mm*

5 Conclusion

A low power consumption AMF (Analog Matched Filter) is proposed which utilizes capacitor Multiply and capacitor Accumulation operations. High speed - high precision A/D converter is unnecessary because the proposed circuit directly samples received analog signal. The code shifting MF structure is used to prevent error from accumulating. A 15-tap AMF circuit was fabricated using CMOS process. Power consumption for 128-tap circuit is estimated as 2.35mW@25MHz 3.3V. The area is estimated as $1.6mm^2$ so that the proposed circuit will be applicable LSI for mobile terminals.

Based on the measurement result, the 128-tap AMF using the capacitor between Poly-Poly is due to be designed.

6 Acknowledgement

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

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