Design and Implementation of a Multi-Carrier Demodulator

H. HO*, V. SZWARC*, C. LOO*, and T. KWASNIEWSKI**
* Communications Research Centre
3701 Carling Ave., Box 11490, Station H, Ottawa, Ontario, K2H 8S2
CANADA

**Department of Electronics
Carleton University
1125 Colonel By Drive, Ottawa, Ontario, K1S 5B6
CANADA

Abstract: - This paper presents a design and implementation of a multi-carrier demodulator (MCD) circuit. The circuit is designed to handle eight channels at T1 data rates. The design, implementation, and simulations are based on Altera’s APEX20K1500 SRAM PLD devices. The MCD circuit design is validated by comparing the performance with functional models developed with SystemView and its communications library. Simulation results for the T1 channel rate MCD design are presented. Circuit test and verification results at both maximum throughput and T1 data rates under typical operating conditions are presented.

KeyWords: - Multi-carrier Demodulator, polyphase-FFT, System on a Chip

1 Introduction
Transmultiplexing techniques and architectures for a broad range of terrestrial and satellite applications have been documented in the literature [1,2,3] over the last thirty years. The MCD implementation considered here has its roots in the polyphase FIR filter and FFT group demultiplexer architecture introduced by Bellanger and Daguet [4]. The multi-carrier demultiplexer is also a key building block in such hybrid architectures as FDMA-CDMA [5] and FDMA-TDMA [6] receivers for wireless applications. In brief, the MCD demultiplexes and downconverts the received FDM signal, which is subsequently demodulated on a per channel basis to recover the original symbol data. To address the considerable digital signal processing requirement, implementation of a polyphase-FFT MCD based on a combination of DSP processors and custom designed arithmetic processing cells has been reported in the literature [7]. However, the current trend towards higher circuit densities makes it now possible to consider a system on a chip (SOC) implementation of the MCD. The MCD circuit proposed in this paper consists of a polyphase-FFT group demultiplexer and eight channel processors operating at T1 (1.544 MSamples/s) data rates. The polyphase-FFT architecture provides a computationally efficient method of down converting to baseband a group of N FDM signals, where N is normally an integer power of two [3]. The coherent demodulation is carried out by using a timing correction technique combined with rate conversion filtering and an all-digital phase lock loop [7-9]. The demodulation is carried out on per channel basis by dedicated channel processors. Since the sampling rate of the group demultiplexer’s signal outputs is different from the channel symbol rate, the channel processors need to perform rate conversion on the signals. Furthermore, symbol timing recovery and carrier phase synchronization is performed on the baseband signals to compensate for any offsets that may occur during transmission.

The eight-channel MCD was implemented with the APEX 20KE1500 PLD technology [11]. The device selection process was based on throughput, power, and logic resource considerations. The availability of embedded RAM enabled the implementation of the design without external memory. Since all filter coefficients are stored in on-chip RAM, memory access time is not a critical constraint on filter throughput. An eight-channel MCD and an eight-channel group demultiplexer circuit have been implemented for performance comparison purposes. The power consumption of the eight channel two chip MCD implementation was measured to be 780 mW per chip, at the T1 data rate. At 28 Msamples/s, the maximum recorded throughput of the MCD circuit, the corresponding power consumption was 1,260 mW per chip.
2 MCD Architecture

The complex signal input to the system consists of eight adjacent FDM channels with bandwidths of B MHz per channel. The real and quadrature components of the sampled input signal $S_{in}$ consist of data streams of 8B Msamples/s. The $S_{in}$ signal is routed to the polyphase filters, whose complex outputs are phase shifted, as depicted in Fig. 1. The complex output of the FFT is comprised of the individual signals down converted to baseband. Each $S_{out}$ signal is wired to a channel processor where carrier phase and symbol timing is recovered. The channel processor also performs a rate conversion on the baseband signal converting it from the channel sample rate $f_s$ to the symbol rate $f_b$.

2.1 Group Demultiplexer

The group demultiplexer (GD) consists of a complex polyphase-FIR filter bank, a group of phase shifters, and an FFT module. The complex polyphase filter bank consists of two banks of low pass FIR filters of 7 taps each. One of the filter banks processes the real signal and the second processes the quadrature signal. The number of taps and the filter coefficient word size were determined [10] with a view to minimizing the hardware while achieving a desired system bit error rate as a function of the signal-to-noise ratio. The filter at the receiver has the root-Nyquist characteristic. However, the implementation of the filter is based on a distributed approach by partitioning it between the group demultiplexer and the channel processor. Thus the polyphase-FIR filter has the characteristics of a fourth-root raised cosine filter. The real and quadrature portions of the polyphase filter have the same set of coefficients.

The phase shifter block consists of a set of eight complex multipliers. These complex hardwired multipliers execute multiplication at the sample rate of the polyphase filter outputs. As the stored constant phase shift adjustment inputs to the multipliers have mostly modest Hamming weights, this facilitates compact circuit implementations.

The FFT module is an eight point, radix-2, decimation-in-time, discrete Fourier transform circuit. The fully parallel FFT implementation consists of hardwired, interconnected complex butterflies. The butterfly outputs were scaled by a factor of two to prevent overflow. Thus the output of an eight point FFT is scaled by a factor of eight.

2.2 Channel Processor

The channel processor consists of an adaptive rate conversion filter and clock recovery and timing recovery circuits. The rate conversion filter together with the clock recovery module converts the data rates of the baseband signals to the original symbol rate. The rate conversion filter contains two complex, nine tap, pulse shaping FIR filters. Each of the filters will compute the input signal by sampling it at best eye opening and at zero crossing points respectively. The FIR filters have the characteristics of a fourth-root raised cosine filter. The clock recovery module determines if any symbol timing error has occurred and produces a signal to control the rate conversion filter adaptively. The carrier recovery module performs carrier phase and frequency offset compensation for the PSK modulated signal at the output of the rate conversion filter as shown in Fig. 2.

3 MCD Design

The VHDL design for the 8 channel MCD has been written and compiled using Mentor Graphic's Leonardo Spectrum synthesis tools.

The input to the polyphase filter bank is a complex data signal of 16 bits consisting of real and quadrature components of eight bits each. The input signal is routed to all of the FIR filters by means of a decoder. For the eight-channel system, the polyphase FIR filter bank consists of 16 such filters. Each channel requires two identical seven tap FIR filters, one for the real and one for the quadrature component of the input signal. The FIR filter realization is based on the direct form architecture with each filter consisting of seven multipliers and a Wallace adder that combines the outputs of the multipliers. For this implementation, all the multiplication and addition operations in each filter are combined and executed by means of shift and add operations. The partial products generated by suitably shifting the input samples are added using carry save adders to yield the individual filter outputs.

The implementation of the phase shifter architecturally corresponds to that of a complex multiplier, which consists of four multipliers and two adders, whose dimensions can be set as required. For this MCD system, the phase shifter module contains 8 complex multipliers. The phase
shift operation involves the multiplication of a 22 bit complex data sample shifted out of the polyphase filter by a fixed phase shift coefficient. The coefficients consist of a set of complex data of 18 bits stored in a look up table in two's complement fractional format. As multiplication of two fractional numbers produces a smaller number, the use of this format mitigates overflow problems. The partial products generated from the multiplication are combined using ripple adders and the outputs are truncated to yield 24 bit complex results in two's complement fractional number format.

For the FFT design, the twiddle factors are stored in two lookup tables formatted as one-dimensional arrays. One array contains the real component and the other contains the imaginary component of the twiddle factors. The FFT circuit design is based on the Cooley-Tukey algorithm with all the building blocks hard wired. The twiddle factor components are precalculated and represented by 9 bit signed numbers, with values ranging from –255 to +255. The complex data I/Os are represented by 24 bits in two's complement fractional number format.

The channel processor module depicted in Fig. 2, processes the GD output signals on a per channel basis. The 24 bit wide complex signal is shifted into the channel processor circuit via a FIFO register. The FIFO register functions as a buffer between the GD and the rate conversion filter. The sampling rates for the FIFO's input and output are the channel data rate $f_s$ and symbol rate $f_b$, respectively. The rate conversion filter's output consists of two 24 bit complex signals, in two's complement format, which correspond to the signal sampling at the maximum eye opening and the transition points. The rate conversion filter consists of two complex, 9-tap FIR filters with the filter coefficients being adaptively controlled by the clock recovery module. The FIR filter implementation is based on the direct form and each one contains nine, 12 bit real multipliers and a nine input, 12 bit real adder. The pre-computed filters coefficients are stored in a look up table. There are 311 coefficients for each of the complex filters and the same set of coefficients is employed for both of the real and quadrature parts of the filters. The filter has a fourth-root raised-cosine characteristic with coefficients quantized to 7 bits in two’s complement format.

The clock recovery module design is based on a double sampling method with a predetermined step size of 2 degrees for timing control. The step size selection is important since it affects the speed and the quality of the timing correction process. The output signals produced by this module are used to control the rate conversion filter. One of the signals controls the coefficient selection process and the other controls the data flow into the rate conversion filter from the FIFO register.

The carrier recovery module is based on a digital PLL architecture designed to achieve an optimum response time and to minimize transient response oscillations. The circuit consists of a phase error detector, a digital loop filter, and a digital VCO. The complex input and output signals of the carrier recovery module are 24 bits wide in two’s complement format. The digital VCO circuit has been realized by using two look up tables. Each of the two look up tables contains 512 data samples which represent one cycle of the sinusoidal waveform's real and quadrature components, respectively. Consequently, the carrier phase error is adjusted with a phase accuracy of 0.7 degrees. In this implementation, the PSK modulated signal has been differentially encoded to avoid phase ambiguity problems in the phase error detector circuit.

4 MCD Functional Verification

To verify the MCD circuit design, a functional model has been implemented using SystemView software tools [12]. The implemented model incorporates transmit and receive portions of the multi-carrier system and includes an eight channel GD and a channel processor as depicted in Fig. 3. The functional model, implemented in fixed number format, accurately reflects the architecture and I/O characteristics of the MCD circuitry. The functional model makes use of SystemView’s built-in communications library, which includes such library elements as a QPSK modulator/demodulator and a pseudo random signal generator.

The signal input to each channel in Fig. 3 is a pseudo random sequence. These signals are then modulated and multiplexed by a group modulator to generate the composite FDMA signal. The group modulator is complementary to the group demodulator in both its functionality and architecture. Thus, the group modulator incorporates a group of Tx channel processors, a polyphase filter bank with root-Nyquist characteristics, phase shifters, and an inverse FFT. The output of the group modulator consists of a
multi-carrier signal with the eight channels up-converted into the appropriate channel slots. This functional model can be used effectively to verify the operation of the MCD as well as to determine the bit error rate for specific signal to noise ratios.

The MCD model has been built with building blocks described in the previous section. The binary data at the output of the receiver module is collected and compared against the data generated by the PN sequence generator at the transmit side.

Functionality of the MCD circuits has been verified, based on the above model, using stimuli generated or present at various stages and interfaces of the functional model depicted in Fig. 3.

5 Implementation and Simulation Results

Simulation results and hardware resource requirements for the eight channel GD and MCD implementations are shown in Table 1. The results show that the eight-channel GD requires only 14% of the selected device's logic resources and can support data rates that are significantly higher than T1. On the other hand, the MCD design implementation requires two devices and the simulation results show that the throughput does satisfy the requirements of T1 data rates. However, the maximum throughput of the MCD circuit is lower than that of the GD. The factors responsible for this include the increased routing delays, in this implementation with 74% logic element utilization, as well as the relatively modest throughputs of the channel processor's arithmetic functions in its timing and carrier recovery modules.

<table>
<thead>
<tr>
<th>Hardware Utilization</th>
<th>Throughput Msamples/s</th>
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<tbody>
<tr>
<td>Logic Elem. Mem. Bits</td>
<td>T1 Max T1 Max</td>
</tr>
<tr>
<td>GD 7337 (14 %) 0</td>
<td>12.4 47</td>
</tr>
<tr>
<td>MCD Chip 1 38239 (74 %) 267264 (60 %)</td>
<td>12.4 35</td>
</tr>
<tr>
<td>MCD Chip 2 38239 (74 %) 267264 (60 %)</td>
<td>12.4 35</td>
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Table 1: Hardware requirements and simulation throughput results for eight-channel GD and MCD.

The throughput information in Table 1 was obtained using Altera’s Quartus II timing analyzer.

The GD and MCD circuit implementations have been carried out using Altera’s Quartus II compiler. Hardware requirements for the design implementations were determined from the compilation process, which provides data on the number of logic cells and memory bits needed to execute mapping and routing.

Hardware testing of the eight channel GD and MCD circuits was carried out with an IMS XL100 digital tester. The GD and MCD circuits were tested for functionality and found to be fully operational at T1 data rates. Furthermore, power consumption of the circuits has been measured for throughputs at both T1 and maximum data rates, under typical operating conditions as presented in Table 2.

<table>
<thead>
<tr>
<th>Throughput Msamples/s</th>
<th>Power (mW)</th>
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<tbody>
<tr>
<td>T1 Max T1 Max</td>
<td></td>
</tr>
<tr>
<td>GD Chip 1 12.4 28</td>
<td>779 1260</td>
</tr>
<tr>
<td>MCD Chip 2 12.4 28</td>
<td>779 1260</td>
</tr>
</tbody>
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Table 2: Test data for the eight channel GD and MCD circuits.

6 Summary

The eight channel multi-carrier demultiplexer and demodulator circuits have been designed and implemented on Altera’s APEX 20KE1500 PLD devices. The functionality of the GD and MCD circuits has been verified by means of accurate functional models developed with the SystemView's tools and communications library. The availability of high density PLDs has enabled the implementation of the entire eight channels GD on one chip. For the eight-channel MCD implementation two chips are required. Simulation of the eight-channel MCD circuit shows that the circuit performance satisfies the throughput requirement for T1 channel data rates. Circuit tests performed on the eight-channel MCD PLD implementation confirmed the simulation throughput results. Furthermore, the maximum throughput of 28 Msamples/s indicates the viability of extending the circuit design to handle E1 data rates. Power consumption for the eight channel GD and MCD were measured to be 203 mW and 1,558 mW, respectively, at T1 data rates. The power and hardware requirements for both chips making up the
MCD module are identical reflecting the actual circuit partitioning between the two chips. For the case of maximum data throughput of 28 Msamples/s, the power consumption of each of the two chips making up the MCD is 1260 mW.

References:

Figure 1: Multi-carrier Demodulator block diagram.
Figure 2: Rx channel processor block diagram.

Figure 3: Block diagram of a Tx/Rx chain for functional and circuit verification of the MCD.