1V Sample-and-hold Circuit Using Switched Opamp

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Abstract: Sample-and-hold circuits are usually used to be the front-end of the analog circuit. It can transform the continuous time signal to the discrete time signal that is suitable for the sampling of the main circuits. This paper presents a new low voltage sample-and-hold circuit. The sample-and-hold circuit can operate under V_{DD}=1V supply voltage, and the output swing is 380mV_{pp} under UMC 0.5μm DPDM process. The sample-and-hold circuit uses the pseudo-differential architecture to suppress the common mode noise and avoid the use of the common mode feedback (CMFB) circuit. We also use a switched opamp technique to reduce the power consumption. The power dissipation is only 68.6 μW, and save 21% power compared to that of the non-switched-opamp approach. The total harmonic distortion is about 28dB.

Key-Words: Low voltage, low power, switched opamp, sample-and-hold circuit.

1 Introduction

Sample-and-hold circuit is a basic building block that is usually used in analog SC circuits. It can be used as the front-end circuit of the pipelined ADC, subranging ADC or SC filter to transform the continuous time signal to discrete time signal that is suitable for the sampling of the main circuit. Integration of the low voltage sample-and-hold circuits and the low voltage SC circuits on a single chip can achieve low power and low cost purposes.

Switched opamp is a good technique to implement low voltage SC circuits [1]. The circuit can operate normally while the opamps are turned on and they will not affect the normal operation while the opamps are turned off. The current of the opamps can be reduced effectively to achieve power-saving purpose while the opamps are turned off. The switched opamp technique has both low voltage and low power characteristics and is suitable to implement the SC circuit.

Many low voltage SC circuits are used in portable electronic devices. Some SC circuits need the sample-and-hold circuits to be the front-end circuit to enhance the circuit performance. A new low voltage sample-and-hold circuit that can be the front-end of the SC circuits is proposed in this paper. The switched opamp is used for low-power consideration. The total circuit is operated in 1V supply voltage with sampling frequency of 50Ks/s, and total power consumption is 68.5μW. The sample-and-hold circuits with ordinary opamp may consume 87.2μW. The switched opamp technique can save power consumption up to 21%. The total harmonic distortion (THD) of this sample-and-hold circuit is 28dB.

2 Low Voltage Switched Opamp Design

In a low supply voltage application, the opamp structure is different from that of the normal supply voltage. Generally, the minimum supply voltage is $V_{DD,min}=V_{th,p}+2V_{ov}$ [2]. Since the circuit is designed to operate under V_{DD}=1V, the input DC voltage level is V_{IN_DC} =0V, and the output voltage of the opamp is V_{OUT_DC} =V_{DD}/2= 0.5V for the full swing purpose. In order to obtain a higher voltage gain, the opamp is designed by the two-stage folded-cascode low voltage architecture [7] as shown in Fig.1. Both C_C and M_C are used for the Miller compensation to obtain a better phase margin. M_{14}, M_0, and M_C are the opamp switches to control the switched opamp to switch in "ON" or "OFF" state. The quiescent current of the first stage is I_{1st}=23.09μA, and the quiescent current of the second stage is I_{2nd}=18.73μA. The first stage of the opamp is kept in a "always-turn-on" state, and the second stage of the opamp is controlled by the opamp switches. This scheme can shorten the turn-on time of the opamp to speed up the switching operation [2].

This opamp is designed by the DPDM 0.5μm CMOS technology. The geometry sizes of the transistors of the opamp are summarized in Table I.

The threshold voltage of the NMOS is $V_{th,n}$=0.8V, and that of the PMOS is $V_{th,p}$=1.03V. It is as much as possible to drive the MOS transistors of the opamp to operate at subthreshold region [5] that can result in higher transconductance and voltage gain. The voltage gain of the opamp is 67dB, and its unit gain frequency is 2.5MHz with the load capacitance C_{load}=1pF. While CKB is high, the opamps are switched off, and the outputs of the opamps can maintain the voltage value of the previous phase. From Fig.2, the capacitors C_{int}'s are charged to Vin. The quiescent current of every opamp is 34.34μA at the "off" phase. While CK is high, the opamps are switched on, and the outputs of the opamps are the voltage drops across the capacitors C_{int}'s. In addition to maintain the performance of the opamps, the aspect ratios of the switches M0 and M14 are quite large. The quiescent current of every opamp is 43.71μA at the "on" phase.

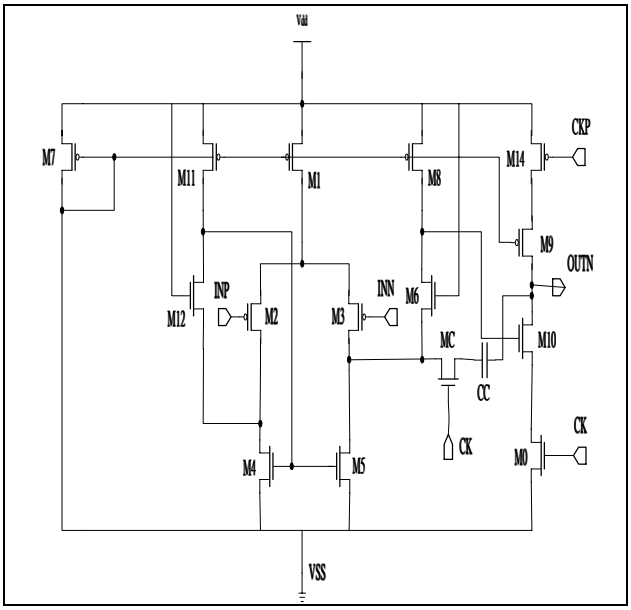

Fig.1 Low voltage switched opamp structure

3 The Proposed Sample-and-Hold Circuit

The proposed sample-and-hold circuit is composed of switches, capacitors, and opamps [6], and the diagram is shown in Fig.2. The circuit cannot maintain a rail-to-rail output swing, because the input terminals are connected serially to the NMOS switches [4]. When CKB is high, the opamps are turned off by switches M0 and M14, and the input signal is sampled on the capacitors C_{int1} and C_{int2}. The output terminals maintain the previous phase output voltage value by the capacitors $C_{ext1,2}$. The capacitors $C_{ext1,2}$ can also suppress the charge sharing while the opamps are turned off. The values of capacitors values of $C_{ext1,2}$ are about 0.1nF, and thus are not suitable to be implemented on the chip. When CK is high, the opamps are turned on, and the voltages across the capacitors $C_{int1,2}$ are transferred to the output of the opamp. It may take some time to turn on the switched opamp. It is worth mentioning that M_{S1}-M_{S4} are designed by the minimum size to limit the charge sharing. The output swing of this circuit is 380mV_{pp} with supply voltage V_{DD}=1V. The input DC level V_{IN_DC} and the output DC level V_{OUT_DC} of the sample-and-hold circuit are both 100 mV. The output voltages of the sample-and-hold circuit will be settling obviously while the opamp is turned on. The pseudo-differential architecture is used to limit the common mode noise effectively and can avoid the use of the CMFB circuit. The total power consumption of this sample-and-hold circuit with switched opamps is 68.6μW, while that of the sample-and-hold circuit with ordinary opamps is 87.4μW. The use of the switched opamps can save power and thus can be used in the low power application. Because the output swing is not rail-to-rail [3] and the charge sharing results from the switched opamp, the THD of this sample-and-hold circuit is thus 28dB.

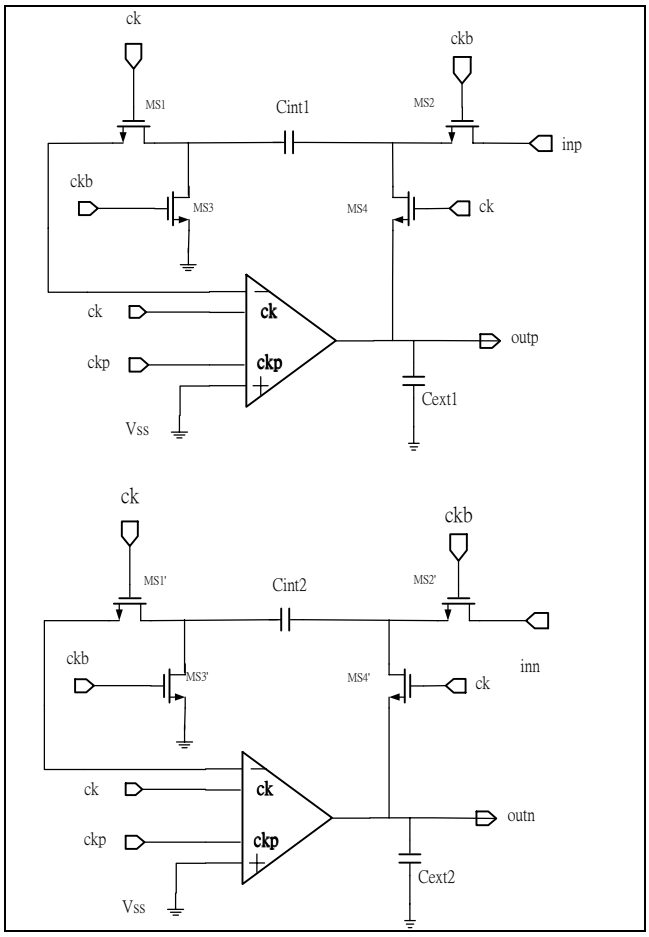

Fig.2 The proposed sample-and-hold circuit

4 Simulation results

This sample-and-hold circuit can operate on supply voltage of V_{DD}=1V with $V_{th,n}$=0.8V and $V_{th,p}$=1.03V by the 0.5μm CMOS technology. The amplitude of the input signal is 400mV_{pp} with frequency of 5KHz. The sample-and-hold circuit can generate the corresponding sinusoidal-like waveform at the output. The clock sampling frequency is 50Ks/s, and the output waveform of the proposed sample-and-hold circuit is shown in Fig.3. The switched opamp is used to implement the sample-and-hold circuit for low power application. The quiescent current is 87.2μA while the opamps are turned on, and 49.9μA while the opamps are turned off. The average power consumption of this sample-and-hold circuit is only 68.6μW. However, the sample-and-hold circuit with the ordinary opamp may consume 87.4μW. The switched opamp technique saves power consumption of 21%. The harmonic distortion is most caused by the opamp switches M0 and M14, since the two switches may cause the charge-sharing problem. The total harmonic distortion is 28dB with sampling frequency of 50Ks/s and supply voltage of 1V. The performance of the sample-and-hold circuit is summarized in Table II.

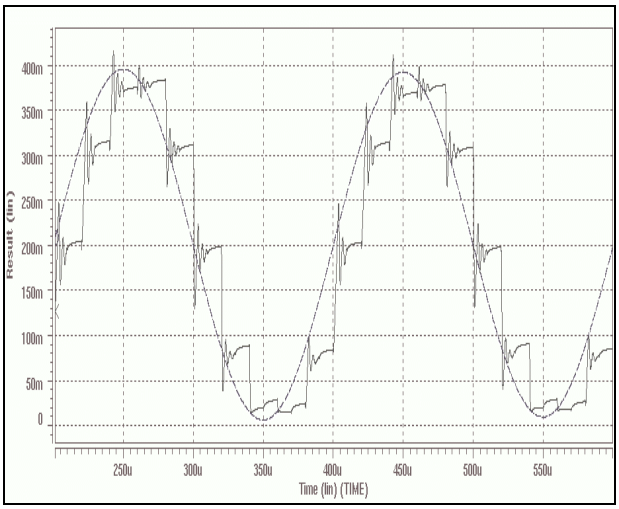

Fig.3 The output waveform of the proposed sample-and-hold circuit

5 Conclusion

The sample-and-hold circuit is designed by the switched opamp under supply voltage of V_{DD}=1V. The pseudo-differential architecture is used to suppress the common mode noise [3]. The output swing of the sample-and-hold circuit is 380mV_{pp} while the amplitude of the input signal is 400mV_{pp} with frequency of 5KHz. The output spectrum of the sample-and-hold circuit is shown in Fig.4. The total power consumption of this sample-and hold circuit is 68.6μW. The switched opamp technique reduces 21% power dissipation better than the ordinary opamp. The THD of this circuit is 28dB because the output swing is not rail-to-rail and the charge sharing results from the switched opamp.

Supply voltage	1V
Sampling frequency	50Ks/s
THD	28dB
Power	68.6μW
1st stage opamp current	23.09μA
2nd stage opamp current	18.73μA
Opamp bias current	1.89μA

Table II The circuit performance

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