A High Accurate and High Output Impedance Current Mirror

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Abstract: Current mirror is one of the most important building blocks of analog integrated circuits. For high performance analog circuit applications, accuracy and output impedance are the most important parameters to determine the performance of the current mirror. A new current mirror based upon regulated-gate cascode (RGC) circuit is proposed to provide very high accuracy and high output impedance. A novel feedback gain stage is used to increase the output impedance and the current matching accuracy significantly. The proposed circuit also has output swing similar as traditional two-stage cascode current mirror.

Key-words: Regular-Gate Cascode (RGC), Improved Active-Feedback Cascode Current Mirror (IAFCCM), current-mode, accuracy, current mirror.

1 Introduction

Because the current-mode approach has better performance, it is gaining interest to use to analog circuit design [1]. In lots of analog circuit design, the current mirror is widely used in the biasing or the loading elements. Thus the current mirror is one of the most important building blocks of analog integrated circuits.

Both the accuracy and the output impedance determined the performance of a current mirror and both must be sufficiently high. Much works focus on these two features. The cascode current mirror and the regular-gate cascode (RGC) current mirror [2] were used to increase output impedance. Improved active-feedback cascode current mirror (IAFCCM) [3] was proposed to improve the accuracy. And the three-stage feedback current mirror [4] was proposed to improve both the accuracy and the output impedance. They still have some problems of output voltage swing, accuracy or output impedance.

In the paper, a new high accurate current mirror is proposed. It based upon the RGC circuit to improve the output impedance and also to improve the current accuracy of the current mirror. A novel feedback gain stage is used to increase the output impedance and matching accuracy significantly. Moreover, the proposed new current mirror also has output swing similar as the traditional two-stage cascode current mirror and without the stability problem. Therefore, the performance of the proposed current mirror is better than that of the RGC and IAFCCM.

2 Analysis of previous circuits and the proposed circuit

2.1 Previous current mirror circuits

The accuracy and output impedance of a classical cascode current mirror are much higher than that of a simple current mirror. But it is possible to gain in higher accuracy and output impedance by using novel circuit schemes.
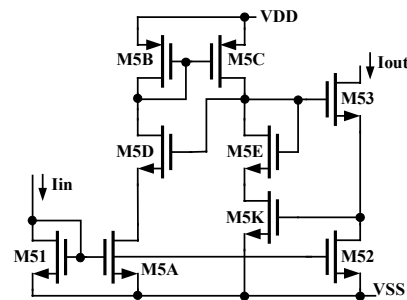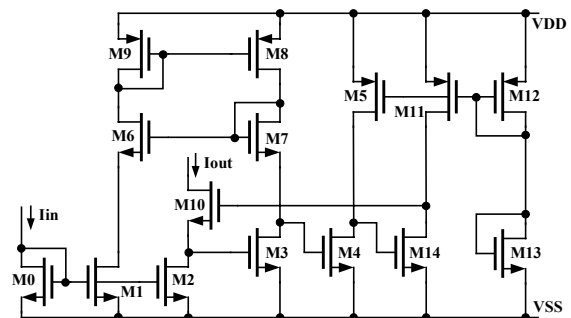

Fig.1 IAFCCM

Fig.2 Three-stage feedback current mirror

The IAFCCM and the three-stage feedback current mirror are shown in Fig.1 and Fig.2, respectively. They are both proposed to increase the output impedance and the accuracy. In the high precision applications, the cascode current mirror and the IAFCCM may not suitable because the output impedance of them is not high enough. The output node voltage can influence the output current in the cascode current mirror and the IAFCCM.

Although, the three-stage feedback current

mirror improves lots of the output impedance and accuracy, it has the problems of the stability and power dissipation. Because of the three-gain stage feedback circuit, it needs compensation to make the whole circuit stable. The additional compensation capacitor increases the circuit area. Moreover, it also needs an additional biasing circuit and increases the cost of power dissipation.

2.2   The proposed current mirror

As shown in Fig.3, an appropriate solution is proposed. It improved the output impedance without any additional compensation and biasing circuit. So it reduces the circuit area and saves the power. Furthermore, it also improves the matching accuracy.

The MOS transistors MN1 – MN4 are used as a two-stage cascode current mirror. The biasing MOS transistors MN5, MN6, and MP1 – MP4 are used to improve the matching accuracy of the cascode current mirror. The novel cascode negative feedback gain stage, which is formed by the MOS transistors MN7 and MN8, increases the output impedance of the cascode current mirror.
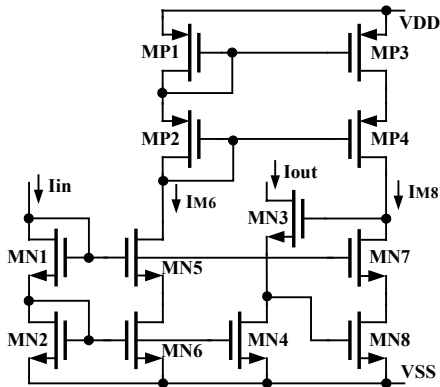

Fig.3 The proposed new current mirror

Figure 4 shows the feedback circuit of the proposed current mirror. The output impedance of the node Vo can be estimated by following equations,

$$V_1 = i_{out} \frac{1}{gd_4} \qquad (1)$$

$$i_{out} = gm_3 v_{gs3} + gd_3 v_{ds3} \qquad (2)$$

the Eq.(2) can be rewritten as,

$$i_{out} = gm_3 \left[gm_8 \left(-\frac{gm_7}{gd_7} \frac{1}{gd_8} \right) - 1 \right] v_1 + gd_3 (v_o - v_1)$$

$$\Rightarrow i_{out} \left(1 + \frac{gm_3}{gd_4} + \frac{gd_3}{gd_4} + \frac{gm_3 gm_8 gm_7}{gd_7 gd_8 gd_4} \right) = gd_3 v_o$$

$$R_{out} = \frac{gm_3}{gd_3} \frac{gm_7 gm_8}{gd_7 gd_8} \frac{1}{gd_4} \qquad (3)$$

where gm_i and gd_i represent the transconductance

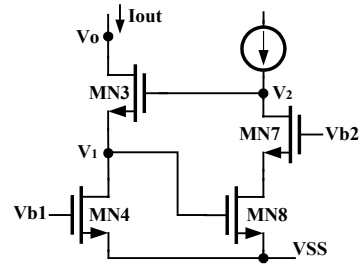and the channel conductance of the MOS MNi, respectively.

Fig.4 The feedback circuit

It is easy to find that the output impedance of the new proposed circuit, Rout, is higher than that of IAFCCM, which has the output impedance as shown in Eq.(4)

$$R_{out} = gm_{53} gm_{5K} \frac{1}{gd_{52}} \frac{1}{gd_{53}} \left(\frac{1}{gd_{5K}} // \frac{1}{gd_{5C}} \right) \qquad (4)$$

But the output impedance of the new proposed current mirror Rout is lower than that of the three-stage feedback current mirror which has the output impedance as shown in Eq.(5)

$$R_{out} = \frac{gm_{10}}{gd_{10}} \frac{1}{gd_2} |A|^3 \qquad (5)$$

where $A \cong -\frac{gm_i}{gd_i}$ (i=3,4, and 14, respectively).

Although the three-stage feedback current mirror has the highest output impedance, it needs to compensate. So, the new proposed current mirror is the appropriate solution if the area and the output impedance are the trade-off.

Another factor of a good current mirror is the current matching accuracy between Iin and Iout. In the proposed circuit, the MOS transistors MP1 – MP4 are used to match the current I_{M6} and I_{M8}. And, if the aspect ratio of the MOS MN5 and MN7 are the same, It can be find that $V_{GS5}=V_{GS7}$. Then V_{DS6} equals to V_{DS8}, and further make $V_{GS6}=V_{GS8}$. Because of $V_{GS6}=V_{GS2}= V_{DS2}$ and $V_{GS6}=V_{DS4}$, it is easy to find that $V_{DS2}=V_{DS4}$ which results in Iin equals to Iout.

3   Simulation Result

The HSPICE simulation results are based upon 0.35um 1P4M CMOS process with 3.3V supply voltage. Figure 5 shows the I-V curve simulation results of the proposed new current mirror and the three-stage feedback current mirror. The middle line is the I-V plot of the input reference current, Iin. The top line is the I-V plot of the three-stage feedback

current mirror, and it shows that the output impedance is higher than the proposed circuit. As mention earlier, it needs compensation to make it stable, which does not require in the proposed circuit. The lowest line is the I-V plot of the proposed circuit. Although the output impedance is a little lower than that of the three-stage feedback current mirror, it is high enough for lots of high precision applications.

In Fig.5, it also shows the comparison result of the accuracy. The current matching accuracy of the proposed current mirror is better than that of the three-stage feedback current mirror.
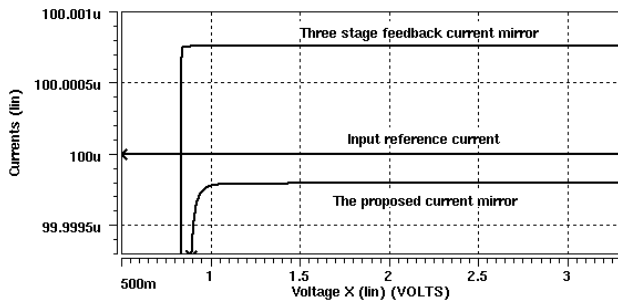

Fig.5 The I-V curve of the simulation result

Table 1 Performance comparison

Issues	IAFCCM	Three-stage feedback current mirror	Proposed current mirror
Mirroring error at Iin=5uA	0.036%	0.0162%	0.00002%
Mirroring error at Iin=10uA	0.03%	0.0121%	0.00002%
Mirroring error at Iin=50uA	0.024%	0.0043%	0.00008%
Mirroring error at Iin=100uA	0.019%	0.0008%	0.00027%
Mirroring error at Iin=150uA	0.017%	0.0021%	0.0025%
Rout	$\propto \dfrac{1}{gd}\left(\dfrac{gm}{gd}\right)^2$	$\propto \dfrac{1}{gd}\left(\dfrac{gm}{gd}\right)^4$	$\propto \dfrac{1}{gd}\left(\dfrac{gm}{gd}\right)^3$

Table 1 compares the performance of IAFCCM, the three-stage feedback current mirror, and the proposed current mirror under various input currents. The input reference current changes from 5uA to 150uA. The proposed current mirror has highest accuracy when the input reference current is lower than 150uA. Due to the cascode structure of the proposed current mirror, some MOS transistors will leave saturation region when the input reference current is over 150uA. Therefore the matching accuracy would worse than the three-stage feedback current mirror. From Table 1, it also can be found that the output impedance of the proposed current

mirror is between that of IAFCCM and the three-stage feedback current mirror.

Figure 6 is the step response of the proposed current mirror. The step curve is the input reference current which changes from 50uA to 100uA. The other curve is the output current response. From fig.6, it can be found that the proposed current mirror is stable when the input current changes.
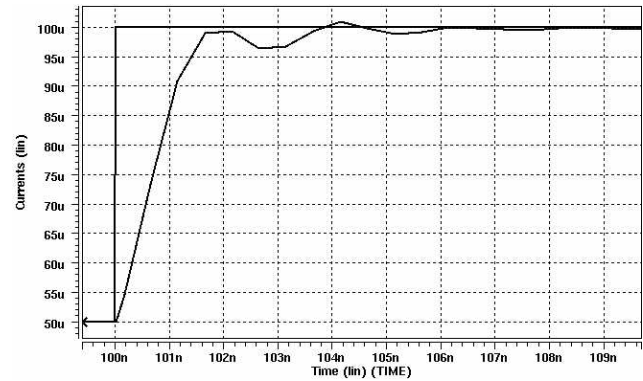

Fig.6 Step response of the proposed circuit

4   Conclusion

An appropriate current mirror circuit is proposed which has higher accuracy and lower output impedance compared with the three-stage feedback current mirror. The main advantage between the proposed circuit and the three-stage feedback current mirror is that the proposed circuit is stable without any compensation. Therefore, the proposed structure is a much suitable current mirror for use in high linearity, high output impedance current output stages.

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