CONTROL STRATEGY OF A SOLAR POWER INVERTER
(Analysis of an Advanced Third Order System)

K. H. EDELMOSER, F. A. HIMMELSTOSS
Institute of Electrical Drives and Machines
Technical University Vienna
Gusshausstr. 27-29, A-1040 Wien
AUSTRIA

Abstract: - In mains-coupled power inverter applications a reactive filter is required to interface the generator to the power grid. Conventional structures of power inverter filters, required for grid coupling operation and to fulfill EMI requirements, lead to a system which is difficult to control (because of its high system order) and problematic to realize due to unknown mains impedance behavior. The simplest structure to fulfill the requirements is a third order system. To reach the goal of an always stable and robust system here a modified third order structure in conjunction with a special compensator is used to overcome the problem of the low damped system. The structure is analyzed in detail, a controller solution is developed and some realization hints are given. The presented concept is well suited for mains coupled power inverters, especially solar inverter applications.

Key-Words: - Solar power inverter, Grid-connected, Mains filter, Inverter control, Robust control

1 Introduction

State-of-the-art solar power inverters [1,2] use simple filter structures to connect the inverter output with the power grid. Due to variable quantitative characteristic of the mains impedance [3], it is very hard to find a structure which is easy to control and well suited for all load points. Practical measurement results show main impedance values of L_3 in the range of 0.3mH up to 1.5mH, while R_3 can vary between 0.1Ω to 2Ω. This sometimes can lead to a non-predictable operating point of the inverter resulting in instable control behavior. The boundary due to di_1/dt limitations in the PWM section (c.f. Fig. 1, represented by L_1), the output impedance and the required output voltage ripple, controlled by C_1, lead to the values of these components. In case of the presented structure an additional component, the inductor L_2, is used to enhance the system performance (c.f. Fig. 1&2). It leads to the dedicated filter structure used in this application to improve the output characteristic.

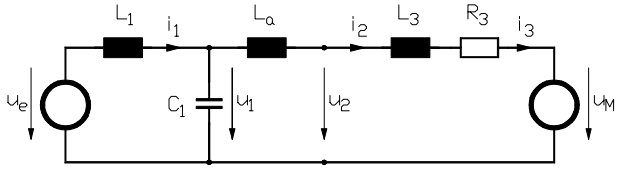

Fig. 1.a. Conventional mains coupling filter

The topology depicted in Fig. 1.b. was derived from the well-known basic third order system given in Fig. 1.a by adding a filter stage formed by L_2 & C_1.

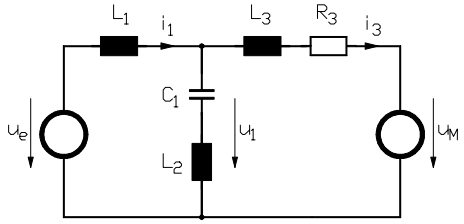

Fig. 1.b. Advanced mains coupling filter

The equivalent circuit depicted in Fig. 1.b. is the simplified converter, relevant for the control design. Here only the voltage difference $u'_e=u_e-u_M$ (this is possible due to the values of the impedances at mains frequency) determines the dynamic behavior of the output current i_3. The phase error (u_e - u_M vs. u'_e) resulting from the current i_{C1} can be neglected (c.f. circuit level analysis).

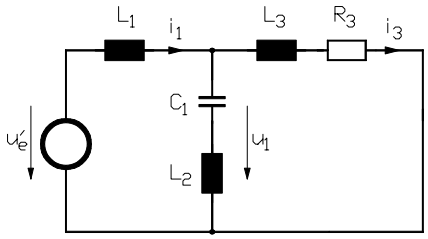

Fig. 2. Simplified model of the coupling filter

2 Mathematical analysis of the inverter

To estimate the behavior of the solution presented, the transfer function of the dynamic system depicted in Fig. 2 was derived:

$$G(s) = \frac{i_3(s)}{u'_e(s)} = \frac{n_2 \cdot s^2 + n_1 \cdot s + n_0}{d_3 \cdot s^3 + d_2 \cdot s^2 + d_1 \cdot s + d_0}, \quad (1)$$

with the coefficients

$$n_2 = L_2 \cdot C_1 \quad (2)$$

$$n_1 = 0 \quad (3)$$

$$n_0 = 1 \quad (4)$$

$$d_3 = C_1 \cdot L_1 \cdot L_2 + C_1 \cdot L_1 \cdot L_3 + C_1 \cdot L_2 \cdot L_3 \quad (5)$$

$$d_2 = C_1 \cdot L_1 \cdot R_3 + C_1 \cdot L_2 \cdot R_3 \quad (6)$$

$$d_1 = L_1 + L_3 \quad (7)$$

$$d_0 = R_3 \cdot \quad (8)$$

Due to the limitations given above, most of the component values are fixed:

$L_1 = 1\text{mH}$ (given by di_1/dt)
$L_3 = 0.75\text{mH}$ [0.3mH..1.5mH] (mains impedance)
$C_1 = 1\mu\text{F}$ (ripple minimization)
$R_3 = 0.5\Omega$ [0.1Ω .. 2Ω] (mains impedance)

Only the value of L_2 in the filter stage can be used for optimization. We can realize a further ripple minimization by building a band rejection at switching frequency (20kHz) leading to:

$L_2 = 0.065\text{mH}$ (filter stage).

In the model only the behavior near to the mains frequency is a point of interest for the output current (but not for the controller design). Due to the fact, that the switching frequency f_S is much higher than the mains frequency f_M and the selected component values given above, the voltage drop on L_1 at mains frequency can be neglected. Therefore, we can assume that $u_e \approx u'_e$.

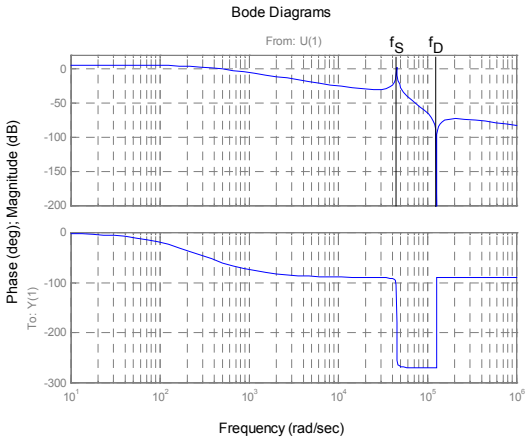

Fig. 3. Principal analysis of the mains coupling filter

As one can see in Fig. 3 the chosen structure leads to a good damping at f_D, which can be used to limit the switching noise transferred to the power grid. The overshooting at f_S has to be disarmed by the inverter control to avoid resonance effects. The next step is to have a look at the sensitivity of this structure concerning changes in the mains impedance. Here a component variation in the circuit level simulator PSPICE is used to find the results (Fig. 4)..

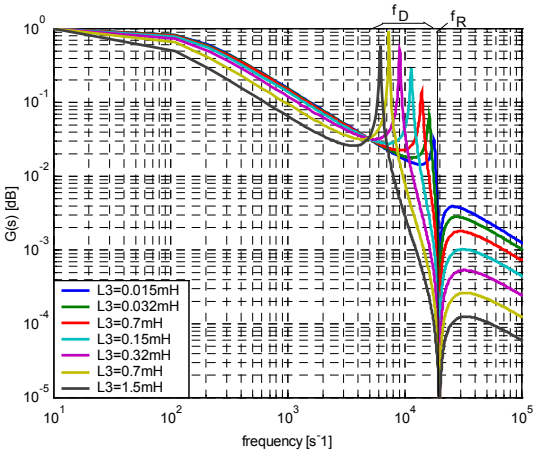

Fig. 4. Simulation results (frequency behavior due to changing of the mains impedance represented by L_3)

3 Worst case analysis

To get proper results, ideal components with additional loss resistors are used in a further simulation model depicted in Fig. 5.

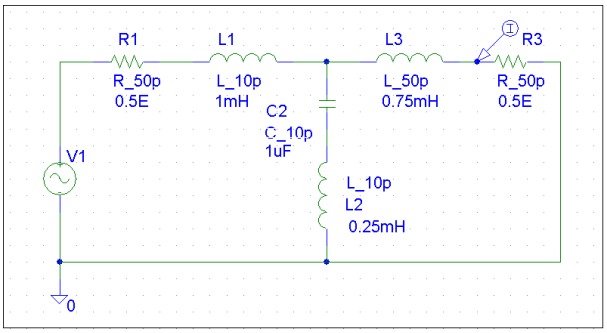

Fig. 5. Simulation model (Monte-Carlo analysis)

This model was used for the Monte-Carlo analysis of the design. Here the value in the designator represents the deviation range of the component (e.g. L_50p represents an inductor with 50% deviation). To make a representative analysis here very detailed models of the components are used. As one can see in the simulation results (c.f. Fig. 6) the high damping rates at the switching frequency f_S and at the third harmonics f_D lead to an excellent EMI suppression (care must be taken in case of comparison to practical realization; here no magnetic coupling effects are considered). Even with excessive unpredictable component values in the load section, this design leads to a satisfactory solution.

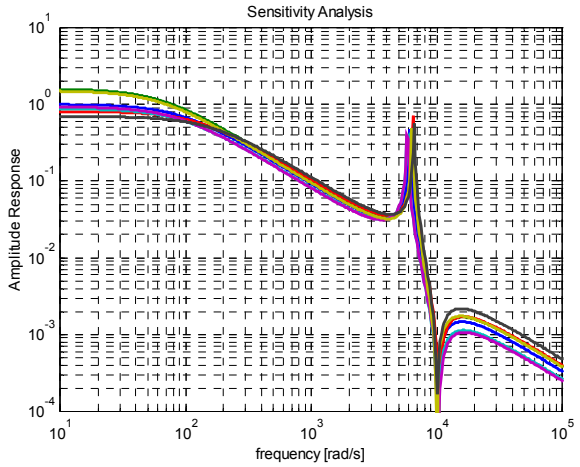

Fig. 6. Simulation results (frequency behavior, Monte Carlo analysis)

The component deviation used here is taken from real inverter components. Therefore, the theoretical results are very reliable for the worst-case analysis.

4 Control of the inverter

A further point of investigation is the control of the optimized inverter structure. Based on the results given above, it is now necessary to analyze the control behavior of the plant in detail. Fig. 6 depicts the Bode diagram of the plant with varying mains impedance:

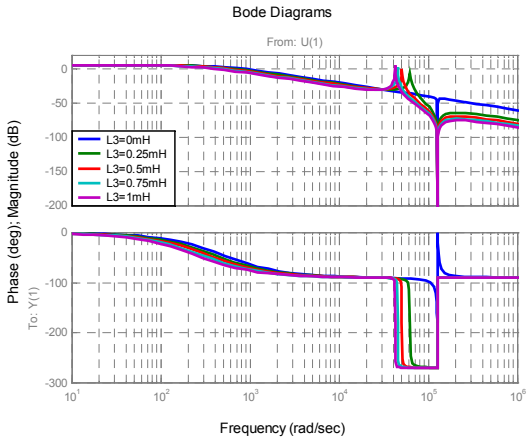

Fig. 7. Transfer function of the plant (varying mains impedance, L_3=0, 0.25, 0.5, 0.75 & 1mH)

To overcome the inaccurate system description, a compensating controller structure is selected. The compensator should affect the two double poles of the plant located at f_S and f_D to avoid instability of the controller. The mathematical analysis of the plant gives us the poles:

S_a=-166 + j45102 (mostly affected by L_3)
S_b=-166 – j45102 (mostly affected by L_3)
S_c=-280.

The poles S_a.&.S_b are mainly determined by the inverter output stage in conjunction with the mains impedance represented by L_3 (Sa & Sb mostly defined by L_2 connected in series to the parallel connection of L_1 and L_3 acting with C_1). The pole located at Sc is primarily affected by the filter stage L_2 / C_1. Therefore, here a robust control scheme is necessary to overcome the influence of the varying mains impedance.

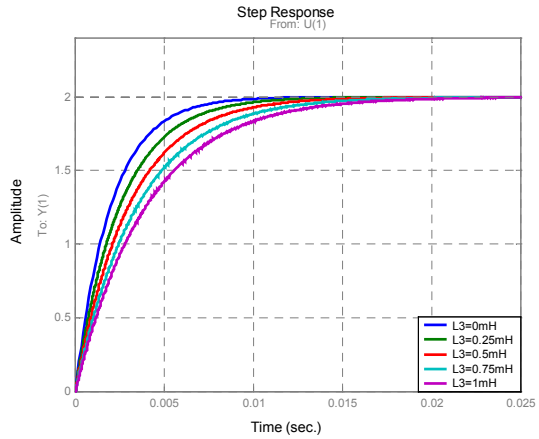

Fig. 8. Step response of the plant (varying mains impedance, L_3=0, 0.25, 0.5, 0.75 & 1mH)

As can be see from the step response depicted in Fig. 8 especially at high values of L_3 an improvement of the dynamic feasibilities of the system is necessary. In Fig. 9 the control principle is given. In a first step the two poles S_a.&.S_b are disarmed by a special compensator. Here the simulator ANA [5] is used. The compensator and the controller can simply be realized together in a microcontroller algorithm. The quantization effects and the dead-time built by the controller and the switching PWM-stage are considered in the model.

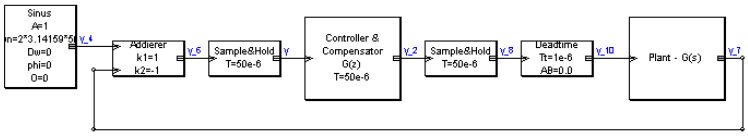

Fig. 9. Control scheme of the inverter

The transfer function of the compensator / controller section for a sampling frequency of 20kHz is given in equation (8)

$$G(z) = \frac{0.6145 - 0.453 \cdot z^{-1} + 1.471 \cdot z^{-2} - 1.621 \cdot z^{-3}}{1 - 2.376 \cdot z^{-1} + 1.973 \cdot z^{-2} - 0.6065 \cdot z^{-3}} \quad . \quad (8)$$

In Fig. 10 the transfer function of the system (compensator/controller operating the plant) by varying the mains impedance represented by L_3 is given.

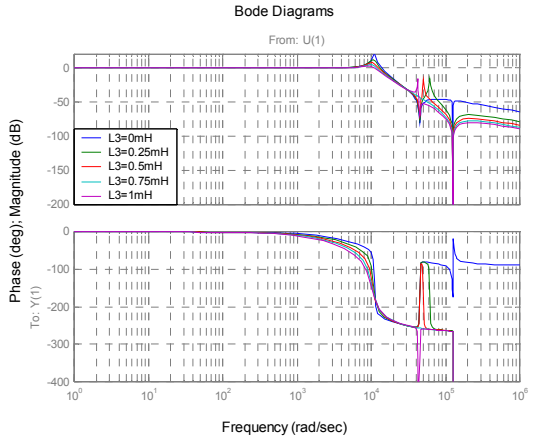

Fig. 10. Transfer function of the system (varying mains impedance, L_3=0, 0.25, 0.5, 0.75 & 1mH)

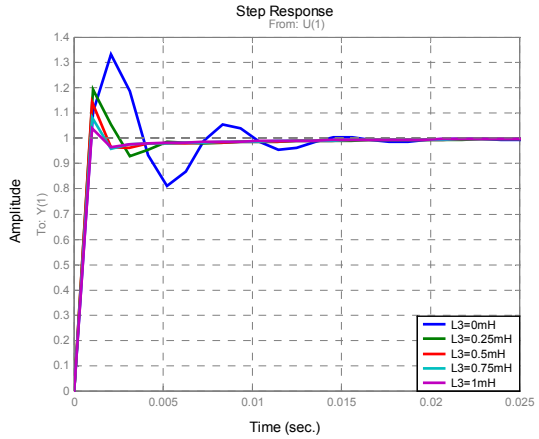

Fig. 11. Step response of the system (varying mains impedance, L_3=0, 0.25, 0.5, 0.75 & 1mH)

The dynamic analysis of the inverter is presented in Fig. 11. As one can see from the step response, the system has sufficient dynamic potential to operate at the 50 or 60Hz power grid. In addition, the sensitivity of the control loop in respect to variations in the mains impedance is in an acceptable range.

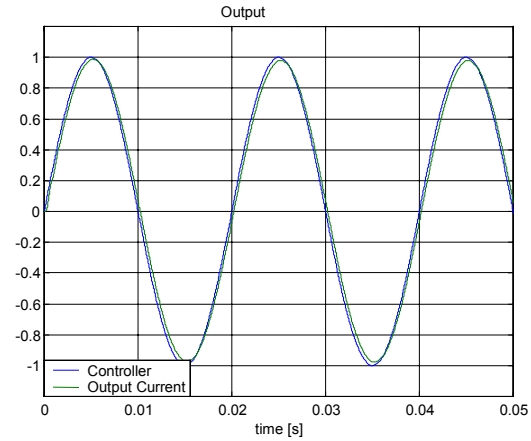

Fig.12. Controlled system at work

In Fig. 12 the resulting output shape of the inverter is given. The harmonics distortions of the output current is acceptable.

5 Realistic Operation - Simulation

This system can easily be implemented in a standard microcontroller. To analyze the effects of the realization in a cost effective 8-bit microcontroller and for serious controller design, amplitude quantization effects have also to be taken into consideration. The simulation model is given in Fig. 13. The usage of an 8-bit controller leads to an acceptable shape of the output current (c.f. Fig. 14). To estimate the resulting harmonics distortions of the inverter, the power spectrum is analyzed (c.f. Fig. 15).

Another point of interest is the shape of the output current at low loads. As one can see in Fig. 16 the output shape of the inverter is strongly deformed due to the quantization effects in the control loop.

In the model, the eight bit resolution of the A/D

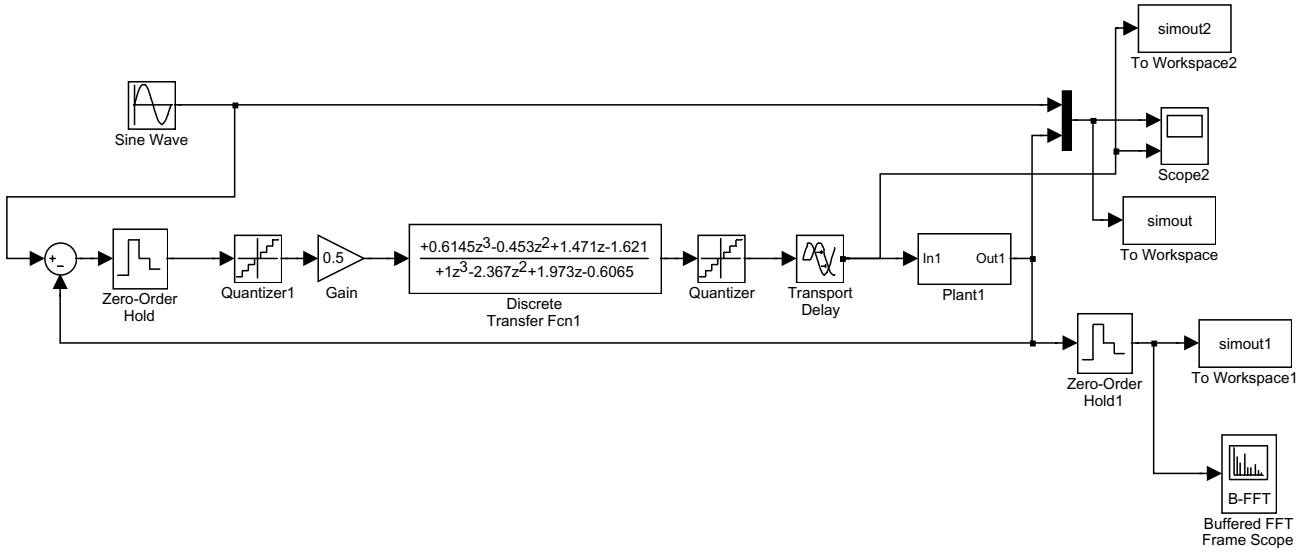

Fig.13. realistic controller model (8-Bit applications)

converters and the available 8-bit numeric is simulated. In addition, the switching delay of the PWM-stage was taken into consideration.

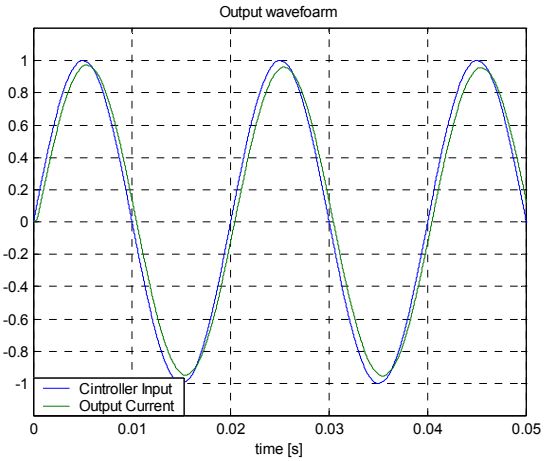

Fig.14. Digitally controlled system with 1% amplitude quantization, 50µs sampling period, including deadtime

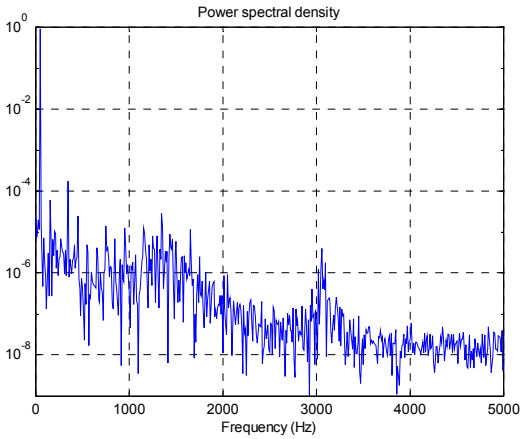

Fig.15. Output spectrum of the digitally controlled system

The simulation results given in Fig. 16 show the inverter operating at 1% of its nominal current.

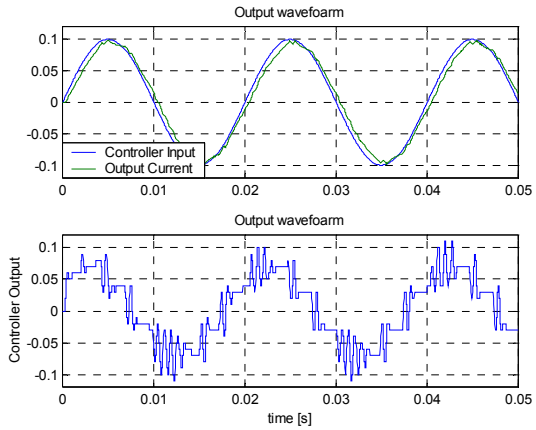

Fig. 16. Output current at low load (0.1A), lower trace controller output

This leads to a power factor of about 0.85. In Fig. 17 on the other hand the inverter is operating at full load condition.

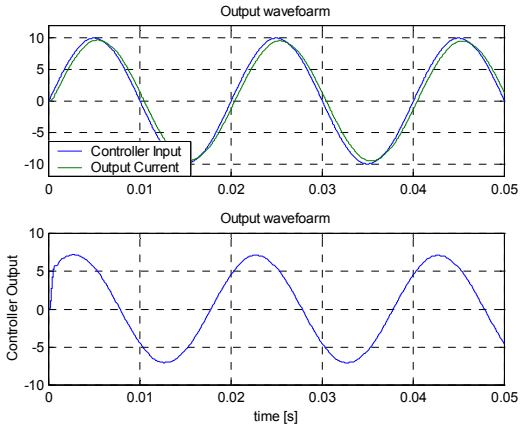

Fig. 17 Output at full load (10A), lower trace controller output

To verify the results of the mathematical analysis a circuit-level based transient simulation was performed using PSPICE. The converter was operated at 20kHz switching frequency, non-ideal power switches are used.

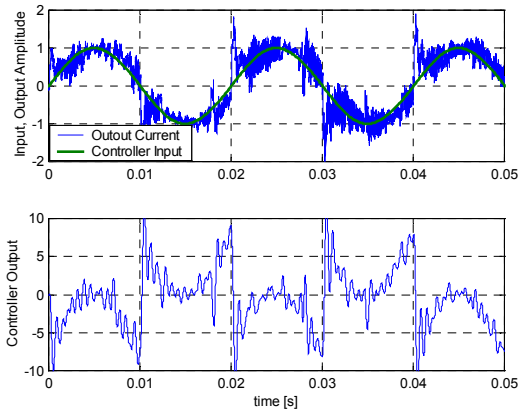

Fig. 18. Output current at low load (1A), lower trace controller output

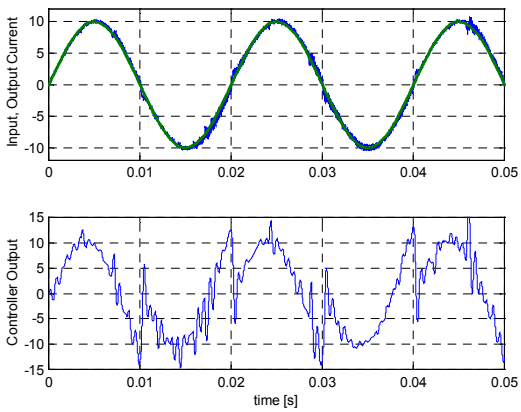

Fig. 19. Output at full load (10A), lower trace controller output

In Fig. 18 the simulation results at 1A load current (10% usage) are shown. Here the quantization effects lead to a rather noisy output current shape. The output current peaks in the upper trace of Fig. 17 result from an implemented phase error of the measuring system.
The resulting degradation of the power factor leads to these disturbances. In case of full power operation the output current leads to very acceptable results (c.f. Fig. 19).

6 Conclusion

To interface the inverter to the power grid, an insensitive mains filter is unavoidable to overcome the variations of the mains impedance. Another aspect, the effective EMC-damping has also to be taken into consideration. To control the resulting mains coupled inverter system in a stable and robust way, it is necessary to find an optimally fitted controller. Due to the weak damping, a special controller design is necessary to avoid inclination to oscillations. The solution, using a compensator filter to compensate the significant poles in conjunction with the controller, leads to a very robust and simple solution. The selected control type is well-suited for digital implementation in an embedded microcontroller. Modern microcontrollers include most of the peripherals required to implement the full system (ADC, PWM, Timers, etc.). Thus, the solution can be built very cheaply , optimal for mass products. On the other hand, the robustness of the design can help to minimize the required computation power, so additional control algorithm can be implemented at the same core (maximum power point tracking, security functions e.g. isolation monitoring on the DC side, mains impedance surveillance to prevent local operation in mains connected applications [7]).

References:

[1] M. Ryan, and R. Lorenz: "A Synchronous-Frame Controller for a Single-Phase Sine Wave Inverter", Applied Power Electronics Conference APEC '97, pp. 813-819, Atlanta, Georgia.

[2] A.Tuladhar, H. Jin, University, T. Unger, K. Mauch and Burnaby, B.C: "Control of Parallel Inverters in Distributed AC Power Supply with Consideration of the Line Impedance Effect", Applied Power Electronics Conference APEC '98, pp. 321-329, Anaheim, California.

[3] F.C. Zach: LEISTUNGSELEKTRONIK. Wien - New York: Springer. 3. Auflage 1990.

[4] A.S. Jackson ANALOG COMPUTATION, New York –Toronto – London: Mc Graw-Hill, 1960.

[5] ANA: Software for technical control simulation http://www.iert.tuwien.ac.at/.

[6] P.A. Dahono, Y.R. Bahar, Y. Sato, T. Kataoka: “Damping .of transient oscillations on the output LC filter of PWM-inverters by using a virtual resistor”, Proceedings of the 4th IEEE International Conference on Power Electronics and Drive Systems 2001, Volume: 1 , 22-25 Oct, pp.: 403 –407.

[7] K. H. Edelmoser, F. A. Himmelstoss: "Control Strategy of a Mains Coupled Solar Power Inverter (third order system)”, Proceedings of the International Symposium on Signals, Circuits and Systems SCS 2001, July 10 - 11 2001, Iasi, Romania, pp. 309-312.

ACKNOWLEDGEMENT

The authors is very much indebted to the 'Fonds zur Förderung der wissenschaftlichen Forschung' which supports the work of the Power Electronics Section at their university.