A CURRENT-MODE CMOS IMAGER USING SHUNTING INHIBITION-BASED DYNAMIC RANGE COMPRESSION

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Abstract: - An ultra-wide dynamic range current-mode CMOS imager is presented. It achieves dynamic range compression by using biologically inspired shunting inhibition vision models. As a result, it features retina-like characteristics, enabling the sensor to adapt to a wide range of scene illumination conditions. Local image contrast and edge information are preserved and can be further enhanced. The properties of the shunting inhibition-based dynamic range compression can be defined by a simple set of externally-tunable parameters, making the proposed current-mode CMOS imager architecture fully programmable. The prototype was designed in full custom ALCATEL 0.5μm CMOS technology.

Key-Words: - CMOS imager, Shunting Inhibition, Dynamic Range, edge enhancement, VLSI, System-On-Chip

1. INTRODUCTION

CMOS imagers are expected to gradually replace Charge-Coupled Devices (CCDs) as the next generation of solid-state imagers [1]. Advantages over their CCDs counterparts include lower cost, lower power consumption and most importantly "System-On-Chip" functionality [2]. A fully integrated on-chip camera system will not only slash production costs, but it is also expected to greatly improve imager performance as image processing can be coupled together with image capture [2].

Dynamic range is an important performance criterion for CMOS imagers because natural lighting levels can vary by over nine orders of magnitude [3]. The dynamic range of conventional [1] CMOS imagers is mainly limited by the photodiode quasi-linear response, causing blooming to occur for typical natural scene illumination conditions. In contrast to conventional CMOS imagers, logarithmic response CMOS imagers [4] can cope with wide scene illumination variations because the output voltage is a logarithmic function of the photocurrent. However, the sensor logarithmic response, obtained using a MOS transistor working in the subthreshold region, does not adapt to the background illumination level, resulting in a loss of local image information and hence degraded image quality [5].

In this paper, non-linear on-chip image processing is introduced, in a current-mode CMOS imager, to achieve a dynamic range compression that can preserve and further enhance local image information while providing simultaneously automatic global adaptation to the mean input light intensity. The integrated on-chip processing is based on shunting inhibition models of neurophysiological mechanisms [6] arising in biological vision systems. These mechanisms allow biological vision systems to adapt to a broad range of background illumination conditions, while still being able to capture and enhance fine details of the scene [7]. Mimicking this powerful nonlinear signal processing operation performed by the outer layers of the retina, has attracted much interest in the past decade. The trend has been towards building "silicon retinas" [8] able to emulate retinal functions such as motion detection or contrast enhancement. For instance, Moini's current mode implementation of shunting inhibition was

aimed at building an insect-vision based motion detector [9] whereas Nilson's aim was to implement one model of a multiplicative shunting neural network [10]. In contrast, the focus of this work is to improve the image quality of existing CMOS solid-state imagers. A VLSI friendly shunting inhibition-based on-chip processing is thus proposed, in this paper, to extend CMOS imager dynamic range for improved image quality. The compact, fully programmable current-mode implementation is also presented. A simple set of parameters provides a means to control externally the sensor sensitivity range, its dynamic range compression properties as well as the level of edge enhancement performed.

In the next section, shunting inhibition-based dynamic range compression is introduced and its properties presented. Section 3 describes the VLSI implementation of the current-mode CMOS imager including its architecture and operation. Finally, conclusions are drawn in Section 4.

2. SHUNTING INHIBITION-BASED DYNAMIC RANGE COMPRESSION

Shunting Inhibitory Cellular Neural Networks (SICNNs) are a class of biologically inspired neural networks introduced [6,7,11] to model the visual system [6,7,11]. A SICNN is a two-dimensional network of interconnected processing cells. In this network, interactions can only occur locally within each cell neighborhood. The state of each cell is described by the following differential equation:

$$\frac{dx_{ij}}{dt} = I_{ij} - a_{ij}x_{ij} - \sum_{m,n\in N(i,j)} w_{mn} f(x_{mn}) x_{ij} \qquad (1)$$

where the subscripts i,j refer to cell(i,j); x_{ij} is the cell state; I_{ij} is the external input to the cell; $a_{ij} > 0$ represents the decay factor of the activation; f is a non-negative activation function relating the cell's state to its output; $w_{mn} > 0$ is the synaptic weight from cell(m,n) to cell(i,j), and $N(i,j)$ is the interaction neighborhood of cell(i,j). Since $w_{mn} > 0$, the response of each cell is seen to be inhibited (Equation (1)) by its interaction neighborhood $N(i,j)$, hence the term "Shunting Inhibition" [11].

Equation (1) describes the dynamics of a feedback SICNN. In a feedforward network, the state of the cell(m,n) is replaced by the external input I_{mn} to that cell. Consequently, a feedforward SICNN is described by the following differential equation:

$$\frac{dx_{ij}}{dt} = I_{ij} - a_{ij}x_{ij} - \sum_{m,n\in N(i,j)} w_{mn} f(I_{mn}) x_{ij} \qquad (2)$$

For a time invariant input and a linear activation function $f(\xi)=\xi$, the steady state response of the feedforward SICNN described by Equation (1), is given by [11]:

$$x_{ij} = \frac{I_{ij}}{a_{ij} + \sum_{m,n\in N(i,j)} w_{mn} I_{mn}} \qquad (3)$$

Simply assume now that each pixel of the acquired image is the external input I_{ij} to the cell. The processed image will thus be represented by the states x_i, whereas the interaction neighborhood of cell(i,j) would correspond to the chosen $k\times k$ processing window. Under these conditions, the decay factor a_{ij}, weights w_{mn} and window size $k\times k$ will be the sole parameters determining the properties and the performance of the SICNN network. Dynamic range compression is mediated by the expression in the denominator of Equation (3). Tuning the decay factor a_{ij} will modulate dynamic range compression to achieve global sensor adaptation to the mean input light intensity, as illustrated in Figure 1.

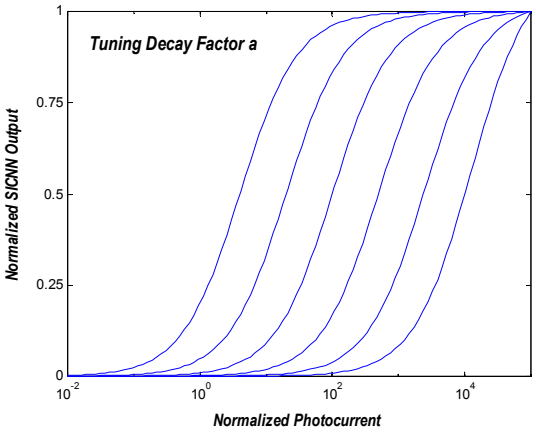

Figure 1. *The influence of decay factor "a" on the SICNN response. Note that curves are shifted to the right as the decay factor "a" is increased.*

Consequently, the sensitivity of a shunting inhibition-based CMOS imager can be optimized for any given photocurrent value range and hence for a very wide range of scene illumination conditions. In contrast, the sensitivity of logarithmic CMOS imagers cannot be

set, causing the saturation level to be reached very quickly. Tuning weights w_{mm} will set the SICNN output upper limit as illustrated in Figure 2. This provides a means to ensure that the SICNN always falls within the ADC input range, irrespective of the input photocurrent level.

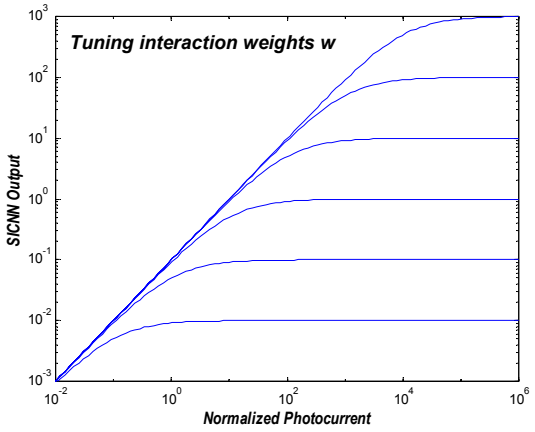

Figure 2. *The influence of interaction weights w on the SICNN response. Note that the saturation level is shifted down as weights w are increased.*

Additionally, shunting inhibition-based dynamic range compression exhibits a luminance-dependant behavior. This property is illustrated in Figure 3, where the SICNN output of a scene displaying a constant local contrast between regions 1, 2 and 3, is given for different illumination levels.

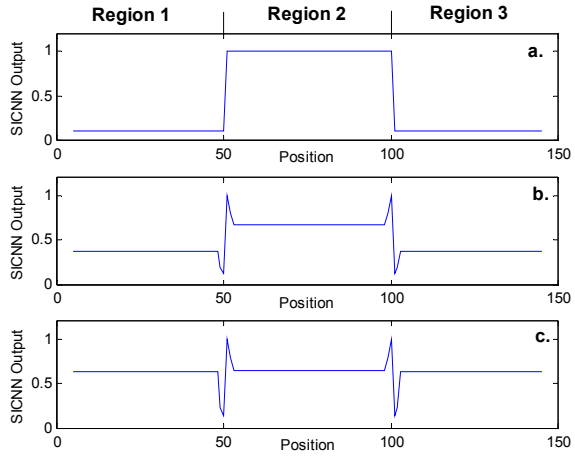

Figure 3. Normalized SICNN Output as a function of luminance: a) low, b) Medium, c) High.

The Relative Edge Enhancement (REE), defined as the peak-to-peak difference divided by the change in background luminance (Jernigan and McLean in [7]), is seen to increase (Figure 3) with luminance. This behavior is similar to that of neurophysiological mechanisms in biological retinas, upon which the proposed shunting inhibition-based dynamic range compression is modeled. No image enhancement is carried out at low illumination levels: REE=1. In contrast, at medium to high illumination levels, edge and contrast enhancement is performed: REE >1.

Furthermore, provided that the SICNN parameters w_{mm} are chosen properly, the SICNN output can give an edge-enhanced image or an edge image [12] as seen in Figure 3c.

3. VLSI IMPLEMENTATION

The core of the CMOS imager prototype (Figure 4) is a 32×32 photosensitive pixel array. Line and column readout circuitry enable the selection of either a single pixel or a window of pixels. Readout can be chosen to be sequential or random. As seen in Figure 4, pixels within a column, share the same column bus. A set of column switches controls the current flowing into the output bus. As incident photons are sensed, generated electron-hole pairs are collected at the pixel level. The photocurrent is then handout to the column bus once the row has been selected.

In the sequential mode, readout is carried out line by line. A single pixel I_{pix} is first selected and its output photocurrent is sent to a switched-current circuitry. Subsequently, the same pixel is selected along with its 8, 24 or 48 closest neighbors. The corresponding column switches are enabled so that all selected pixel outputs merge into the output bus. The current sum I_{sum} is then weighted (weight $w=w_{mn}$), through a tunable active input current mirror, before being added to an externally controlled constant current I_a. Subsequently, a control circuitry hands out simultaneously currents ($wI_{sum}+ I_a$) and I_{pix} to a current-mode ADC that digitizes $I_{pix}/(wI_{sum}+ I_a)$, i.e, the SICNN output.

The same sequence is repeated for each pixel of a selected line. In the random readout mode, pixel selection is done externally via two 5-bit address words.

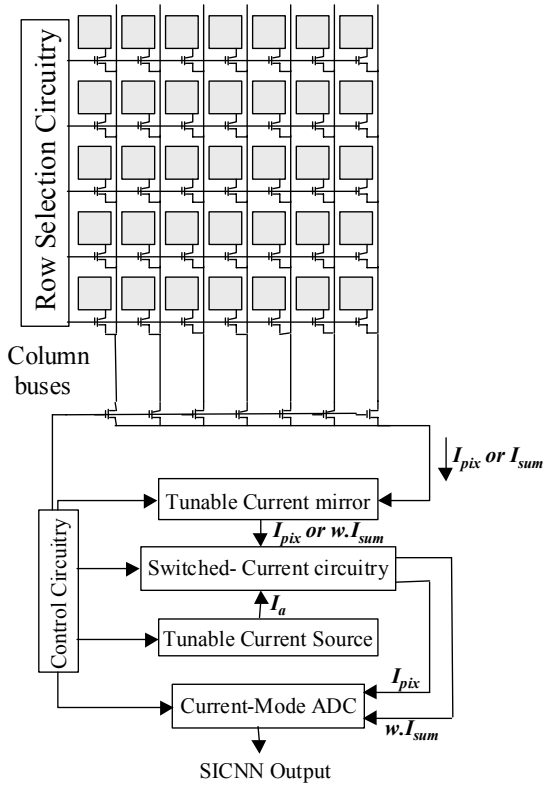

Figure 4. *Current-mode CMOS imager architecture.*

The photo-sensing element is an Ndiff/Psubstrate photodiode chosen for its high quantum efficiency. It operates in the photocurrent mode and converts incident photons into electron-hole pairs. The generated photocurrent exhibits a wide dynamic range typically from several pA at low illumination levels to several hundred nA at high illumination levels. When selected, the pixel photocurrent is sent out to its corresponding column bus. All transistors, within a pixel, operate in the subthreshold region ensuring an overall low power device operation. The output node voltage N is clamped using a tunable active current mirror, based on a customized version of the circuit topology [13] given in Figure 5. As a result, photocurrents as small as leakage currents can be readout with acceptable delays.

In Figure 5, C_{bus} refers to the large output bus capacitance whereas I_{in} is the total current flowing in the output bus. For $V_{G1}=V_{G2}$, the output node, labeled *N,* is clamped to V_{clamp} and $I_{in}\approx I_{out}$ provided that *M1* and *M2* are matched. To make the active current mirror tunable, choose $V_{G1}\neq V_{G2}$ and size transistors *M1* and *M2* so that they operate in the subthreshold region for the entire range of variation of the output bus photocurrent. Under these assumptions, *M1* and *M2* drain currents can be expressed [13] as:

$$I_{in} = I_{o1} e^{(V_{G1}-V_s)/nU_t}$$
$$I_{out} = I_{o2} e^{(V_{G2}-V_s)/nU_t} \quad \textbf{(4)}$$

where $U_t=kT/q$; V_s is the voltage at the source of both transistors *M1* and *M2*. If both transistors are properly matched, then $I_{o1}\approx I_{o2}$ and the active current mirror gain G_i will be given by:

$$G_i = \frac{I_{out}}{I_{in}} = e^{(V_{G2}-V_{G1})/nU_t} \quad \textbf{(5)}$$

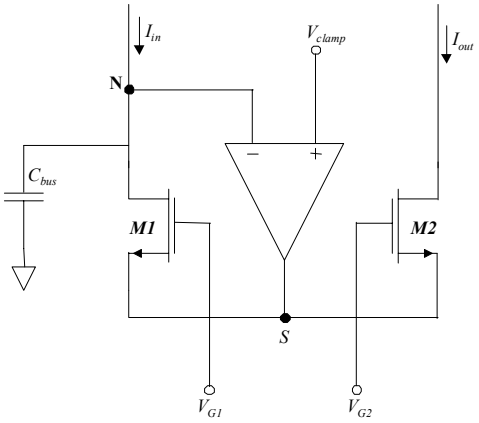

Figure 5. *Active input current mirror Topology [13]*

The output current I_{out} can thus be controlled exponentially by tuning $V_{G2}-V_{G1}$. The current can thus be amplified or attenuated over an ultra-wide dynamic range. If properly compensated, the active input current mirror, shown in Figure 5, remains stable [13] even for an arbitrary small input photocurrent I_{in}. However, as photocurrent levels approach the pA range, the current mirror becomes increasingly slower. For C_{bus}=1pF and I_{out}=10pA, careful design led to a time constant of 100ns.

As seen, the tunable active current mirror provides a mean for setting the SICNN w_{mn} parameters appearing in Equation (3). However, for a given processing window, all the weights w_{mn} will be constant and equal to the active current mirror gain G_i. Fortunately even in this last case, SICNN properties can still be preserved by a careful choice of a couple of parameters

(*a,w*). The decay factor "*a*" is implemented using a current source reference that can be externally tuned over 12 decades. Under these conditions, the proposed prototype can operate for photocurrents varying over 6 orders of magnitude.

The chip was designed in full custom ALCATEL 0.5µm CMOS technology. It occupies a total area of 10 mm^2 and comprises two CMOS imager prototypes as seen below in Figure 6. The current-mode CMOS imager, presented in this paper, is the prototype located on the left side of the layout view. The shunting inhibition based-processing circuitry is very compact as it only accounts for 12% of the prototype core area.

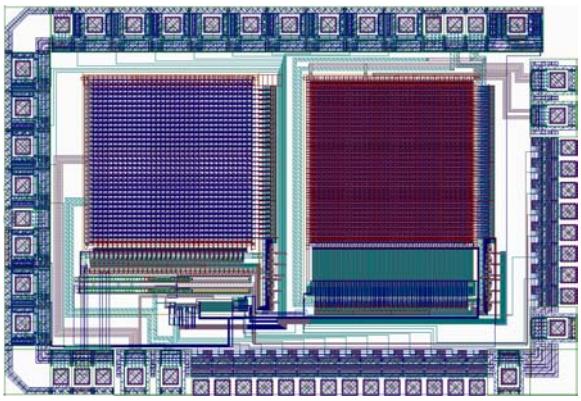

Figure 6. *Chip Layout view. Note that two CMOS imagers have been integrated on the same chip. The prototype presented in this paper is the left one.*

4. CONCLUSION

A current-mode CMOS imager, integrating shunting-inhibition based dynamic range compression, was designed in full custom ALCATEL 0.5µm CMOS technology. Fully programmable, its features are shown to include: ultra-wide dynamic range, controllable sensor sensitivity, edge and contrast preservation and/or enhancement. Similar to the behavior of neurophysiological mechanisms in biological retinas, the prototype exhibits luminance-dependent characteristics suitable for machine vision applications.

5. ACKNOWLEDGEMENTS

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