Optimized Mains Filter for Grid Connected Solar Power Inverter

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Abstract: - Conventional structures of power inverter filters, required for grid coupling operation and to fulfill EMI requirements, lead to a system, which was difficult to control (due to its high system order) and problematic to realize due to unknown mains impedance behavior. In this paper, a matching filter topology is presented, which can overcome all these limitations. It is shown, that the optimal adaptation of the presented structure leads to a simple, insensitive, easy to use and very robust solution.

Key-Words: solar power inverter, grid-connected, mains filter

1 Introduction

State of the art solar power inverters [1,2] use simple filter structures to connect the inverter output with the power grid. Due to variable quantitative characteristic of the mains impedance [3] it is very hard to find a structure, which is easy to control and well suited for all load points. Practical measurement results show main impedance values of L_3 in the range of 0.3mH up to 1.5mH, while R_3 can vary between 0.1Ω to 2Ω. This sometimes can lead to a non-predictable operating point of the inverter resulting in instable control behavior. The boundary due to di_1/dt limitations in the PWM section (c.f. Fig. 1, represented by L_1), the output impedance (minimum value given by L_2) and the required output voltage ripple, controlled by C_1, lead to the values of these components (C_3 is mostly given due to EMI-requirements). In case of the presented structure an additional component, the capacitor C_2 is used to enhance the system performance (c.f. Fig. 1&2). It leads to the dedicated filter structure used in this application to improve the output characteristic.

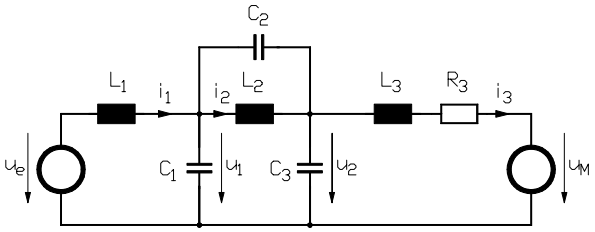

Fig. 1: Optimized mains coupling filter

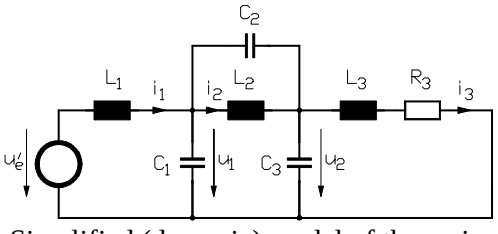

Fig. 2: Simplified (dynamic) model of the mains filter

2 Mathematical analysis of the inverter

To estimate the behavior of the solution presented, the transfer function of the dynamic system depicted in Fig. 2 was derived:

$$G(s)=\frac{i_3(s)}{u_e'(s)}=\frac{n_2\cdot s^2+n_1\cdot s+n_0}{d_5\cdot s^5+d_4\cdot s^4+d_3\cdot s^3+d_2\cdot s^2+d_1\cdot s+d_0}, \quad (1)$$

with

$$n_2=L_2\cdot C_2 \quad (2)$$

$$n_1=0 \quad (3)$$

$$n_0=1 \quad (4)$$

$$d_5=C_1\cdot C_2\cdot L_1\cdot L_2\cdot L_3+C_2\cdot C_3\cdot L_1\cdot L_2\cdot L_3+C_1\cdot C_3\cdot L_1\cdot L_2\cdot L_3 \quad (5)$$

$$d_4=C_1\cdot C_2\cdot L_1\cdot L_2\cdot R_3+C_2\cdot C_3\cdot L_1\cdot L_2\cdot R_3+C_1\cdot C_3\cdot L_1\cdot L_2\cdot R_3 \quad (6)$$

$$d_3=C_1\cdot L_1\cdot L_2+C_2\cdot L_1\cdot L_2+C_1\cdot L_1\cdot L_3+C_3\cdot L_1\cdot L_3+C_2\cdot L_2\cdot L_3+C_3\cdot L_2\cdot L_3$$

$$d_2=C_1\cdot L_1\cdot R_3+C_3\cdot L_1\cdot R_3+C_2\cdot L_2\cdot R_3+C_3\cdot L_2\cdot R_3 \quad (8)$$

$$d_1=L_1+L_2+L_3 \quad (9)$$

$$d_0=R_3 \quad (10)$$

Due to the limitations given above, most of the component values are fixed:

L_1 = 2mH (given by di_1/dt)
L_3 = 0.75mH (0.375mH..1.5mH) (mains impedance)
C_1 = 1µF (ripple minimization)
C_3 = 0.47µF (EMI-output filter)
R_3 = 0.5Ω (0.1Ω .. 2Ω) (mains impedance)

Only a part of the filter stage can be used for optimization. We can realize a further ripple minimization by building a band stop characteristic at switching frequency (20kHz) leading to:

L_2 = 0.1mH (filter stage)
C_2 = 0.075µF (filter stage)

In the model only the behavior near to the mains frequency is a point of interest. Due to the fact, that the switching frequency f_S is much higher than the mains frequency f_M and the selected component values given

above, the voltage drop on L_1 at mains frequency can be neglected. Therefore, we can assume that $u_e \approx u'_e$.
The output resistance of the inverter switching stage and the loss mechanism of the reactive components are neglected in this model. Only the dynamic behavior of the inverter output structure which is not effected from ohmic components was analyzed. In a later step also the output resistor of the PWM-section was added.

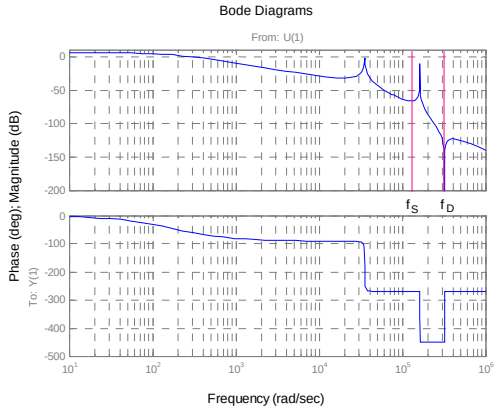

Fig. 3: Principal analysis of the mains coupling filter

As one can see in Fig. 3 the chosen structure leads to a good damping at f_S, which can be used to limit the switching noise transferred to the power grid. The second dedicated damping at f_D can also be used to damp the third harmonics of the switching inverter stage when it is located correctly. The next step is to have a look at the sensitivity of this structure concerning changes in the mains impedance. Here a component variation in the circuit level simulator PSPICE is used to find the results. Fig. 4 shows the optimized structure.

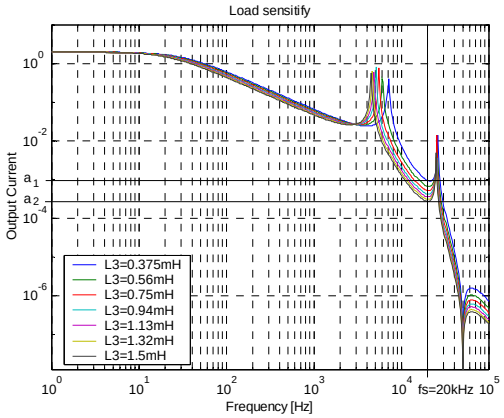

Fig. 4: Simulation results (frequency behavior due to changing of the mains impedance)

As one can see in Fig. 4 only the damping of the filter is effected by variation of the mains impedance. The damping values (theoretically from 60dB to 66dB depending on L_3) lead to an optimal solution. Here, also the third harmonic of the PWM switching stage, located at 60kHz is damped very well.

3 Worst case analysis

To get proper results ideal components with additional loss resistors are used in a further simulation model, depicted in Fig. 5. This model was used for the Monte-Carlo analysis of the design. Here the value in the designator represents the deviation range of the component (e.g. L_50p represents an inductor with 50% deviation). To make a representative analysis here very detailed models of the components are used.

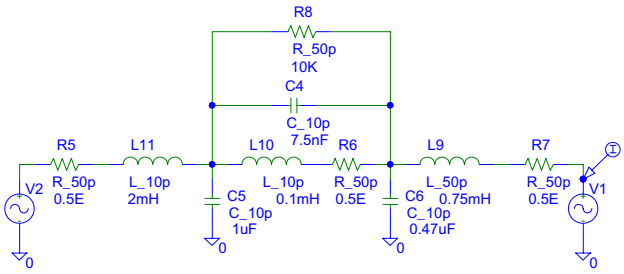

Fig. 5: Simulation model (Monte-Carlo analysis)

As one can see in the simulation results (c.f. Fig. 6) the good damping rates at the switching frequency f_S and at the third harmonics f_D lead to an excellent EMI suppression (care must be taken in case of comparison to practical realization; here no magnetic coupling effects are considered).

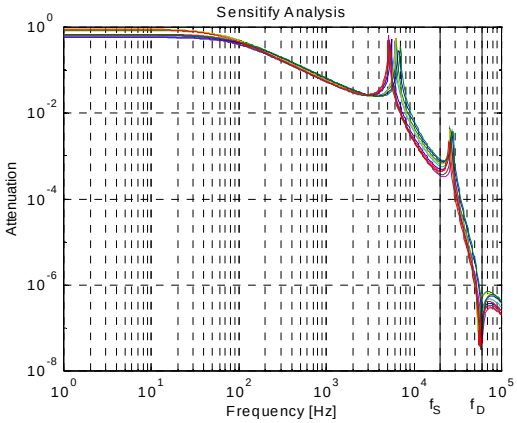

Fig. 5: Simulation results (frequency behavior, Monte Carlo analysis)

Even with excessive unpredictable component values in the load section, this design leads to a satisfactory solution. The component deviation used here is taken from real inverter components. Therefore, the theoretical results are very reliable for the worst-case analysis.

4 Control of the inverter

A further point of investigation is the control of the optimized inverter structure. Based on the results given above, it is now necessary to analyze the control behavior of the plant in detail. Fig. 6 depicts the bode diagram of the plant with varying mains impedance:

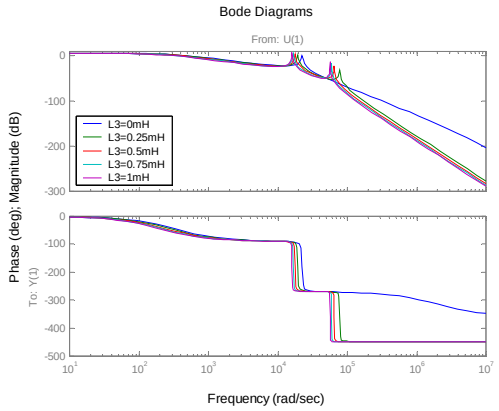

Fig. 6 Transfer function of the plant (varying mains impedance, L3=0, 0.25, 0.5, 0.75 & 1mH)

In addition, the step response of the system was analyzed:

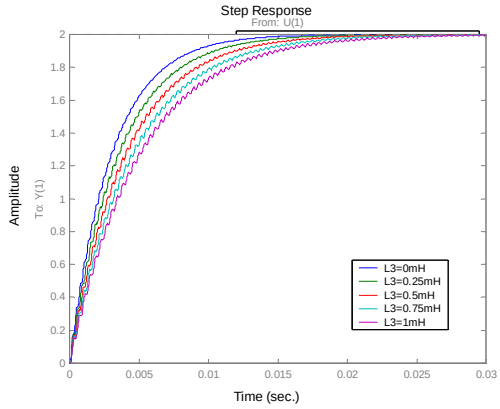

Fig. 7. Step response of the plant (varying mains impedance, L3=0, 0.25, 0.5, 0.75 & 1mH)

To overcome the inaccurate system description a compensating controller structure is selected. The compensator should affect the two double poles of the plant located at f_S and f_D to avoid instability of the controller. The mathematical analysis of the plant gives us the poles:

Sa=-20 + j*160e3
Sb=-20 – j*160e3
Sc=-230 + j*34780
Sd=-230 – j*34780
Se=-180 (approximated value, depending on L_3)

The poles Sa..Sd are mostly determined by the inverter output filter itself (Sa & Sb mostly by the filter stage L_2 / C_2, Sc & Sd mostly by the stage L_1 / C_1, while the pole Se varies with the mains impedance. So, here a compensator can be used to minimize the influence of the pole pair Sa and Sb leading to a reduced effective plant order. In Fig. 8 the control principle is given. Here, the simulator ANA [5] is used. The compensator and the controller can simple be realized together in a microcontroller algorithm. The quantization effects and the dead-time build by the controller and the switching PWM-stage is considered in the model.

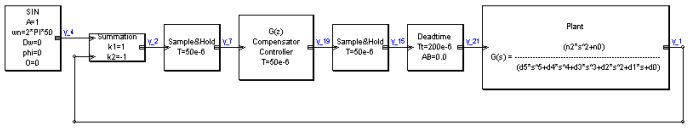

Fig. 8. Control scheme of the inverter

The transfer function of the compensator / controller section for a sampling frequency of 20kHz is given in equation (11).

$$G(z) = \frac{2.757 - 6.467 \cdot z^{-1} + 7.186 \cdot z^{-2} - 3.356 \cdot z^{-3}}{1 - 2.376 \cdot z^{-1} + 1.973 \cdot z^{-2} - 0.6065 \cdot z^{-3}} \quad (11)$$

In Fig. 9 the transfer function of the system (compensator/controller operating the plant) is given:

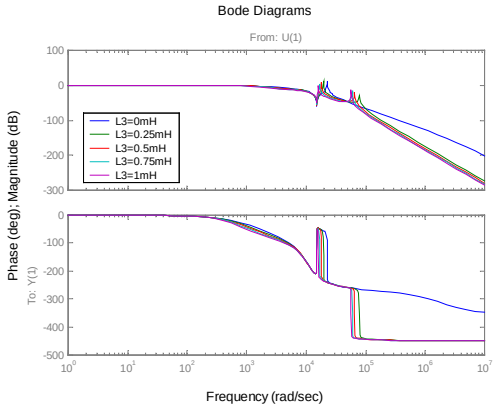

Fig. 9 Transfer function of the system (varying mains impedance, L3=0, 0.25, 0.5, 0.75 & 1mH)

The dynamic analysis of the inverter is presented in Fig. 10. As one can see from the step response, the system has sufficiently dynamic potential to operate on the 50 or 60Hz power grid. In addition, the sensitivity of the control loop in respect to variations in the mains impedance is in an acceptable range.

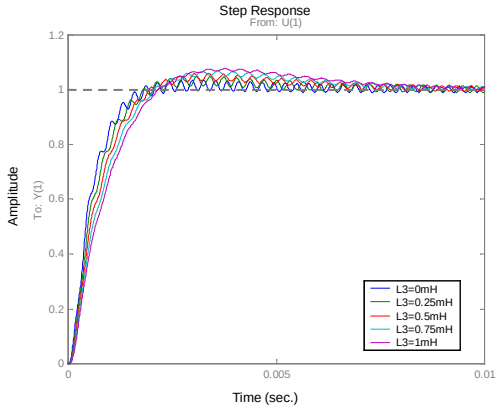

Fig. 10. Step response of the system (varying mains impedance, L3=0, 0.25, 0.5, 0.75 & 1mH)

In Fig. 11 the resulting output shape of the inverter is given. One can see the acceptable harmonics distortions of the output current.

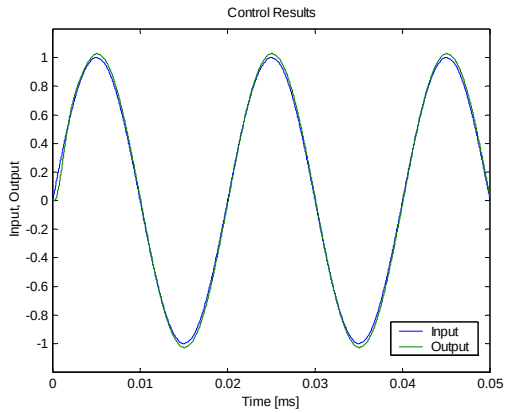

Fig.11. Controlled system at work

5 Realistic Operation - Simulation

This system can easily be implemented in a standard microcontroller. To analyze the effects of the realization in a cost effective 8-bit microcontroller and for serious controller design also amplitude quantization effects have to be taken into consideration .

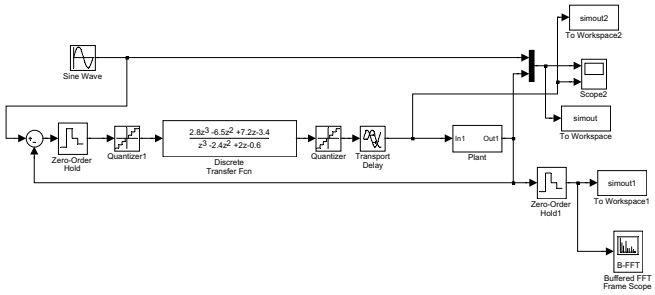

Fig.12. realistic controller model (8-Bit applications)

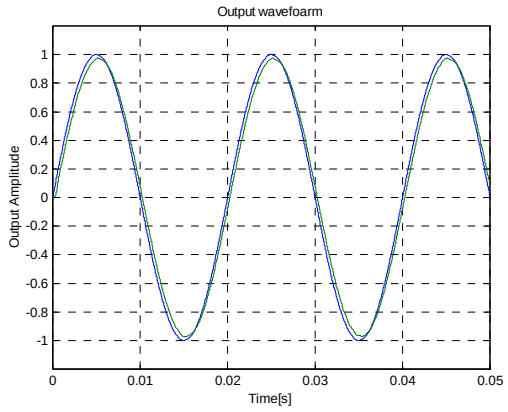

Fig.13. digital controlled system with 1% amplitude quantization, 50µs sampling period

As one can see in Fig. 13 the usage of 8-bit controller also lead to an acceptable output current shape. To estimate the resulting harmonics distortions of the inverter, the power spectrum is analyzed (c.f. Fig. 14).

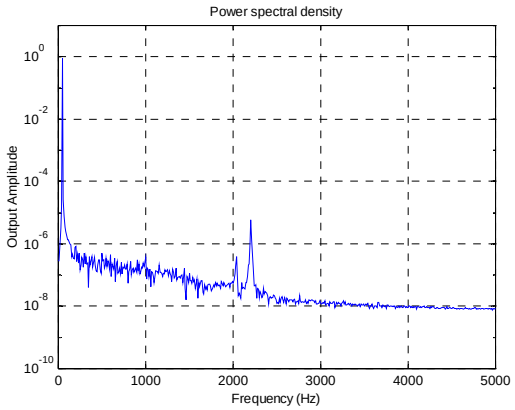

Fig.14. Output spectrum of the digitally controlled system

A further point of interest is the shape of the output current at weak load points.

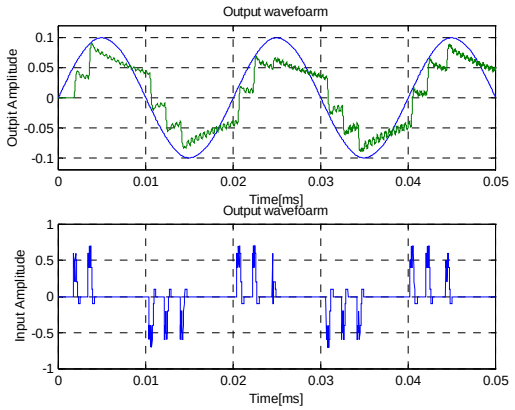

Fig. 15. Output current at weak load (0.1A), lower trace controller output

As one can see in Fig. 15 the output shape of the inverter is strongly deformed due to the quantization effects in the control loop. Here, the inverter operates only on 1% of its actual current rating. The resulting harmonic distortions leads to a power factor of about 0.85.
Contrarily, in Fig. 16 the inverter is operating at full load.

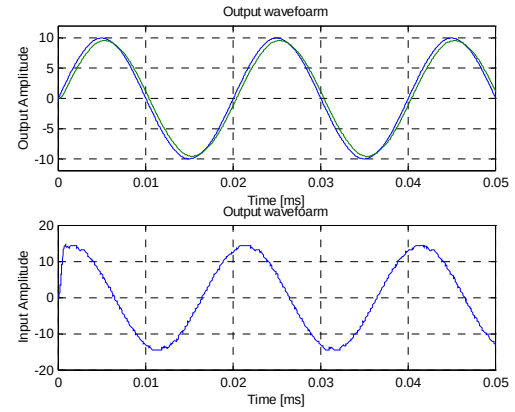

Fig. 16 Output at full load (10A), lower trace controller output

To verify the results a circuit level based simulation was performed using PSPICE. In Fig, 17 the simulation results at 1A load current (10% usage) are shown. The quantization effects and the high system order lead to a rather noisy output current shape in case of weak load current. The output current peaks in the upper trace of Fig. 17 result from an implemented phase error of the measuring system. The resulting degradation of the power factor lead to these peaks.

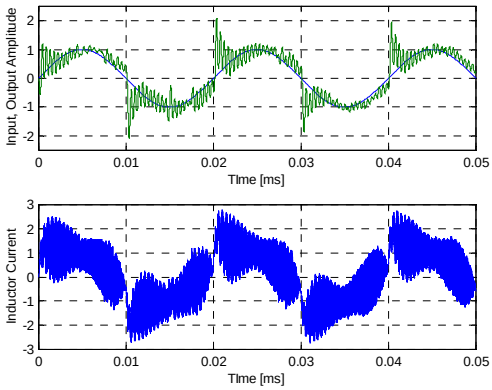

Fig. 17. Output current at weak load (1A), lower trace controller output

In case of full power operation the output current lead to very acceptable results (c.f. Fig. 18). Here a power factor (cos φ) of about 0.995can be reached.

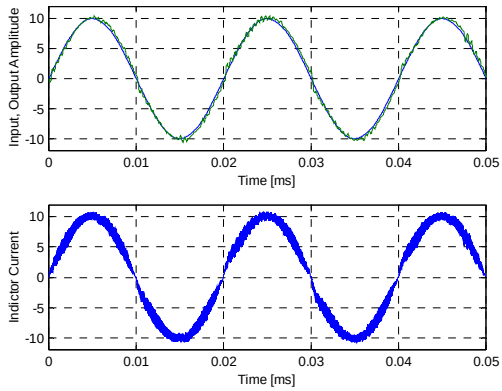

Fig. 18 Output at full load (10A), lower trace controller output

6 Practical results

In Fig. 19 the output behavior of a breadboarded 1kW inverter model (c.f. Fig. 1) is shown at 60% load factor. The source voltage u_e was generated by a PWM switching stage operating at 20kHz from a DC-link of 400V. The inverter was fully digital controlled by a PIC-17 microcontroller running at 20MHz. The mains voltage was gathered directly by a differential amplifier, the mains current is measured by a current builder from LEM. The resulting current shape leads to an acceptable power factor of 0.98.

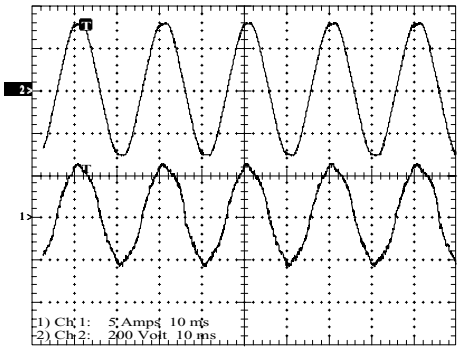

Fig. 19 Output of the laboratory inverter: mains voltage (upper trace, 200V/d), mains current (lower trace, 5A/d)

7 Conclusion

To interface the inverter to the power grid an insensitive mains filter is unavoidable to overcome the variations of the mains impedance. Also a robust controller is necessary to operate the system in an always stable and robust way. Most filter parameters are fixed by system requirements. Therefore, after designing the filter the goal is to find an optimal fitted controller for the inverter. Due to the high system order and the weak damping, a special controller design is necessary. The solution, using a pole compensating filter in conjunction with the controller, leads to a very robust and simple solution. The selected control type is well suited for digital implementation in an embedded microcontroller. Thus, the solution can be built up in a very cheap way, optimal suited for mass products. Due to the high sophisticated filter structure the resulting output current shape fulfills the requirements of the EMC and the grid operating companies.

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