A Low-Power 2GHz CMOS LNA with Active Inductor and Negative Conductance Generator

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Abstract: - This paper presents the design of a 2GHz CMOS low noise amplifier using the recently proposed CMOS active inductor [1][2][3] and negative conductance generator (NCG) [4][5][6] without any passive components. Negative feedback is used with a regulated cascode amplifier to realize a grounded active inductance and achieve power amplification. A negative conductance generator technique is utilized to extend Q-factor. The proposed low noise amplifier, which includes a common-gate configurations input matching network and output buffer for 50-Ohm environment, is designed and simulated with a standard 0.35-um digital CMOS process using HSPICE. Simulation results of the low noise amplifier tuned around 2GHz with a power gain (S_{21}) of 17.6dB, S_{11} of –11.2dB, S_{22} of –11.9dB, S_{12} of –39.4dB and a power consumption of 21.5mW from a 3.3-volt single power supply.

Key-word: - Active inductor, Negative Conductance Generator, S-parameter, Power Consumption

1. Introduction

Motivated by the growing market of RF communications system, much effort has been devoted to the implementation of RF components in a CMOS technology. The low noise amplifier is the most demanding block in a RF system. The specifications of low noise amplifier must be satisfied simultaneously including, high quality factor, large power gain, low noise figure, good impedance matching, good linearity, low power consumption and low cost. These demanding requirements have traditionally led to the implementation of discrete design or the use of exotic process. Inductors are fundamental for the design of low noise amplifiers. Most of the published low noise amplifiers are implemented by using on chip passive spiral or bond wire inductors. The quality factor of an integrated passive inductor is normally low, thus a high quality factor often requires additional processing steps. Nevertheless, by applying techniques such as the ones proposed in [6][7] it is possible to compensate the quality factor of these inductors, involving extra cost. Moreover, the inductor value is dependent on the size of the inductor [8], and not tunable, thus additional tuning circuitry is required. The chip area occupied by an integrated passive inductor is usually large compared to other components. The above difficulties can be overcome by using an active inductor. In this paper, we carry out a through description of low noise amplifier using active inductor and demonstrate how through negative conductance generator design to

increase the power gain of the low noise amplifier. The design of the active inductor is given in section **2**. The design of the negative conductance generator is given in section **3**. The design methodology of the proposed low noise amplifier is given section **4**. Simulation results are shown in **5**. Finally, the conclusion is given in section **6**.

2. The active inductor

An often-used way making active inductors is through the combination of a gyrator and a capacitor. Proposed circuits [1] such as the ones depicted in Fig. 1 exploit the parasitic within the devices. Those active inductors can operate in the GHz range.

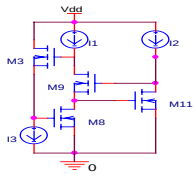

Fig. 1 Regulated cascode active inductor

It is necessary by using regulated cascode technology to reduce the inductor loss and increase the cascode gain. Base on a first small signal analysis the equivalent RLC network for this inductor is shown in Fig. 2.

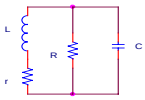

Fig. 2 Equivalent RLC model of active inductor

In order to increase the quality factor Q, the Q-enhancement technology are proposed to enhance the quality factor of the active inductor.

3. The negative conductance generator

The negative conductance generators are proposed to enhance the quality factors of the integrated passive inductors. [4][5][6] The negative conductance generator is generated by a source-follower with common gate stages as depicted in Fig. 3.The principle idea is to add a negative conductance to the active inductor so that the active inductor parallel resistive losses of R and series resistive of r can be compensated. The negative conductance generator has the negative conductance $-G_n$ connected in parallel with the active inductor. Thus the active inductor quality will be improved.

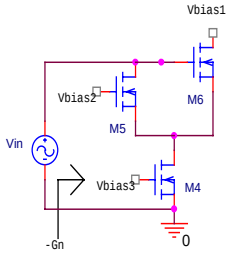

Fig. 3 The negative conductance generator

4. Low noise amplifier design methodology

A common gate CMOS low noise amplifier with an active inductor load was published. [2][3] It follows that to improve the power gain of the proposed common-gate active-inductor load low noise amplifier a large value of R, which shows in Fig. 2 is need. The current flow should be minimized to obtain a large R-value. It is possible to decrease the size of transistor to a minimum. However, good linearity requires a large bias current. Therefore, trade-offs between the power gain and linearity should be taken into account. This paper describes an alternate configuration base on attributes of active inductor and negative conductance generator to increase the value of R and decrease the r of the active inductor load so that the quality factor is increased. The negative conductance generator has the negative conductance $-G_n$ connected in parallel with the active inductor. The active inductor resistive losses of R and r can be compensated.

Therefore, the low noise amplifier has the features of high gain, small chip area and low power consumption. The form of the proposed low noise amplifier consists of four signal-processing stages, as illustrated in Fig. 4.

In this figure, the first stage, transistors M1 and M2 comprise the input amplifier stage. This common-gate configuration provides a simple 50-Ohm input impedance matching and higher linearity in contrast to a common-source configuration without source degeneration. This

common-gate configuration approach also helps to increase the effective reverse isolation in heterodyne architectures due to the signal leakage of the local oscillator from the mixer to the antenna. The

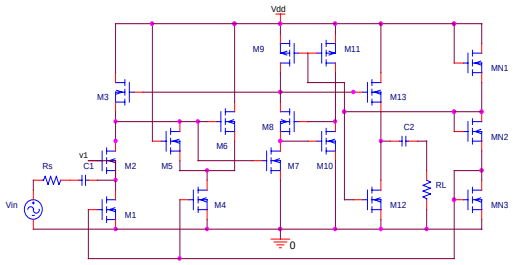

Fig.4 The proposed low noise amplifier

second stage, active inductor is constructed by transistorsM3, and M8~M12. It provides the gain of the low noise amplifier. The equivalent circuit model is shown in Fig. 2. The inductor loss reducing and cascode gain increasing can be used the regulated cascode active inductor. Transistors M10 and M12 are formed the active inductor constant current source. The third stage, negative conductance generator is constructed by transistors M4~M7. The principle idea is to generate an out-of-phase current respected to the input current and feed it back to the input voltage at the same node called the negative conductance generator, [5] which increasing the R value of the active inductor. Therefore, it is possible to improve the quality factor of the active inductor. The final stage, transistors M13 and M14 are formed the output voltage buffer. The designed amplifier is followed by a voltage buffer in order to drive a 50-Ohm resistive load and requires a large drain current to drive a low resistance load.

5. Simulation results

The complete low noise amplifier was simulated with parameters from a standard CMOS 0.35-um digital process technology using HSPICE. The normal supply voltage is 3.3V. The Figs. 5,6 show the simulated results of S21, S11, S12 and S22, where the amplifier is tuned around 2GHz. It can be seen that S21 is 17.6dB and S11, S22 and S12 are –11.2dB, -11.9dB and –39.4dB around 2GHz. The layout of the low noise amplifier is shown in Fig. 7. The area of the proposed circuit is occupied about 108um×104um, which is smaller than using the passive component of the previous work of the low noise amplifier. The power consumption of the low noise amplifier is 21.4mW. As a way of reference, a comparison between our design using the regulated cascode active inductor with negative conductance generator and other designs reported in the literature is presented in table 1.

6. Conclusion

Previous works on RF low noise amplifier have relied on the use of integrated passive inductors as tined elements. This paper presents the design of a CMOS low noise amplifier using an active inductor and negative conductance generator as a frequency selective element and Q-enhancement. The proposed circuit was verified by HSPICE simulation, which demonstrated that the center frequency and the power gain of the low noise amplifier were electronically tunable. The performance of the low noise amplifier was found to be better those employed integrated passive inductor. The advantage of this work is evidently the reduction of the chip area which about 108um×104um.

	Karanicolas	Texas A&M	Thanachayanont	This work
Technology	0.5um CMOS	0.5um CMOS	0.8um BiCMOS	0.35um CMOS
Gain(dB)	15.6	20.5	23	17.6
Freq(Hz)	900M	1G	900M	2G
Power(mW)	20	14	50	21.4
Inductor	On chip spiral	Active	Active	Active
Area(mm^2)	0.28	0.08	NA	0.012

Table 1 Comparison of low noise amplifier

Reference

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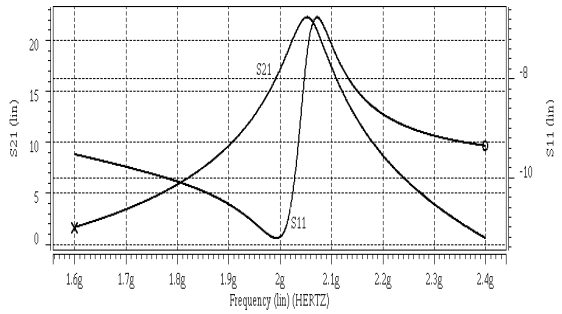

Fig. 5 S21, S11 of the low noise amplifier

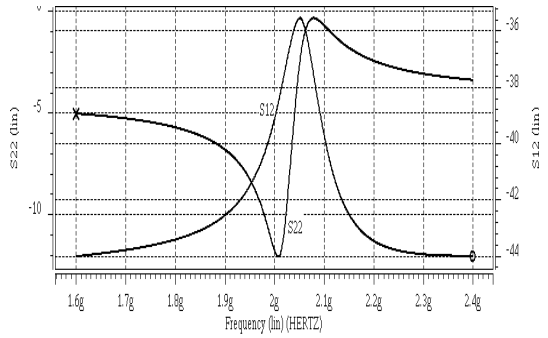

Fig. 6 S12, S22 of the low noise amplifier

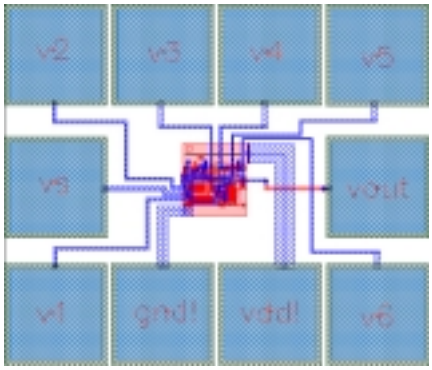

Fig. 7 The layout of the low noise amplifier