Design, Simulation and Fabrication of Interconnected Rings as High-Speed Clock Distribution Networks

MANUEL SALIM MAZA, MÓNICO LINARES ARANDA.
Departamento de Electrónica
Instituto Nacional de Astrofísica, Optica y Electrónica, INAOE
Luis Enrique Erro 1. Sta. Ma. Tonantzintla, Puebla, Pue.
MEXICO. Apdo. Postal 51 y 216. Tel/Fax 52 (222) 2663100

Abstract: - Globally asynchronous, locally synchronous clock distribution networks based on interconnected rings offer good performance regarding scalability, low clock-skew and high-speed clocking. Moreover they present linear metal-cost growth and the power consumption is directly proportional to number of rings. In this paper the design of clock distribution networks using interconnected 3-inverter stage rings at ± 45º 1:1 (one ring per sink), working as high speed clock distribution networks, is analyzed and verified by experimental measurements obtained from a fabricated chip. A typical 3.3V AMS 0.35μm CMOS N-well process was used for the design and fabrication. Experimental results showed that this proposal is a robust approach to MCM and SOCs.

Key-Words: Clock distribution networks, ring oscillators, GALS.

1. Introduction

In the last years it has been noticed a growing demand on portable equipment as cellular telephones, laptops, cameras, and audio players. It is desirable for these equipments to incorporate more functions and improve their performance in order to become more attractive to the consumers; but also keeping low power consumption that will be reflected in longer batteries' duration and life-time. These equipments do the most of its processes and functions in an integrated circuit and in digital synchronous way. This implies a clock distribution network carrying the clock signal(s) to every node that require it, for instance, hundreds of thousands of transistor gates among all the chip, representing the largest load on-chip [1].

In many applications, Clock Distribution Networks (CDN) drive the highest frequencies of the system, the largest interconnection lengths and consume 30 to 60% of the system power [2]-[4]. Therefore reducing this budget, a significant consume reduction in the whole system is obtained.

In the other hand, due to the complexity of the CDN design, tools that route, insert buffers and design the net automatically are needed. The designs obtained in this way are not reliable at frequencies above the GHz (even from 500 MHz) because there are fluctuations in the performance expected due to the interconnection models used [5]. According with this, the performance of the CDN will impact in great measure over the peak features of the system.

In this work we design and fabricate an array of 16 interconnected rings. It is demonstrated that interconnected rings are robust under fabrication process variations and can achieve high frequency with low clock skew. Experimental results agree with simulations. The rest of the paper is organized as follows. In Section 2, CDN and the interconnected ring topology used are presented. In Section 3, a fabricated array of 16 non-expanded interconnected rings, their experimental measurements of frequency, skew and power consumption are presented. In Section

4, the conclusions of this work are given.

2. Clock Distribution Networks

The maximum distance that a switching signal can travel across a region, in which the time of flight (TOF) does not limit the signal propagation, circumscribes a region known as the isochronous region. The size of this region decreases for an increasing relative length, chip area and operation frequency [1], as shown in fig. 1. The most of the systems globally distribute an original clock signal (global nets), nevertheless the systems are becoming larger and frequencies faster, then the problem of TOF is worst and nets that optimally distribute the clock signal are required [1]. New techniques have been proposed to solve this problem in clock distribution networks (CDNs); some techniques offer solutions at the process or fabrication levels such as the flip-chip package [1]; at the architecture level as asynchronous communication between blocks [7]; and the coupling of oscillators as the (local net) CDNs [8]-[12]. The interconnected rings technique has proved to generate, lock and feed a clock signal to more than one chip [9]; has been used for quadrature generators and with sleep mode [10]; and further variations oscillate faster [12] but present less robustness or output swing or consume more power or area [11].

The interconnected rings technique was presented in [11] as a globally asynchronous, locally synchronous (GALS) CDN for chip lengths from 4 to 24 mm. These lengths are a trend in larger VLSI projects (MCM and SoC) [1].

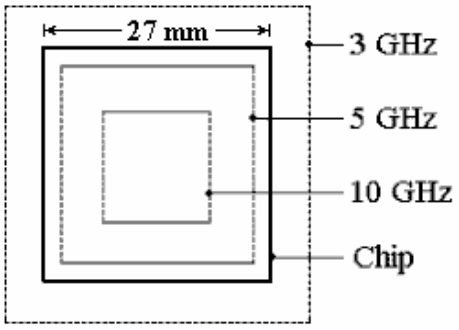

Fig. 1. Chip size and time of flight (TOF) relationship for a microprocessor with minimum dimension of 50nm and ε=1.5.

2.1 Interconnected rings

Interconnected rings have been studied for 5-stages [9] and for 3-stages with a triangular configuration [10]. The analytical model of interconnected 3-inverters rings was presented in [8]. The topology *3 inv. ±45° 1:1* was presented in [11], it showed advantageous features to be used on large systems. The structure of 16 interconnected rings of 3 inverter stages covering 8mm x 8mm chip area is shown in fig. 2. This structure was analyzed and compared with other approaches; up to 144 rings were interconnected covering a 24mm x 24mm area. It was shown that local nets have linear metal-cost and global nets have exponential metal-cost per stage, this is very important because the trend is to increase the number of stages on the nets and the complexity of global nets also increase. By repeating the basic ring, the array will keep the basic cell properties satisfactorily, and the power consumption is proportional to the number of rings [11].

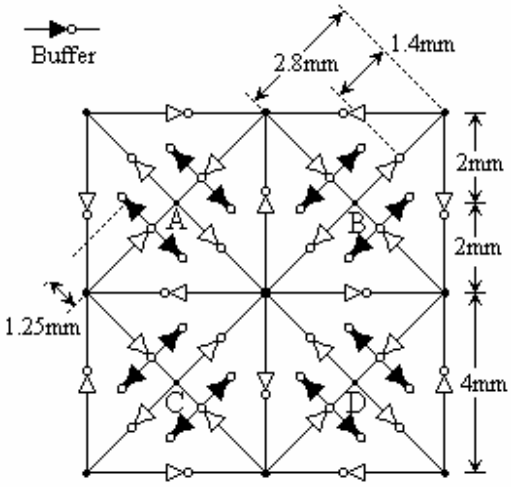

Fig. 2. 16 interconnected 3-inverter stage rings at ±45°1:1 (one ring per sink) with buffers at each sink.

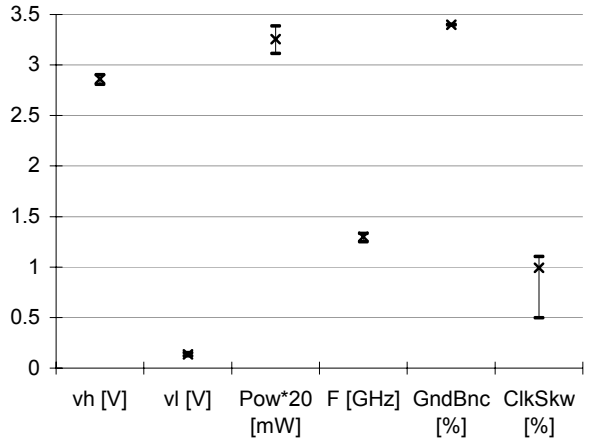

Fig. 3. Merit figures for the 16-interconnected-rings array with FD at Monte Carlo analysis.

The oscillation conditions in the interconnected rings are very easily met using an odd number N of digital inverters in the ring since they have very large gain, but for N=1 or other kind of inverters or oscillators the conditions and design could be very tight [11]. The frequency of the array is close to the frequency of a single cell, but not the same due to border effects in the lattice.

The array of 16 interconnected rings was extracted from layout using *Virtuoso* of *Cadence,* and was simulated in *HSPICE* for the AMS 0.35µm technology. The 6π-RLC model was used for the interconnections. Power consumption, operation frequency, clock skew between sinks and ground bounce measurements were performed.

In order to probe robustness of the array, a 30 cases Monte Carlo analysis to 16 interconnected rings was performed. Variations on threshold voltage V_t (23% for Nmos and 18% for Pmos transistors) and oxide thickness t_{ox} (8%) were considered. Figure 3 quickly shows how the merit figures of the 16 interconnected rings behave under V_t variations due to fabrication process; X denotes the average value, and bars denote maximum and minimal values. *vh* and *vl* stand for high and low voltage of the signal in the array. *Pow*20* stands for power consumption of the array (including 4 frequency dividers or FD); *F* stands for frequency of the array. *GndBnc* stands for ground bounce (and power bounce also), it was measured as a minimum (and maximum) voltage at every node in the array and FD and it is presented relative to Vdd (3.3V). *ClkSkw* stands for Clock Skew, it was measured as the largest difference in time at the 4 inputs of the FD and it is presented relative to the period (1/F) of the array.

3. Experimental results

16 interconnected 3-inverter non-expanded rings were fabricated using CMOS AMS 0.35µm technology. Due to the high speed of the rings and load of the measurement instruments, by-16 FD were used. The schematic and block diagram of the FD are shown in fig. 4 [13]. The FD work with an input signal of up to 1.7GHz. Four signals with the same phase in the array are the inputs of the FD and taken out of the chip. These signals are taken from nodes A to D as depicted in fig. 2 and 5a.

Figure 5-a depicts the 16 interconnected rings array and its 4 FD and fig. 5-b shows the whole chip. In fig. 6 an output waveform obtained at laboratory from the fabricated chip is shown. The values measured for clock skew, power consumption and the internal frequency (by 16) are presented in table I for two different power supplies. In fig. 7, experimental power

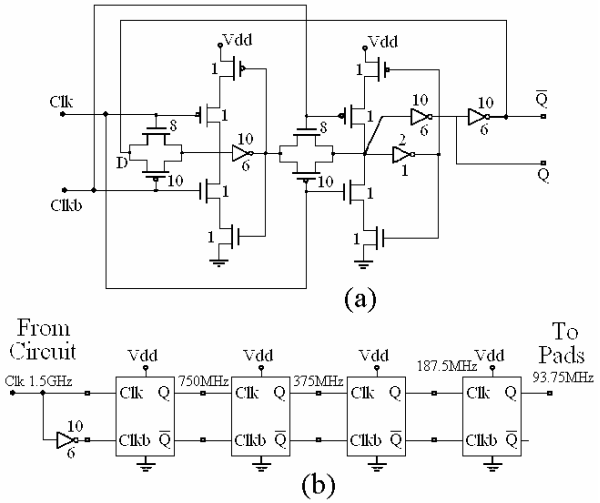

Fig. 4. By-16 Frequency Divider (FD): a) Basic divider; b) By-16 FD block diagram.

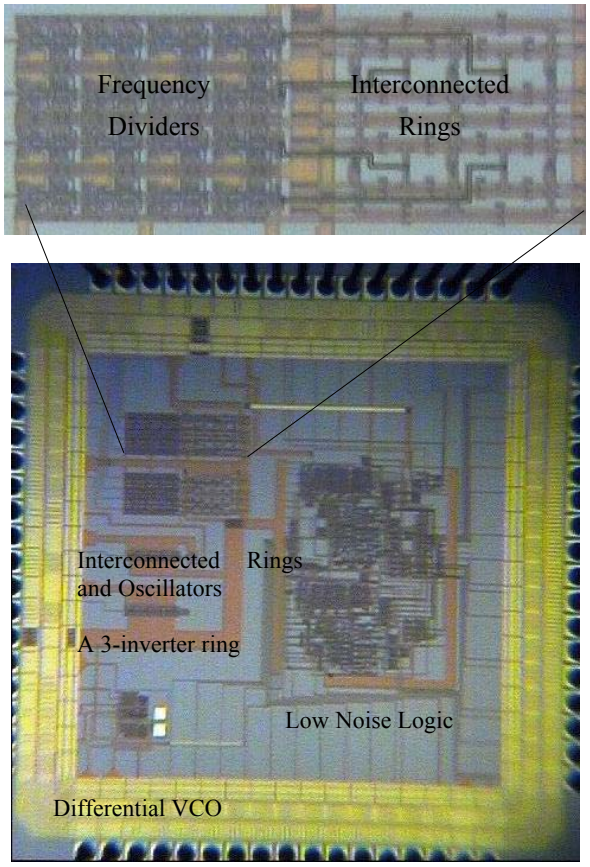

Fig. 5. Photograph of the whole chip.

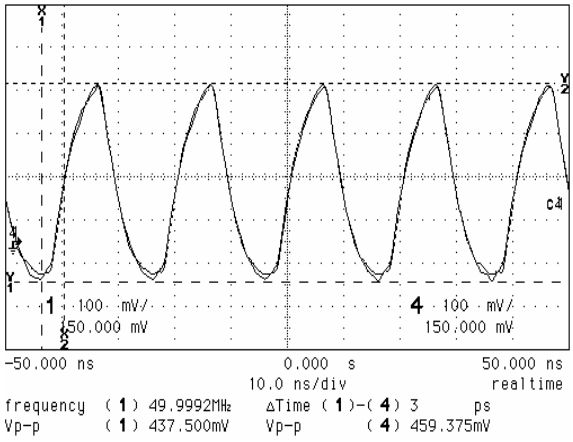

Fig. 6. Experimental output waveform from 16 interconnected rings at Vdd_{cir}=2V.

consumption and frequency vs Vdd_{cir} are depicted. Values are normalized with the maximum presented in table I for Vdd_{cir}=3.3V.

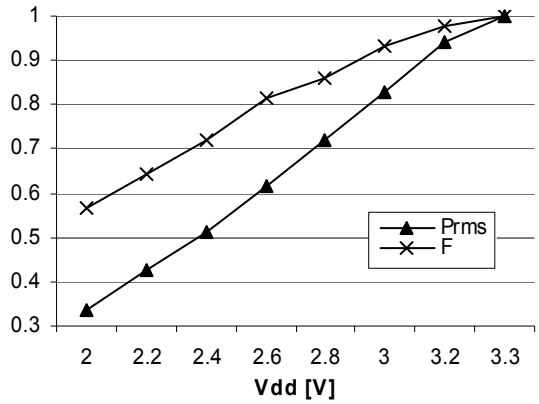

Fig. 7. Power consumption and frequency vs Vdd for the 16-interconnected-rings array. Values are normalized

Table I. Internal frequency, clock skew and power consumption of the 16-interconnected-rings array.

Vdd_{cir} [V]	2	3.3
f_{int} [GHz]	0.799	1.41
f_{ext} [MHz]	49.99	88.37
Skew [%]	0.24	17.6
P_{16R} [mW]	2.47	5.68

Table II. Simulated vs measured internal frequency and power consumption of the 16-interconnected-rings array.

	f_{int} [GHz]	$P_{16R4Div}$ [mW]
Simulation	1.29	65.1
Experimental	1.37	50.7

Notice the high linearity of power consumption and the response of frequency vs Vdd. For variations of power near 3.3V, the sensitivity of frequency is lower than at 2.2V, this is desirable because designs usually will run at the highest speed possible. Finally, in table II, a comparison of the simulated and measured frequency and power consumption of the array (including FD) is presented. f_{int} stands for frequency of the array inside the chip and $P_{16R4Div}$ stands for power

consumption of the 16 interconnected rings array and its 4 frequency dividers. Experimentally measured frequency was 6% faster and power consumption was 28% lower than expected from simulation, this is very encouraging for this kind of CDN.

4. Conclusions

Trend to use larger systems leads to more complex global nets. Interconnected rings is proposed and verified to use as GALS clock distribution networks. In this work we show that interconnected rings are robust under fabrication process variations and present power consumption linear proportional to number of rings. Experimental measurements obtained at laboratory agree satisfactorily with simulations. Very low clock skews were obtained and 1.37GHZ of frequency for 50.7mW of power consumption (including the frequency dividers).

Appendix
Current Measurement

A dedicated pin to feed the pads on the chip and one pad for each structure were used in order to get RMS current consumption of each structure, as presented in fig. 8.

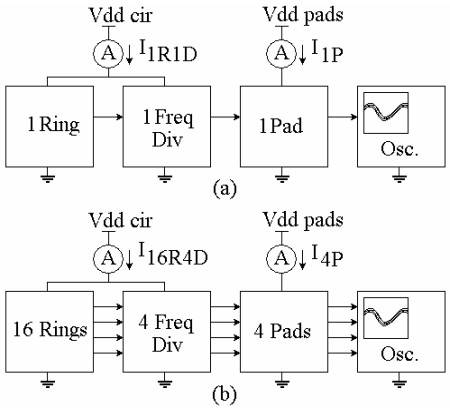

Figure 8. Setup for current measurements: a) One ring and its FD; b) 16 rings and 4 FD.

Power consumption of a single ring without frequency dividers was obtained as follows:

$$I_{16R4D} / 4 = I_{4R1D} \quad (1)$$

$$I_{4R1D} - I_{1R1D} = I_{3R} \quad (2)$$

$$I_{3R} / 3 = I_{1R} \quad (3)$$

From these steps, equivalent currents for 16 (or N) rings and the frequency dividers can be obtained.

Acknowledgments

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