New Voltage Level Shifting Circuits for High Performance CMOS Interface Applications

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Abstract: - A new design method for high performance level shifting circuits is presented in this paper. We propose two level shifting circuits that reduce problems that exist in complementary level shifting circuits described previously. Using HSPICE parameters of a 0.35um CMOS process, simulations have been performed under various capacitive loading and operating conditions. The simulation results show that our design method can achieve 16.6% low-to-high propagation delay decrease and 27.2% low-to-high power delay product improvement when converting 3.3V to 5V compared with conventional level shifting circuits. In addition, as the working voltages being converted are reduced, the design yields still greater advantage without degrading circuit performance.

Key-Words: - Level shifting, Interface, Body effect, Mixed voltage, Pre-driver, CMOS

1 Introduction

With the advancement of the semiconductor processing technology, the working supply voltage of integrated circuits（IC）is getting lower. Many integrated circuits operate at low power supplies（V_{DDL}）such as 3.3V, 2.5V and 1.8V for low power applications. But some chips made of previous generation technology can only operate at a higher supply voltage. Therefore, the voltage level shifting is an important problem for data transmission between two chips. In addition, embedded system and system-on-a-chip (SOC) are becoming more and more popular in recent years. Many circuits with different power supply voltages are sometimes made to coexist and integrated in the same chip. Then a mixed-voltage system may be required [1, 2]. However, for a conventional inverter, as shown in Fig.1(a), there exists a static current at the interface between a low voltage component to a high voltage component. That will induce a large static power consumption. To resolve the interface problem, level shifting circuits should be placed between V_{DDL} and V_{DDH} components. Moreover, at the interface, the level shifting circuit should provide a correct voltage level signal to the next stage without static power dissipation.

Fig.1(b) is a circuit diagram of the conventional complementary voltage level shifting circuit [3, 4]. In Fig.1(b), it is composed of a pre-driver circuit,

two cross-coupled PMOS transistors P1 and P2, and two NMOS transistors N1 and N2.
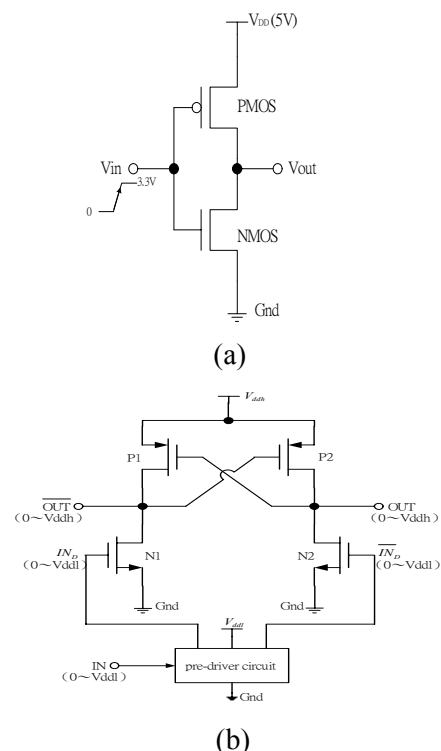

(a)

(b)

Fig.1 Prior art circuits (a)conventional inverter (b)conventional level shifting circuit

The pre-driver circuit is operated between the ground and the lower supply voltage V_{DDL}, and it provides both true and complementary input signals.

The two NMOS transistors N1 and N2 are controlled by these two complementary input signals. Above the NMOS transistors, there are the cross-coupled PMOS transistors acting as a differential latch. When the output at one side is pulled low, then the opposite PMOS transistor will turn on, and then the complementary output on the other side will be pulled high.

When the input signal IN is a logical high level so that N2 is in cutoff while N1 is biased active and provides a conducting path to ground. Thus, this consequence will pull the node $\overline{OUT}$ down to ground, which will turn P2 into conduction. When the input signal IN is switched to logic low, the operation is forced to reverse states. Here, the voltage level of the output $\overline{OUT}$ at the transition state is determined by the ratio of on resistances of transistors N1 to P1 plus N1 which are both turned on. Therefore, the pull-up transistor's strength is designed weak so as to make the on resistance of transistors P1 and P2 large enough for correct circuit operation. However, due to the size of P1 and P2 is made small, the driving capability to the next stage is reduced. Then the low-to-high propagation delay becomes longer while the high-to-low operation is fast due to the strong strength of pull-down transistors N1 and N2. Thus the low-to-high (t_{plh}) and high-to-low (t_{phl}) propagation delay times are very asymmetric. This problem exerts a great influence on the circuit operation speed and its performance is reduced.

2 Existing Level Shifting Circuits

Two existing level shifting circuits are shown in Fig.2. In Fig.2(a) [5, 6], it has the same form as the traditional level converter circuit, however, by adding two extra NMOS transistors N3 and N4 to reduce the contention problem compared with Fig.1(b) circuit. These two NMOS transistors are placed below the cross-coupled PMOS transistors to increase the switching speed of the circuit. But it has additional loading effect for the pre-driver circuit. Thus, there should be a strong driving capability of thepre-driver circuit to increase the discharge/charge capability over the nodes OUT and $\overline{OUT}$.

Let us assume that initially the input signal IN swings from low to high, NMOS transistor N1 turns on and N2 turns off. Moreover, both NMOS transistors N3 and N4 initially turn on. The node $\overline{OUT}$ will be discharged through the NMOS N3 and the node OUT will be charged via the NMOS N4 till NMOS N4 becomes off. Therefore, there are extra charging and discharging paths to speed up the output level transition in each input signal transition.
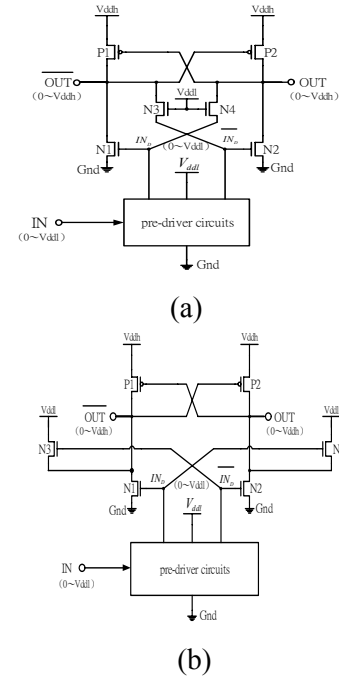

(a)

(b)

Fig.2 Existing level shifting circuits（a）prior art 1（b）prior art 2

Fig.2(b) shows a circuitry of the prior art 2 [7]. Besides the form of the traditional level converter circuit, it is also added two extra NMOS transistors N3 and N4 to provide only an additional charging path to the nodes OUT and $\overline{OUT}$. Furthermore, the extra circuit only acts in the transient period of the input signal switching. So, it can be called a transient circuit.

When the input signal IN swings from low to high, NMOS transistor N1 turns on and N2 turns off. The node $\overline{OUT}$ is discharged to the ground and turns the cross-coupled PMOS transistor P2 on. The node OUT will then be charged to high. At this moment, the extra NMOS transistor N4 initially turns on to help the node OUT charging, it is then later turned off. Therefore, the extra NMOS transistors N3 and N4 are always off in the static period.

Although the existing level shifting circuits can improve the asymmetry of t_{plh} and t_{phl}, the low-to-high transition speed is still slow. Therefore, we will propose a new design method of the level shifting circuit to speed up PMOS turn-on and therefore reduce both t_{plh} and power-delay product significantly.

3 Proposed Level Shifting Circuits

The conduction of the PMOS transistor requires that its gate voltage should be a threshold voltage $|V_t|$

lower than its source voltage. Moreover, the $|V_t|$ has relations to the body-to-source voltage V_{BS} of the MOS transistor, according to the body-effect equation given below [8, 9]. Therefore, to reduce $|V_t|$ to speed up the conduction of the PMOS transistor, a new body-controlled circuit is presented. This circuit will temporarily reduce V_{BS} of the cross-coupled PMOS P1 and P2 when the input signal IN switches its state. Then, the voltage level of the body changes back to V_{DDH} to avoid the static leakage current.

$$|V_t| = |V_{t0}| + \gamma(\sqrt{2\phi_f + V_{BS}} - \sqrt{2\phi_f}) \quad (1)$$
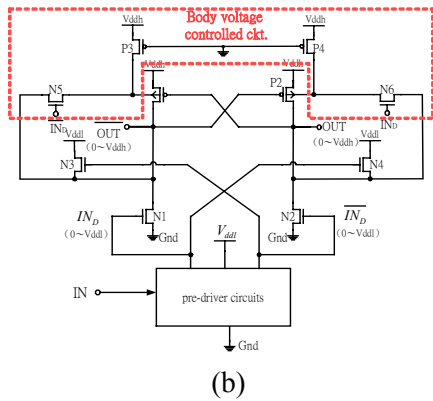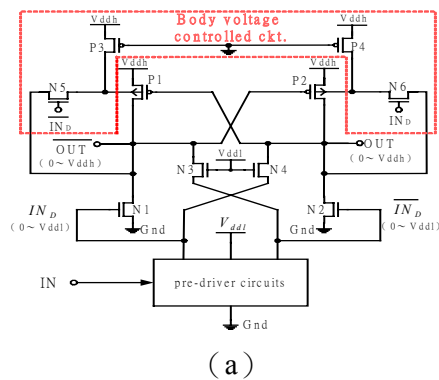

（a）

(b)

Fig.3 Proposed level shifting circuits (a)proposed circuit 1 (b)proposed circuit 2

Fig.3(a) is the proposed circuit 1 in which the body-controlled circuit is added. The body-controlled circuit includes two NMOS transistors N5 and N6, and two PMOS transistors P3 and P4. The gates of NMOS transistors N5 and N6 are controlled by $\overline{IN_D}$ and IN_D, respectively. The body of PMOS transistors P1 and P2 are connected to the drains of PMOS P3 and P4, and NMOS N5 and N6. NMOS N3 and N4 are the extra discharging and charging paths as shown in prior art 1.

When the input signal IN swings from low to high, NMOS transistor N1 turns on and N2 turns off. Then, the node $\overline{OUT}$ is discharged to the ground and turns the cross-coupled PMOS transistor P2 on. At the same time, NMOS N6 turns on, and begins to help PMOS P2 charge the node OUT more quickly. Moreover, the $|V_t|$ of the PMOS transistor P2 is reduced, because the voltage level of the body of the PMOS transistor P2 is lowered via the NMOS N6. Thus, the PMOS transistor P2 will turn on more quickly, and the node OUT will then be charged to high faster. In addition, the NMOS N6 turns off after the node OUT being charged to Vddl$-|V_t|$, and the voltage level of the body of the PMOS P2 will be charged to Vddh via the PMOS P4. Therefore, the extra NMOS transistors N5 and N6 are always off in the static period.

Fig.3(b) shows the proposed circuit 2. The proposed body-controlled circuit consists of PMOS transistors P3, P4 and NMOS transistors N5, N6. Both NMOS N3 and N4 provide the extra charging path as shown in prior art 2. Similar to the proposed circuit 1, the $|V_t|$ of PMOS P1, P2 are reduced to make P1, P2 conduct its current earlier to enhance the switching speed.

When the input signal IN swings from low to high, NMOS transistor N1 turns on and N2 turns off. Then, the node $\overline{OUT}$ is discharged to the ground and turns the cross-coupled PMOS transistor P2 on. At the same time, NMOS N6, N4 turn on, and begin to help the node OUT charging. Moreover, the $|V_t|$ of the PMOS transistor P2 is reduced, because the voltage level of the body of the PMOS transistor P2 is lowered through the NMOS N6. Thus, the PMOS transistor P2 will turn on more quickly, and the node OUT will then be charged to high faster. In addition, the NMOS N6, N4 turn off after the node OUT being charged to Vddl$-|V_t|$, and the voltage level of the body of the PMOS P2 will be charged to Vddh via the PMOS P4. Therefore, the extra NMOS transistors N5, N6 and N3, N4 are always off in the static period.

4 Simulations and Comparisons

All the level shifting circuits we described before are simulated for different capacitive loadings and voltage converting conditions using HSPICE parameters of TSMC 0.35um CMOS process. In this simulation, the pre-driver circuit is replaced by 5-stage inverters to provide a real complementary input signals. Tables 1-6 list the power consumption

(pwr), low-to-high propagation delay time (tplh), low-to-high power delay product (PDP-lh), average propagation delay time (speed) and average power delay product (average PDP) for level shifting circuits of Figs.1-3.

Tables 1 and 2 show simulation results of the proposed circuits compared with prior art circuits for 0.5pF capacitive loading with Vddl＝3.3V and Vddh＝5V, respectively. Tables 3 and 4 change Vddl to 2.5V, and Tables 5 and 6 change Vddl and Vddh to 1.8V and 3.3V, respectively.

Table 1 Simulation Results and Comparisons
(3.3V→5V, loading = 0.5pF)

	conventional	prior art 1	Proposed 1
Pwr (w)	1.62E-03	1.45E-03	1.42E-03
improvement	12.45%	2.13%	---
tplh (s)	1.96E-09	1.77E-09	1.68E-09
improvement	14.04%	4.92%	---
PDP-lh (s)	3.18E-12	2.57E-12	2.39E-12
improvement	24.74%	6.95%	---
speed (s)	1.50E-09	1.45E-09	1.399E-09
improvement	6.83%	3.38%	---
average PDP	2.44E-12	2.10E-12	1.99E-12
improvement	18.42%	5.45%	---

Table 2 Simulation Results and Comparisons
(3.3V→5V, loading = 0.5pF)

	conventional	prior art 2	Proposed 2
pwr (w)	1.62E-03	1.45E-03	1.42E-03
improvement	12.75%	2.41%	---
tplh (s)	1.96E-09	1.72E-09	1.63E-09
improvement	16.60%	5.17%	---
PDP-lh (s)	3.18E-12	2.50E-12	2.31E-12
improvement	27.24%	7.46%	---
speed (s)	1.50E-09	1.38E-09	1.338E-09
improvement	10.92%	3.22%	---
average PDP	2.44E-12	2.01E-12	1.89E-12
improvement	22.28%	5.55%	---

Table 3 Simulation Results and Comparisons
(2.5V→5V, loading = 0.5pF)

	conventional	prior art 1	Proposed 1
pwr (w)	1.71E-03	1.53E-03	1.50E-03
improvement	12.67%	2.48%	---
tplh (s)	2.09E-09	1.92E-09	1.81E-09
improvement	13.37%	5.83%	---
PDP-lh (s)	3.58E-12	2.95E-12	2.70E-12
improvement	24.34%	8.17%	---
speed (s)	2.13E-09	2.11E-09	2.028E-09
improvement	4.97%	3.84%	---
average PDP	3.66E-12	3.24E-12	3.03E-12
improvement	17.01%	6.22%	---

Table 4 Simulation Results and Comparisons
(2.5V→5V, loading = 0.5pF)

	conventional	prior art 2	Proposed 2
pwr (w)	1.71E-03	1.54E-03	1.50E-03
improvement	12.61%	2.79%	---
tplh (s)	2.09E-09	1.85E-09	1.74E-09
improvement	16.48%	5.83%	---
PDP-lh (s)	3.58E-12	2.85E-12	2.61E-12
improvement	27.01%	8.46%	---
speed (s)	2.13E-09	2.00E-09	1.936E-09
improvement	9.28%	3.08%	---
average PDP	3.66E-12	3.08E-12	2.9E-12
improvement	20.72%	5.79%	---

Table 5 Simulation Results and Comparisons
(1.8V→3.3V, loading = 0.5pF)

	conventional	prior art 1	Proposed 1
pwr (w)	7.67E-04	6.69E-04	6.46E-04
improvement	15.84%	3.51%	---
tplh (s)	3.66E-09	3.51E-09	3.33E-09
improvement	9.18%	5.27%	---
PDP-lh (s)	2.81E-12	2.35E-12	2.15E-12
improvement	23.56%	8.60%	---
Speed (s)	3.021E-09	3.12E-09	2.977E-09
improvement	1.46%	4.54%	---
Average PDP	2.32E-12	2.09E-12	1.92E-12
improvement	17.07%	7.89%	---

Table 6 Simulation Results and Comparisons
(1.8V→3.3V, loading = 0.5pF)

	conventional	prior art 2	Proposed 2
pwr (w)	7.67E-04	6.65E-04	6.38E-04
improvement	16.78%	4.00%	---
Tplh (s)	3.66E-09	3.27E-09	3.10E-09
improvement	15.32%	5.11%	---
PDP-lh (s)	2.81E-12	2.17E-12	1.98E-12
improvement	29.53%	8.91%	---
speed (s)	3.021E-09	2.78E-09	2.686E-09
improvement	11.11%	3.52%	---
average PDP	2.32E-12	1.85E-12	1.71E-12
improvement	26.02%	7.38%	---

From these simulation results, it is noted that this design method can achieve 16.6% tplh speed-up and 27.2% low-to high PDP improvement for 3.3V converting to 5V compared with the conventional level shifting circuit. Moreover, it can also achieve 5%~9% tplh decrease and low-to-high PDP enhancement compared with prior art circuits.

Figs.4-6 show the low-to-high PDP improvement percentage as the capacitive load increases for 3 conversion conditions. The low-to-high PDPs of all discussed circuits are normalized to that of the proposed circuit 2. From these simulation results, it is noted that the proposed circuit2 shows the best speed performance for all capacitive loading conditions. In addition, the proposed level shifting circuit can operate at low voltage conversion such as from 1.8V to 3.3V and can still yield more advantage in the low voltage condition.
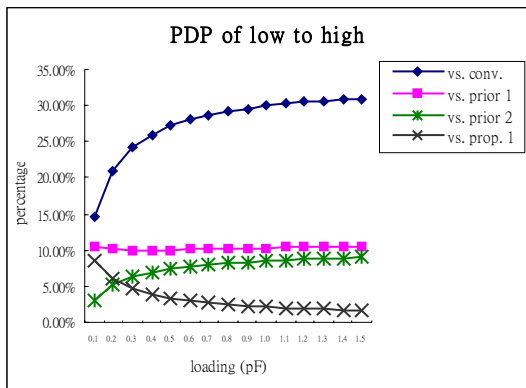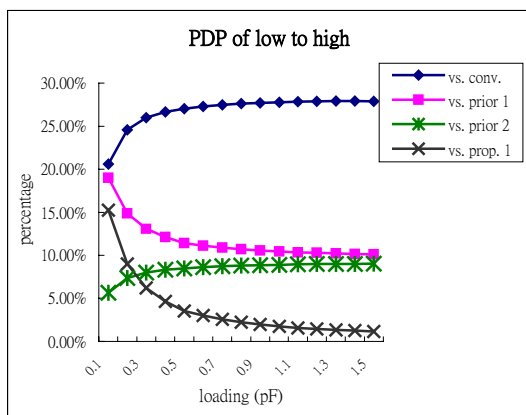

Fig.4 Improved low-to-high PDP (3.3V→5V)

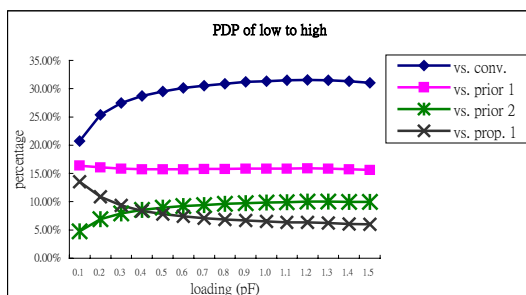Fig.5 Improved low-to-high PDP (2.5V→5V)

Fig.6 Improved low-to-high PDP (1.8V→3.3V)

5 Conclusion

In this paper, a new design method for level shifting circuits has been presented. We propose two level shifting circuits that reduce problems that exist in complementary level shifting circuits described previously. Using HSPICE parameters of a 0.35um CMOS process, simulations have been performed under various capacitive loading and operating conditions. The simulations show that our design method can achieve 16.6% low-to-high propagation delay decrease and 27.2% low-to-high power delay product improvement when converting 3.3V to 5V compared with conventional level shifting circuits. In addition, as the working voltages being converted are reduced, the design yields still greater advantage without degrading circuit performance. Moreover, this method can also be used in other kind of circuit design for improving the pull-up operation of PMOS transistors.

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