Fully Compensated Voltage Mode Delay Lines

CARLOS MUÑIZ [*], ALEJANDRO DÍAZ [*,**]
* Department of Electronics
National Institute of Astrophysics Optics and Electronics
Luis Enrique Erro No. 1, Tonantzintla Puebla. México. Tel/Fax. (+52) 222-2470517
** Department of Electronics
Technological Institute of Puebla, Av. Tecnológico No. 420, Col. Maravillas

Abstract: - A novel continuous time strategy, to compensate offset, gain errors and distortion in voltage mode delay lines is presented. Compensation arrangements, based on MIFGT transistors, allow using transistors with minimum L, extending the bandwidth to intermediate frequency, without increasing the power consumption. A third-order delay line was designed in a 0.5-μm CMOS technology. An offset compensation of 84.7% was obtained.

Key-Words: - Adaptive filters, CMOS, delay line, distortion, floating gates, offset.

1 Introduction

Adaptive Filters (AF) are systems whose structure can be self-modified to improve their behavior according to the environment. Systems identification, prediction and echo cancellation are some of their applications [1]. Analog Adaptive Filter structures (AAF) are able to handle higher frequencies and lower convergence rates than their digital counterparts, besides a reduction in power consumption and area requirements. Traversal filters (TF) are the most commonly used structures to implement AAF, however, their precision is limited by offset contributions of the delay line, the integrator and the error signal, *e(t)*, adding an excess Mean Square Error (MSE) [2]. Several compensation techniques have been proposed. Discrete time circuit level methods, like auto-zeroing and input-output offset storage, are susceptible to offset from clock-feedthrough and 1/f noise [3]. Trimming circuits techniques [4] require treatments post-fabrication, high voltages or currents, and only prevent the mismatch offset. The offset-tap technique [1] only eliminate the offset in *e(t).*

In this work, a continuous-time technique to compensate offset contributions, gain errors and distortion, in a third-order fully-differential delay line is proposed. That allows the use of minimum L in transistors, extending the bandwidth and reducing the power consumption. The compensation arrangements are based in multiple input floating gate transistors (MIFGT). The structure of the present work is as follows: Section 2 introduces the voltage follower core. Section 3 presents the proposed compensation strategy. Section 4 presents results, using HSPICE, of two third-order delay lines, uncompensated and compensated, respectively. Conclusions are enunciated in Section 5.

2 Non-Compensated Voltage Follower

The delay line is developed by connecting fully-differential feedforward voltage followers in cascade. The highly linear voltage follower of Fig.1 [5] has a extended bandwidth and a short settling time with no overshoot transient response. It consists on a differential pair M_{n2}-M_{n3} loaded with transistors M_{n5}-M_{n6}, which are coupled through transistors M_{p10}-M_{p11}. M_{n11} operates in triode, allows a linear adjusting of the common mode voltage. If M_{n2}, M_{n3}, M_{n5} and M_{n6} are identical, for low frequency analysis:

$$V_{inp} - V_{inn} = -\left(V_{outp} - V_{outn}\right), \qquad (3)$$

and for high frequencies and assuming that the follower's load is a similar stage:

$$BW \propto \frac{1}{2\pi}\frac{g_{m5}}{C_{outp}} = \frac{3K_n\left(V_{GS5} - V_{T5}\right)}{8\pi C_{ox} L_5^{\,2}}. \qquad (4)$$

A wider bandwidth if obtained if $V_{eff}=(V_{GS}-V_{TH})$ is increased and L decreased. However, under those conditions, the offset in a the differential pair increases, agreement with [3]:

$$3\sigma_{V_G} = 3\sqrt{\frac{K_n}{g_m L^2} A_{VT}\left(V_{GS} - V_{TH}\right)} = 3\frac{A_{VT}}{\sqrt{WL}}. \qquad (5)$$

3 Compensated voltage follower

The compensation strategy proposed in [5] is conceptually modified in this section in order to allow offset compensation too. If (3) is satisfied in each instant *t*, the voltage follower does not present offset, gain errors and distortion. Reordering (3):

$$V_{outp} + V_{inp} = V_{outn} + V_{inn}, \quad \text{(only DC)} \qquad (6)$$

where signal components have been eliminated. The proposed compensation consists on identifying low-frequency local control loops that allow to satisfy (6); this type of parametric feedback paths do not degrade significantly the bandwidth. From Fig.1, three possible compensation nodes are identified: V_{b2}, V_{cas1} and V_{cas2}. Feedback control circuits are realized using the four input MIFGT OPAMP of Fig.2. If negative feedback, large OPAMP gain, and identical MIFGT capacitors are used, then:

$$\left(V_{1a} - V_{1b}\right) + \left(V_{2a} - V_{2b}\right) = 0. \qquad (7)$$

where the MIFGT's capacitors can be chosen small because negative feedback reduces the parasitic capacitances effect [5]. The offset caused by the pre-stored charge on the MIFGTs can be alleviated by a UV light process [6]. Equation (6) is easily realized, according to (7), using two MIFGT OPAMPs and the voltage selection of V_{1a},V_{2a}, V_{1b},V_{2b}, shown in Fig.3. The Common Mode Feedback (CMFB) is performed, agree with (7), using other OPAMP with $V_{1a}=V_{2a}=V_{ref,}$ $V_{1b}=V_{outp}$ and $V_{2b}=V_{outn}$, where V_{ref} is the reference voltage. To higher OPAMP gain, better will be the offset, gain and distortion compensations, unfortunately, the frequency response trend to present overshooting, which causes a not constant group delay. The offsets in followers of Fig.1 and Fig. 3 can be approximated as the offset in (M_{n2}-M_{n3}, M_{n5}-M_{n6}) and M_{f1}-M_{f2}, respectively. The last one is smaller, because M_{f1} and M_{f2} can be formed with no-minimum L, since they work at low frequencies.

4 Results

Two third-order delay lines, using voltage followers of figures 1 and 3 respectively, have been designed using a 0.5-μm AMI Semiconductors technology, with V_{DD}=3 V, I_{bias}=100 μA, I_{bias2}=40 μA, and capacitors of 40 fF for the MIFGT. M_{f1} and M_{f2} are chosen with L=1.2 μm. Simulation are performed with HSPICE and level 49 MOSIS parameters. The uncompensated voltage follower presents 0.6 V_{pp} input and output signal swing, total harmonic distortion of 1.8%, 5 ns settling time and 6.9% gain error. The compensated voltage follower presents the same performance parameters, but with a total harmonic distortion of 1.2%, and a gain error of 2.6%. Distortion reduction is a consequence of offset compensation, because even harmonics produced for mismatch are reduced. A comparison of the two third order delay lines frequency responses shows that the compensated delay line presents distortion reduction of 33% and gain correction of 62%, but with a bandwidth reduction of 46.57%. The frequency response of the compensated delay line is shown in Fig.4. It can be observed that an overshoot in the frequency response is produced by the compensation net. However, it has a flat group-delay in the range from 20 MHz to 140 MHz. Fig.5 shows a comparison of the MonteCarlo results between the uncompensated delay line, and two compensated delay lines with C_{fg}= 40 fF and C_{fg}=200 fF, respectively. It can be observed an overall offset compensation between 67% and 84%, which can be improved by using larger capacitors.

5 Conclusion

A novel strategy to compensate, in continuous time, offset, gain errors and distortion in delay lines has been presented. Compensation arrangements allow to use transistors with minimum L, extending the bandwidth and reducing the power consumption. The offset compensation strategy is highly efficient, because is better to tolerate the offset in the compensation arrangement, which operates at low frequencies, that offset in the delay line, which operates at high frequencies. A offset compensation of around of 67% has been observed.

References

[1] A. Carusone and D.A. Johns, "Analogue adaptive filters: past and present," *IEE Proc. Circuits Devices Syst.*, Vol. 147, No.1, Feb. 2000.

[2] A. Shoval, et. al., “Comparison of DC Offset Effects in Four LMS Adaptive Algorithms,” *IEEE Trans. on Circuits and Systems-II: Analog and Dig. Signal Proc.*, Vol.42, No.3,March 1995.

[3] M. Steyaert, et. al. “Custom Analog Low Power Design: The problem of low voltage and mismatch,” *IEEE 1997 Custom Integrated Circuits Conference.* pp. 285-292, 1997.

[4] F. Adil and P. Hasler, “Offset Removal from Floating-Gate Differential Amplifiers and Mixers BiCMOS 1Gb7s,” in *Proc. IEEE Midwest Symp. on Circuits and Systems*, Oklahoma, 2002.

[5] G. González and J. Ramírez-Angulo, “Analog Building Blocks For A Sampled Data Fast Wavelet Transform CMOS VLSI Implementation,” *Proc. of the 1998 IEEE Int. Symposium on Circuits and Systems, ISCAS'98*, vol. 2, pp. 382-385, June 1998.

[6] K. Yang and A.G. Andreou, “The multiple input floating-gate MOS differential amplifier: An analog computational building block,” *Proc. Int. Symp. Circ. Syst.*, London, pp.37-40, May 1994.

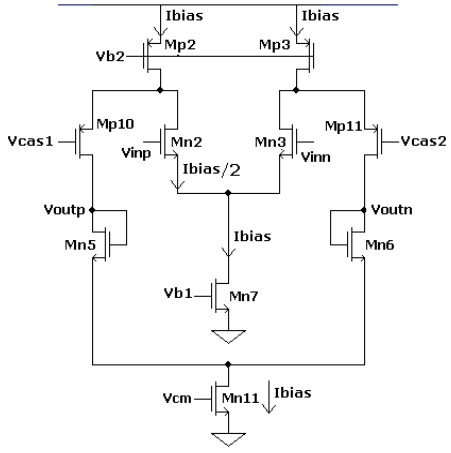

Fig. 1. Uncompensated voltage follower.

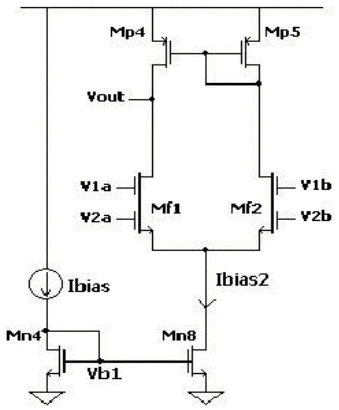

Fig. 2. Four input MIFGT OPAMP.

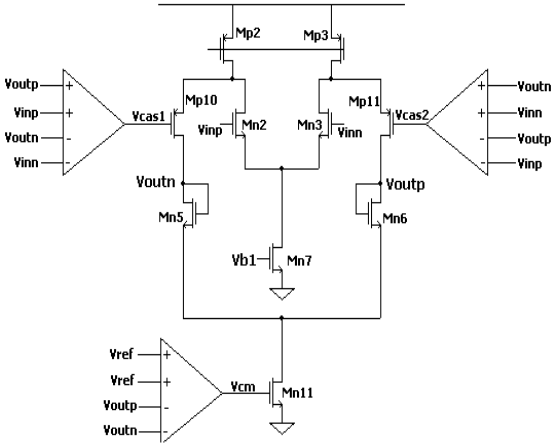

Fig. 3. Compensated voltage follower.

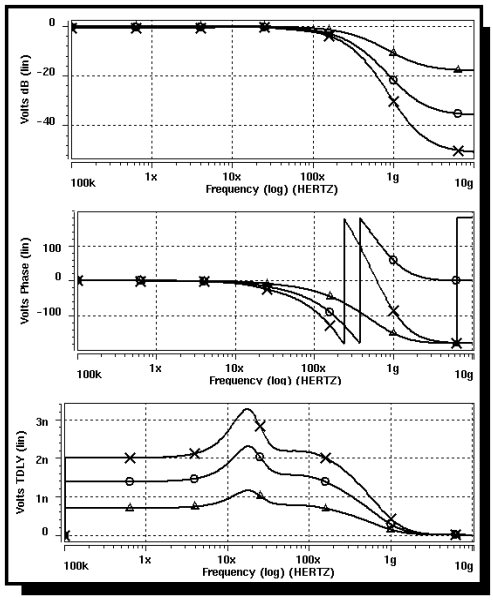

Fig. 4. Frequency response of the comp. delay line.

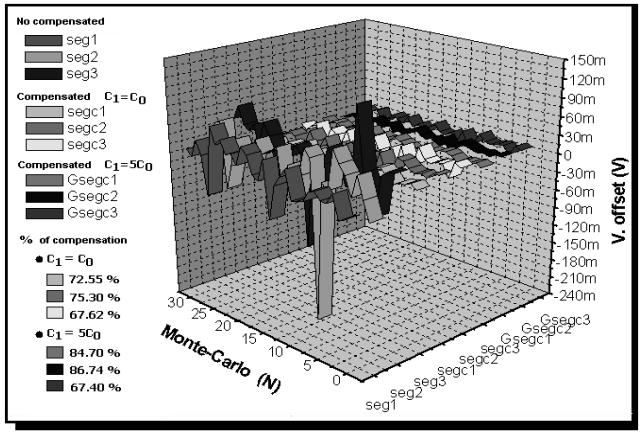

Fig. 5. MonteCarlo analysis (Offset compensation)