A NEW STRUCTURE PROPOSAL FOR A POWER SWITCHING AMPLIFIER

F. VINCENZI R. S., J. B. VIEIRA JR, E. A. COELHO, L. C. FREITAS
Faculdade de Engenharia Elétrica
Universidade Federal de Uberlândia
Campus Santa Mônica-Bloco 3N Av. João Naves de Ávila, 2160 - Uberlândia-MG
BRAZIL

Abstract: - A new current sourced switched power amplifier configuration is presented in this paper. The amplifier topology and control strategy are simple and easy to implement. This amplifier can follow the reference signal in every load condition, from no load to full load range. Moreover, it can be employed in low voltage and high voltage applications. Suitable design provides good dynamic response to low and high frequency input reference signals, without nonlinear distortion and no cross over. As a result a low THD is achieved.

Key-Words: - Switched Power Amplifier, reference signal, Low THD.

1 Introduction

A new structure proposal for a power switching amplifier is presented in this paper.

Signal power amplifiers of any nature are an object of constant research, with the intention of finding new circuits, which are capable of reproducing, faithfully the desired signal.

Within this context various electronic circuit amplifiers are known throughout technical literature. In general their construction increases the weight and the volume of the equipment, as well as the cost, especially when used in high power output applications.

For this reason new electronic circuits capable of performing the function of a power amplifier with reduced cost, weight and volume are a source of constant investigation within the scientific community.

With the objective of reaching this goal a new switching power amplifier is proposed in this paper. The proposed topology utilizes two controlled current sources and a capacitor for the amplifying purpose.

2 The Proposed Switched Power Amplifier

Fig.1 shows the new switching power amplifier circuit, in the half-bridge configuration in which two current sources, implemented by (S_1 , L_1 , V_{DC1}) and (S_2 , L_2 , V_{DC2}) association, amplifies the input reference signal on the output capacitor C_p by high frequency switching operation.

Fig.2 shows the proposed amplifier in the full-bridge configuration, which performs the same function as the half-bridge in Fig.1.

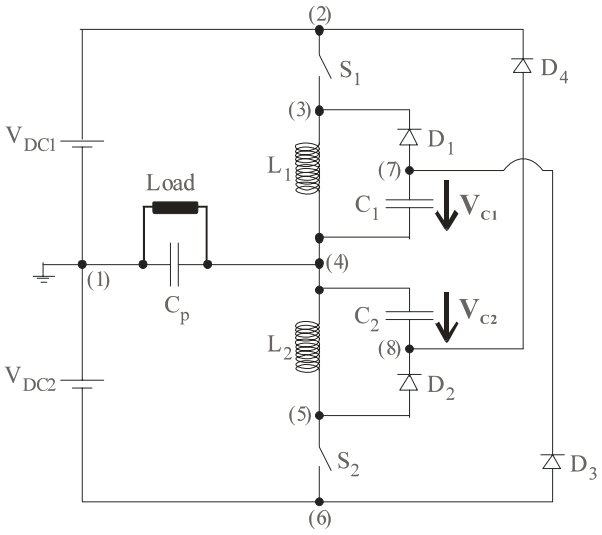

Fig.1: Half-Bridge Configuration.

For the full-bridge amplifier in Fig.2, the maximum voltage on switches is equal to that of the input voltage source, so that in the half-bridge configuration illustrated in Fig.1, the voltage on the switches is the sum of voltage sources V_{DC1} and V_{DC2}. It can be therefore concluded that the full-bridge configuration is very attractive for applications where high input voltage is utilized.

The new switching power amplifiers illustrated in Figs 1 and 2 can be used in several equipment implementations, such as:

- No-breaks
- Electronic Ballast
- Motor drives
- Voltage stabilizers
- Sound amplifiers
- AC/DC regulators

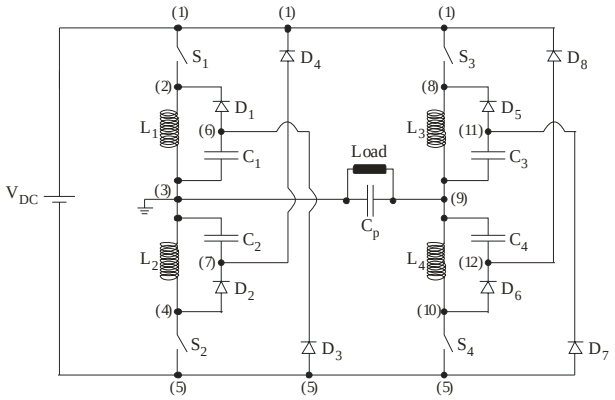

Fig.2: Full-Bridge Configuration.

This article presents the operation analysis, simulation and experimental results relative to the proposed structure in Fig.1, operating as a power switching amplifier. The experimental results obtained validate the simulations carried out by using the PSPICE software. The simulation revealed that the proposed amplifier has low THD and does not present zero crossing distortions (cross-over distortion), which shows that the proposed topology works like an operational amplifier for power applications.

3 Operation Principle

The desired signal is faithfully reproduced on the C_p capacitor because the complementary switching of S_1 and S_2 switches is originated from the comparison between the reference signal (applied to the non inverting input of the operational amplifier) and the output voltage sample (applied to the inverting input of the operational amplifier) . The comparison between the reference signal and the output voltage sample is influenced by the hysteresis limits implemented in the operational amplifier used in the control implementation.

In order to explain the operational principle of the proposed topology, the stages are described taking into consideration the following assumptions.

• The capacitor C_1 consists of a voltage source, whose direction is indicated, in Fig.1 ($V_{C1} = V_{Cp} + V_{DC2}$); .

• The capacitor C_2 consists of a voltage source, whose direction is indicated, in Fig.1 ($V_{C2} = V_{Cp} + V_{DC1}$);

• In any time instant the sum of the voltage over C_1 and C_2 is equal to the sum of the voltage sources V_{cc1} and V_{cc2} ($V_{C1} + V_{C2} = V_{DC1} + V_{DC2}$).

Due to the simplifications above, the operation stages of the proposed amplifier, for the positive half cycle of the output voltage over the capacitor C_p can be reduced in two stages, which are shown in Figs 3 and 4 and described in subsections 3.1 and 3.2. During these stages the voltage source V_{DC1} feeds, through the inductor L_1, the capacitor C_p while the V_{DC2} voltage, inductor L_2 and the load, help the output voltage modulation.

3.1 Stage 1 – Energy transference from input to output

This stage begins when the S_1 switch turns on and S2 turns off complementarily. During this stage the voltage source, through inductor L_1, feeds the output capacitor C_p and the voltage grows almost linearly.

Stage one finishes when the output voltage (V_{Cp}) reaches the upper limit of the hysteresis causing the comparator output state to change turning S_1 off and S2 on complementarily. Part of the stored energy in the L_2 inductor from the previous stage, is transferred to the C_2 capacitor which is considered, for the purpose of simplification, a dependent voltage source.

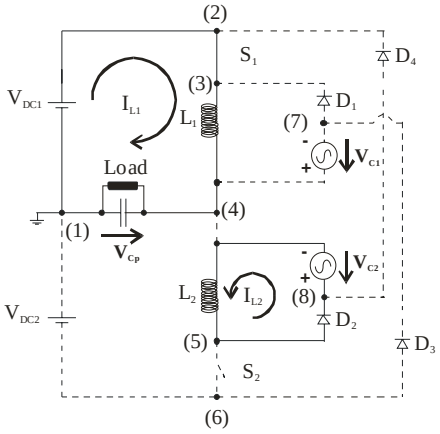

Fig.3: Stage 1 - Energy transference to the load.

3.2 Stage 2 – Auxiliary to the modulation of the output voltage.

As illustrated in Figure 4, this stage begins when S_2 switch turns on and S_1 switch turns off complementarily. During this stage the voltage source V_{DC2}, through the inductor L_2, feeds the C_p capacitor in order to decrease its voltage.

This stage finishes when the output voltage (V_{Load}) reaches the lower limit of the hysteresis causing the comparator output state to change turning S_1 on and S_2 off complementarily. Part of stored energy in the L_1 inductor from the, previous stage, is transferred to the C_1 capacitor which is considered a dependent voltage source.

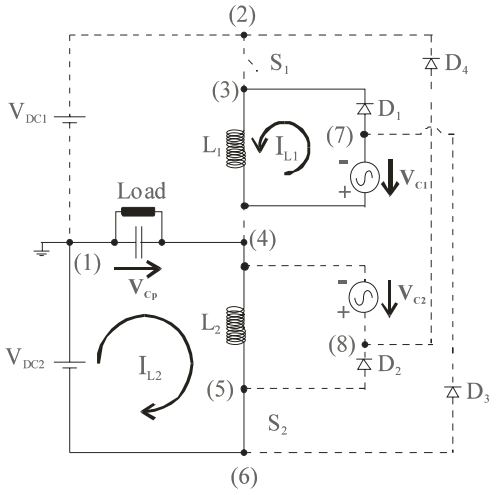

Fig.4: Stage 2 – Both the load and the inductor L_2 help to decrease the voltage on the capacitor C_p.

The stages of the operation described above are invariant to the negative semi-cycle output voltage (V_{Cp}). Therefore in this case the voltage source (V_{DC2}) controls the voltage of the C_p capacitor by means of the L_2 inductor while voltage source V_{DC1}, together with the load act as auxiliaries on the V_{Cp} modulation.

4 Design Guide

The maximum slew-rate has to be considered for correct amplifier design. To determine the slew rate it is necessary to choose either triangle waves or sine waves as an input signal to test the amplifier. It makes no sense to talk about the slew rate of a square wave, since theoretically the slew rate of a perfect square wave is infinite.

The mathematical analysis based on sine wave input signal simplifies the mathematics study and in this case the instantaneous input signal is represented by equation (1).

$$V(t) = V_{pk}.\sin(\omega.t) \qquad (1)$$

where:

- V_{pk} - is the peak potential of the sine wave;
- ω - is the angular velocity, or radian frequency, and it is equal to $2.\pi.f$;
- *t* - is the instantaneous time of interest.

The differentiation of equation (1) results in the desired slew-rate, equation (2).

$$\frac{V(t)}{dt} = \omega.V_{pk}.\cos(\omega.t) \qquad (2)$$

The maximum rate occurs at the zero crossing for the maximum frequency to be amplified when $\cos(0) = 1$. This means that the term $\cos(\omega.t)$ in equation (2) can be dropped resulting in the equation (3).

$$\frac{V(t)}{dt} = \omega.V_{pk} \qquad (3)$$

Equation (4) relates current and capacitance. This equation is very important to calculate the current needed to produce the desired slew rate on a capacitor.

$$I = C.\frac{dV}{dt} \qquad (4)$$

Combining (3) and (4), it is found that the current can be calculated by equation (5).

$$I_{pk} = 2.\pi.f_{\max}.C.V_{pk} \qquad (5)$$

where:

$f_{\max}$ - is the maximum frequency to be amplified

For the positive slope on C_p capacitor Figures 5 and 6 show that inductor L_1 charges capacitors C_p and C_1 and discharges capacitor C_2. The charging and discharging processes happen basically at the same time because the switching frequency is high. So the circuit shown in Figure 7 can be used to find the current equation that produces the maximum slew-rate.

where:

- capacitor C_T is the sum of capacitances C_p, C_1 and C_2;
- at t = 0s the inductor's current is zero;
- *at t = 0s the capacitor's voltage is zero.*

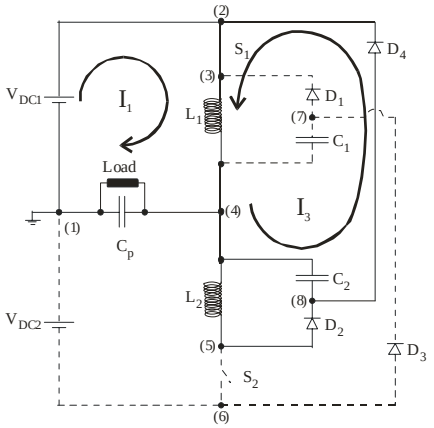

Fig.5: Charging C_p and discharging C_2 (Positive Slope).

Equation (6) shows the instantaneous current in the LC circuit shown in Figure 7.

$$I(t) = \frac{V_{DC}}{Zo}.\cos(\omega.t) \qquad (6)$$

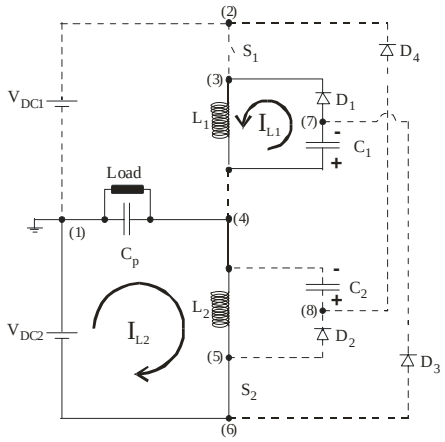

Fig.6: Charging C_1 and discharging C_p (Positive Slope).

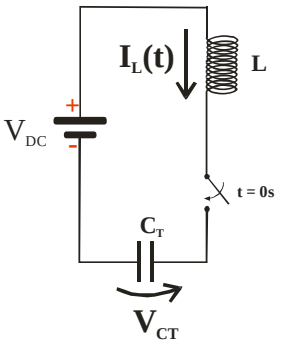

Fig.7: LC equivalent circuit (Positive Slope).

The maximum current occurs when t=0 since $\cos(0) = 1$. This means that the term in Equation (6) can be dropped resulting in Equation (7).

$$I_{pk} = \frac{V_{DC}}{Zo} \qquad (7)$$

where:

$$Zo = \sqrt{\frac{L}{C_T}}$$

Combining Equation (5) and (7) results in Equation (8).

$$L = \frac{{V_{DC}}^2}{4.\pi^2.{f_{\max}}^2.{V_{pk}}^2.C_T} \qquad (8)$$

Notice how driving impedance is never considered. This is because it has nothing to do with slew-rate. The impedance is considered for frequency response and/or filters analysis. It is interesting to note that the maximum slew-rate occurs (at the zero crossing) when the current is maximum and voltage is zero. If the voltage is zero the impedance is unable to drive any current.

The total capacitance C_T is the sum of capacitances C_p , C_1 and C_2. Good values for C_1 and C_2 are $C_p \le (C_1 = C_2) \le 2.C_p$.

Table 1: Design Specification

COMPONENTES	VALUES
Po	150W
$Vo_{(pk)}$	95V
$f_{\max}$	5kHz
$I_{L1(pk)} = I_{L2(pk)}$	$\simeq I_{LOAD}$

Table 1 shows a 150W switched power amplifier specification.

The nominal RMS load voltage (Vo) is:

$$Vo = \frac{Vo_{(pk)}}{\sqrt{2}} \qquad (9)$$

$$Vo = \frac{95}{\sqrt{2}} = 67,2V$$

$$Po = Vo.Io \qquad (10)$$

where:

Po = nominal RMS output power
Vo = nominal RMS output voltage
Io = nominal RMS output current

The nominal RMS load current is given by Equation (10).

$$Io = \frac{150W}{67,2V} = 2,23A$$

The load peak current is:

$$Io_{(pk)} = 2,23A.\sqrt{2} = 3,15A$$

Using Equation 5 C_T is calculated as follow:

$$C_T = \frac{3{,}15A}{2.\pi.5000kHz.95V} = 1{,}1\mu F$$

Making $C_1 = C_2 = 2.C_S$ the capacitance C_p, C_1 and C_2 is:

$$C_1 = C_2 = \frac{2}{5}.C_T = \frac{2}{5}.1{,}1\mu F = 440nF$$

$$C_p = \frac{C_T}{5} = \frac{1{,}1\mu F}{5} = 220nF$$

Finally the L_1 and L_2 inductance value is obtained by Equation 8.

$$L_1 = L_2 = \frac{(100V)^2}{4.\pi^2.(95V)^2.(5kHz)^2.(1{,}1.10^{-6}\mu F)}$$

$$L_1 = L_2 = 1mH$$

5 Simulation and Experimental Results

The simulation results were obtained by use of the PSPICE software and all the mathematical models of the components utilized are of real model components present in the libraries supplied with the software. Experimental results were obtained from a prototype implemented in a laboratory. The parameters used for simulation and prototyping are presented in Table 2.

With the intent of illustrating the amplifier's operation results, as well as to help in their understanding and comparison, the simulation and experimental results have been put in a parallel column table as shown in Figs 9 to 14.

Fig. 9 (a) presents on the upper wave form, the output voltage V_{Cp} and on the lower wave form the reference signal AM, obtained by simulation.

Fig. 10 (a) shows the simulation results, where the output voltage V_{Cp} is shown on the upper wave form and the senoidal reference signal on the lower wave form.

These simulation results reveal a THD of 0.65%.

Fig. 10 (b) presented the currents through the L_1 and L_2 inductors, during the amplifier's operation, when reproducing a sine wave reference signal.

Fig. 13 (c) presents on the upper wave form, the output voltage V_{Cp} and on the lower wave form the reference square wave signal, obtained by simulation.

Fig. 13 (b) presented the currents through the L_1 and L_2 inductors, during the amplifier's operation, when reproducing a square wave reference signal.

To conclude the study and prove the work, the experimental results relative to the proposed amplifier, were extracted from a prototype constructed in a laboratory using the same specifications as those used for the simulation study.

In Figures 11, 12 (a) and 14(c) the obtained experimental results are presented, being that on the upper wave form, in each figure the V_{Cp} output voltage is shown and on the lower wave form the respective reference signal is presented.

Figures 12(b) and 14(d) show, on the upper wave form, the current through the inductor L_1, and on the lower wave form the current through the inductor L_2, during the operation of the proposed amplifier with the intent of reproducing the sine wave and a square wave reference signals respectively.

Figures 9, 10 and 13 obtained by simulation prove the experimental results hold true.

Table 2: Simulated/ implemented circuit parameters.

COMPONENTS	VALUES
$V_{DC1} = V_{DC2}$	100V
C_p	$220nF / 250V$
$L_1 = L_2$	$1mH / 3A$
$S_1 = S_2$	$IRF460$
D_1, D_2, D_3, D_4	$HFA15TB60$
$C_1 = C_2$	$440nF / 250V$
Load	30Ω

5 Control Strategy

A very simple control method was developed and constituted basically from a comparator with a very narrow hysteresis. As illustrated in figure 8.

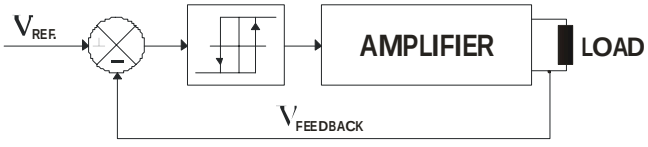

Fig.8: Control Strategy

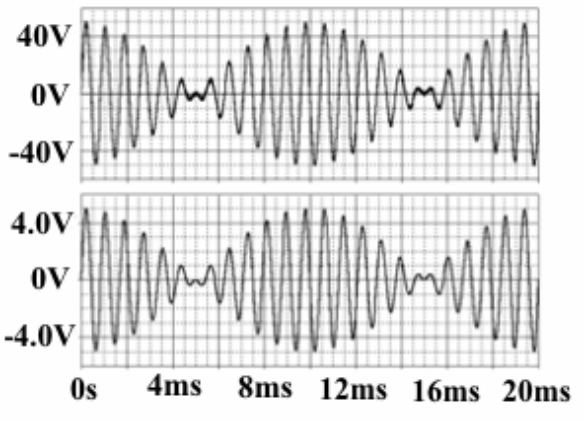

Fig.9: Simulation of AM Modulation:

- Input Signal – 50Hz sine wave
- Carrier Signal – 1.2kHz sine wave

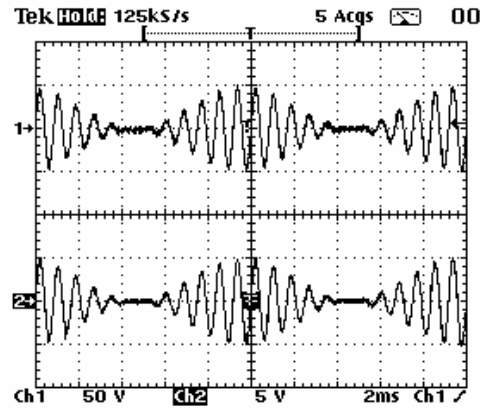

Fig.11: Experimental results of AM Modulation :

- Input Signal – 50Hz sine wave
- Carrier Signal – 1.2kHz sine wave

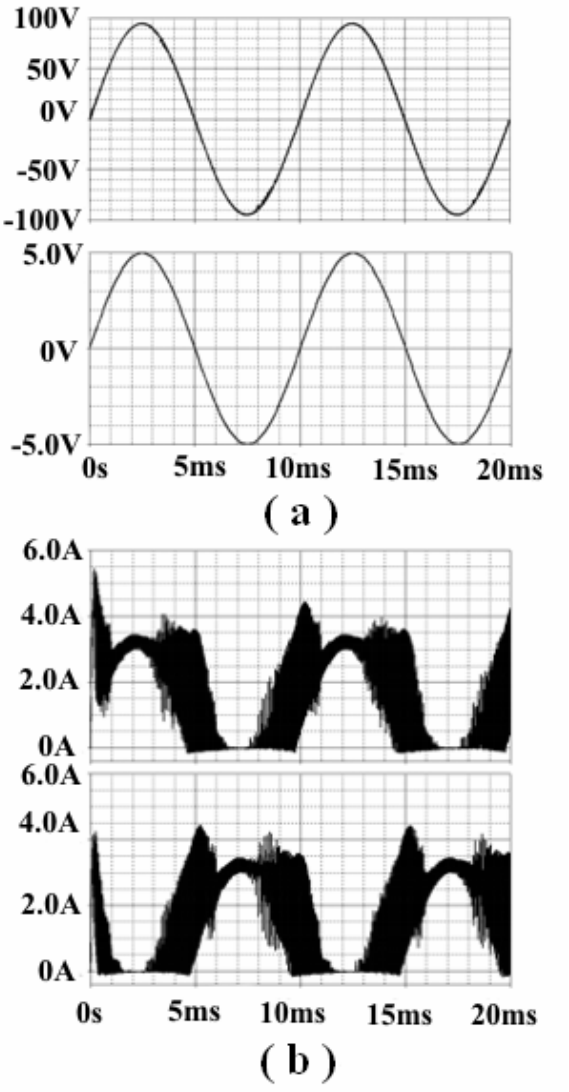

Fig.10: Simulated Wave Forms :

(a) - Upper Wave Form – Output Voltage V_{Cp} ;
(a) - Lower Wave Form – Reference Signal;
(b) - Upper Wave Form – Current Through L_1;
(b) - Lower Wave Form – Current Through L_2.

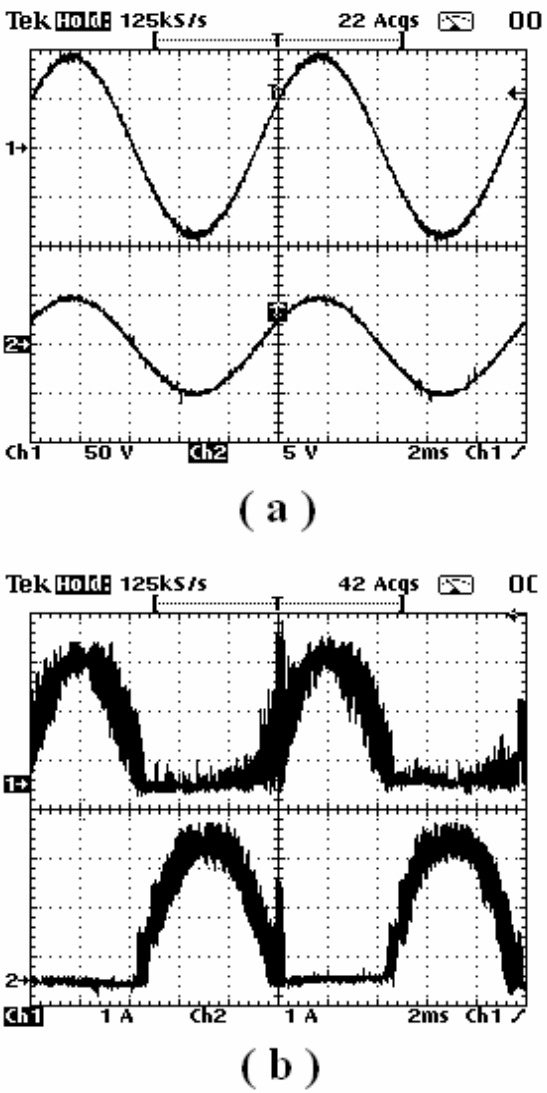

Fig.12: Experimental results of AM Modulation:

(a) - Upper Wave Form – Output Voltage V_{Cp} ;
(a) - Lower Wave Form – Reference Signal;
(b) - Upper Wave Form – Current Through L_1;
(b) - Lower Wave Form – Current Through L_2.

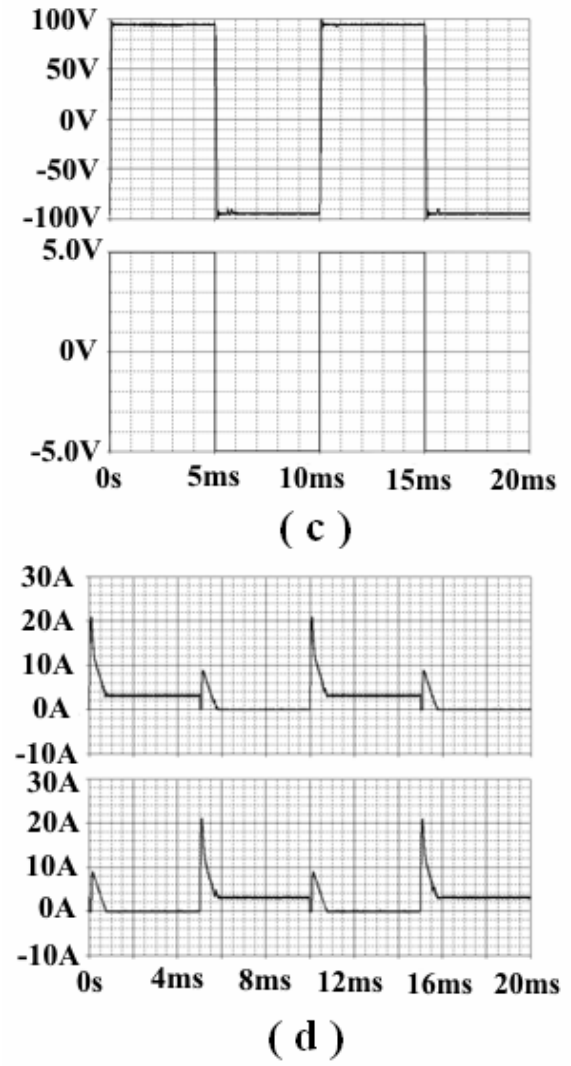

Fig.13: Simulated Wave Forms :
(a) - Upper Wave Form – Output Voltage V_{Cp} ;
(a) - Lower Wave Form – Reference Signal;
(b) - Upper Wave Form – Current Through L_1;
(b) - Lower Wave Form – Current Through L_2.

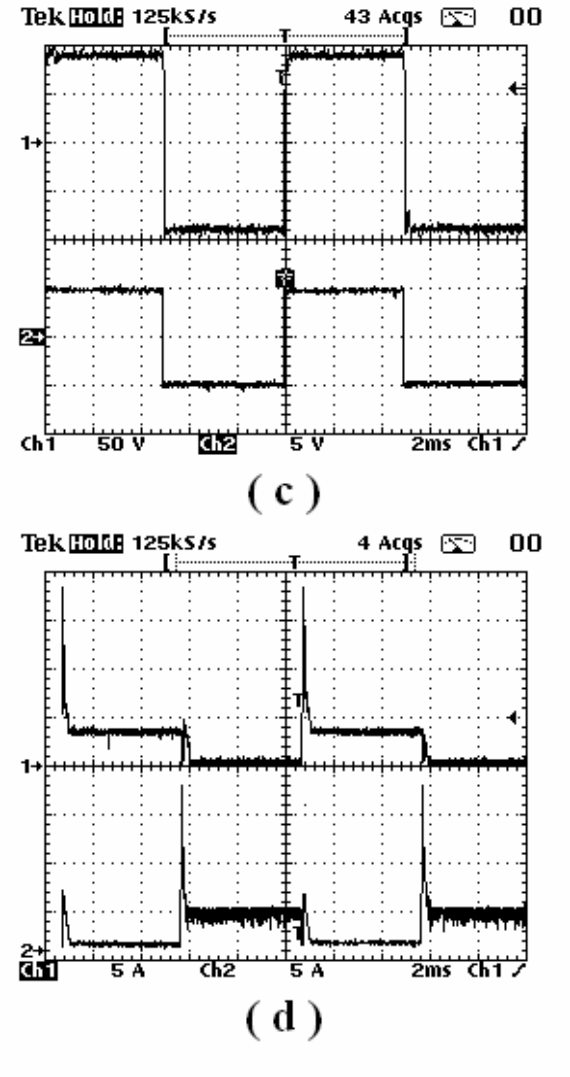

Fig.14: Simulated Wave Forms :
(a) - Upper Wave Form – Output Voltage V_{Cp} ;
(a) - Lower Wave Form – Reference Signal;
(b) - Upper Wave Form – Current Through L_1;
(b) - Lower Wave Form – Current Through L_2.

6 Conclusion

A new structure proposal for a power switching amplifier was presented in this paper

According to the experimental and simulation results, one can see that the output voltage follow the reference input signal for no load to full load range.

In order to keep a constant efficiency from no load to full load range the voltage on the voltage sources V_{cc1} and V_{cc2} must be slightly superior to the peak voltage on the load. This procedure reduces switching and conduction losses.

The proposed topology operates like a operational amplifier, but for high power applications

The proposed amplifier topology, design guide and control strategy are easy to implement.

A well designed project for the new structure proposal results in good dynamic response for high frequency reference signals without amplifying distortion and low THD.

References:

[1] FLINDERS, F. M., WOLFS, P. J. and KWONG, K. C. Improved techiniques for switched power amplifiers, IEEE Transactions on Power Electronics, 1993, Vol 8.

[2] MORAD, E. and ZIOGAS, P. D. and JOOS, G. A DC Commutated High Frequency Half Bridge Forward PWM DC-DC Converter, PESC, 1991, pp. 216-222.