CPLD- BASED ARBITRARY WAVEFORM GENERATOR

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Abstract: A very low cost PC-compatible instrument is presented. It is attached to paralell port and it can generate any arbitrary or standard (sine, square, triangular, etc.) waveform, allowing to set all of its parameters: frequency, amplitude and duty cycle. Amplitude or frequency modulation can be optionally used when sine wave is selected. It is based on DDS (*Direct Digital Synthesis*) technique and implemented on a CPLD (Complex Programmable Logic Device). By means of a text file of 32K values, one waveform cycle can be programmed. Output frequency can be setted from 0.6 Hz to 1 MHz, with maximum measured errors lower than 0.12%. Amplitude resolution is 2.44 mV. PC is only used to set waveform parameters, hence the device operates in an autonomous way. PC can be used by other applications, being one of them the acquisition of the real-time system response. There are several commercial ICs that carry out DDS technique but they only generate sine, square and triangular waveform, whereas the system propposed can also generate any arbitrary waverform in a very easy way.

Keywords: DDS – Waveform Generator – PC – CPLD.

1 Introduction

Digital signal processing methods are used in many everyday applications. Whether it is a digital audio compact disc player, an electronic synthesized piano, or a voice-synthesized telephone message system, it is obvios that complex waveforms can be easily created or reproduced using digital signal generation methods. Digital audio devices read sequentially from memory, a stream of digital data representing the sampled analog signal shape. Data are fed to a digital-analog converter (DAC) at a constant rate, producing a series of voltage steps approximating the signal shape. To obtain the original analog signal an antialiasing filter is used . DDS technology is an innovative circuit architecture that allows fast and precise manipulation of its output frequency under full digital control [1]-[2]. DDS also enables very high resolution in the incremental selection of output frequency .

Several commercial highly integrated devices that use DDS are available to form a complete digitally programmable frequency synthesizer, but they can only generate a sinewave [3]. The goal of this work is to overcame this limitation, integrating a full arbitrary wave generator on a low cost CPLD from Lattice Semiconductor® [4].

2 Theory of Operation

In a DDS system the amplitude values for one complete cycle of the output waveshape are stored sequentially in RAM. Fig. 1 shows a complete block diagram of this system. As RAM values are read, the 12 bits-DAC converts the waveshape data into a voltage waveform whose frequency is proportional to the rate at which RAM addresses are changed. DAC output is a sequence of voltage step values, so a Low Pass Filter (LPF) is needed to interpolate the original analog signal values. Because DAC is clocked at a fixed rate (F_{clock}), LPF cut frequency is constant, so its design is simplified.

The DDS method uses a phase accumulation technique to control the output frequency, so instead of using a counter to generate sequential RAM addresses, an Adder is used. On each clock cycle, the constant (M) loaded into the Phase Increment Register (PIR) is added to the actual value in the Phase Register (PR). The 15 most-significant bits of the PR output are used

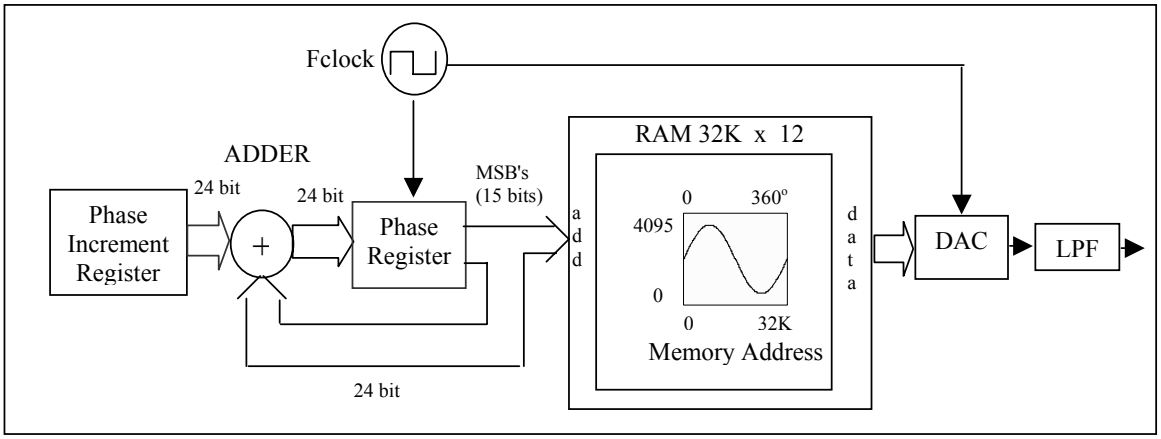

Fig.1: DDS system block diagram.

to address 32K RAM. Modifying the PIR constant, the number of clock cycles (required to step through the entire waveform RAM) is changed, hence adjusting the output frequency. To get a good frequency resolution a 24 bits adder is used, so a $F_{clock}/(2^{24} - 1)$ frequency step (F_s) is achieved.

3 Working parameters range

As mentioned above, output frequency is set as $F_{out} = F_s*M$. In this work a $F_{clock} = 10$ MHz is adopted, so $F_{min} = 0.6$ Hz for M = 1. In order to get a low distortion, at least 10 samples/cycle of output waveform are needed, so M maximum is limited to $(2^{24} - 1)/10$ and hence $F_{max} = 1$ MHz.

Amplitude samples of the waveform wanted are software generated and sent to DDS RAM trough Parallel Port. Values should match DAC dynamic range to obtain the best amplitude resolution. A ± 5V DAC is used, so amplitude resolution is $\pm 5\ V/(2^{11} - 1) = \pm 2{,}44$ mV.

DDS technique does not include modulation capability. If AM or FM modulation is needed additional circuitry must be included. The circuit implemented overcame this drawback employing a greater RAM. Although, a 12 bits-DAC requieres only a 4096 samples RAM to store a continuous wave (CW), a 32 Ks RAM is selected, allowing to store several cycles of a modulated signal, ir order to keep both carrier and modulating phase errors as low as possible. A low carrier phase error is produced when the ratio (carrier freq)/(mod freq) is an integer number. Here, a minimum ratio of 100 is adopted while maximum ratio is limited only by memory size. Taking into account that 10 samples/carrier_cycle are used and the available memory, this maximum ratio is calculated as:

$$\frac{32\,\text{Ksamples}}{10\,\text{samples/carrier-cycles}} = 3200\,\text{carrier-cycles}$$

Finally, taking one modulating cycle the frequency ratio is 3200. So, it is possible to set a range $100 < F_{carrier}/F_{mod} < 3200$, that includes most of typical applications.

For example, if $F_{carrier} = 1$ MHz (F_{max}), then F_{mod} can be selected between 312 Hz and 10 kHz. On the other side if $F_{mod} = 0.6$ Hz (F_{min}), then $F_{carrier}$ can be as low as 60 Hz.

4 Circuit Design

A block diagram of the generator developed is shown in Fig. 2. The main blocks are: Memory (32K x 12 RAM), DAC, Output Stage (Amplifier and Low Pass Filter), Clock Generator and CPLD.

The CPLD (ispLSI1032) performs most of the operations needed for phase accumulation: PR, PIR and Adder blocks. Also it carries out the Parallel Port PC communication through ADD, DATA Decoder and Mode Selector blocks. The CPLD inner connections are shown in Fig. 3. The design is made with a Lattice Semiconductor® environment that works at schematic level, allowing a faster and easier development stage.

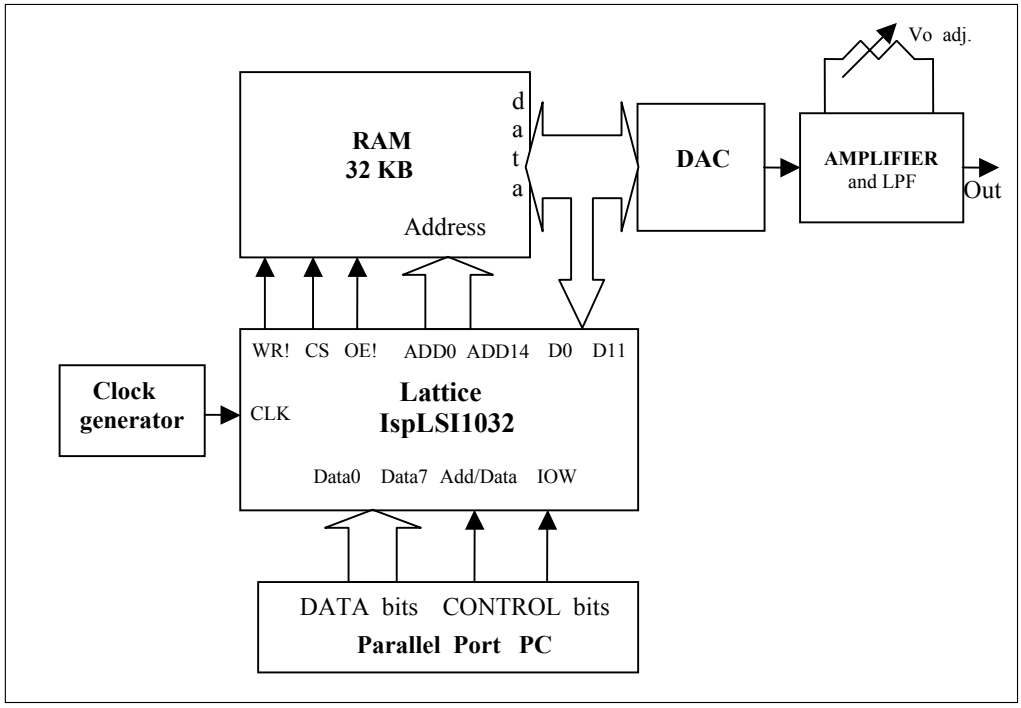

Fig. 2: Block diagram of generator developed.

PR, PIR and Adder blocks are included in ordinary DDS circuits. Decoder block drives data and address RAM buses. Mode Selector block switches data flow between two Modes: Programming (PC to RAM) and Generation (RAM to DAC).

As Fig. 2 shows, CPLD Data Bus is connected to Parallel Interface Data Lines accessed through PC-port 378h. Also, there are two control lines driven by port 37Ah: Add/Data (bit 1) used by Decoder block and IOW (bit 0). When bit 1 is set an Address is sent through Data Bus, otherwise a Data is sent. To latch the address or data values in the Registers, one writing cycle must be generated by means of bit 0.

5 Waveform programming

The PR Register capability to address RAM, is also used in Programming Mode. As mentioned above, when PR = 2^9 memory address 1 is enabled. Every time 2^9 is added to PR, memory address is incremented by 1. So, it is only necessary to set PIR Register to the appropriate value (2^9) to automatically increment memory address by one after each sample value is stored. Programming steps are:

1. Set Programming Mode.
2. Reset System.
3. Load memory address step (2^9), to PIR Register.
4. Write software generated waveform sample values to RAM until it is filled.
5. Calculate M according to desired F_{out} and load its value to PIR Register.
6. Set Generator Mode.

Hence, the circuit generates the waveform programmed by itself, allowing the use of PC by other applications.

6 Conclusions

DDS based function generators offer substantial performance improvements, at reduced costs, over conventional analog function generators. Standard DDS CIs can only generate sine waves, whereas the simple, low cost circuit proposed here can generate any kind of waveform, including amplitude and/or frequency modulation.

It is remarkable the advantages of using CPLD development tools to simplify the design and tunning of the DDS complex circuitry.

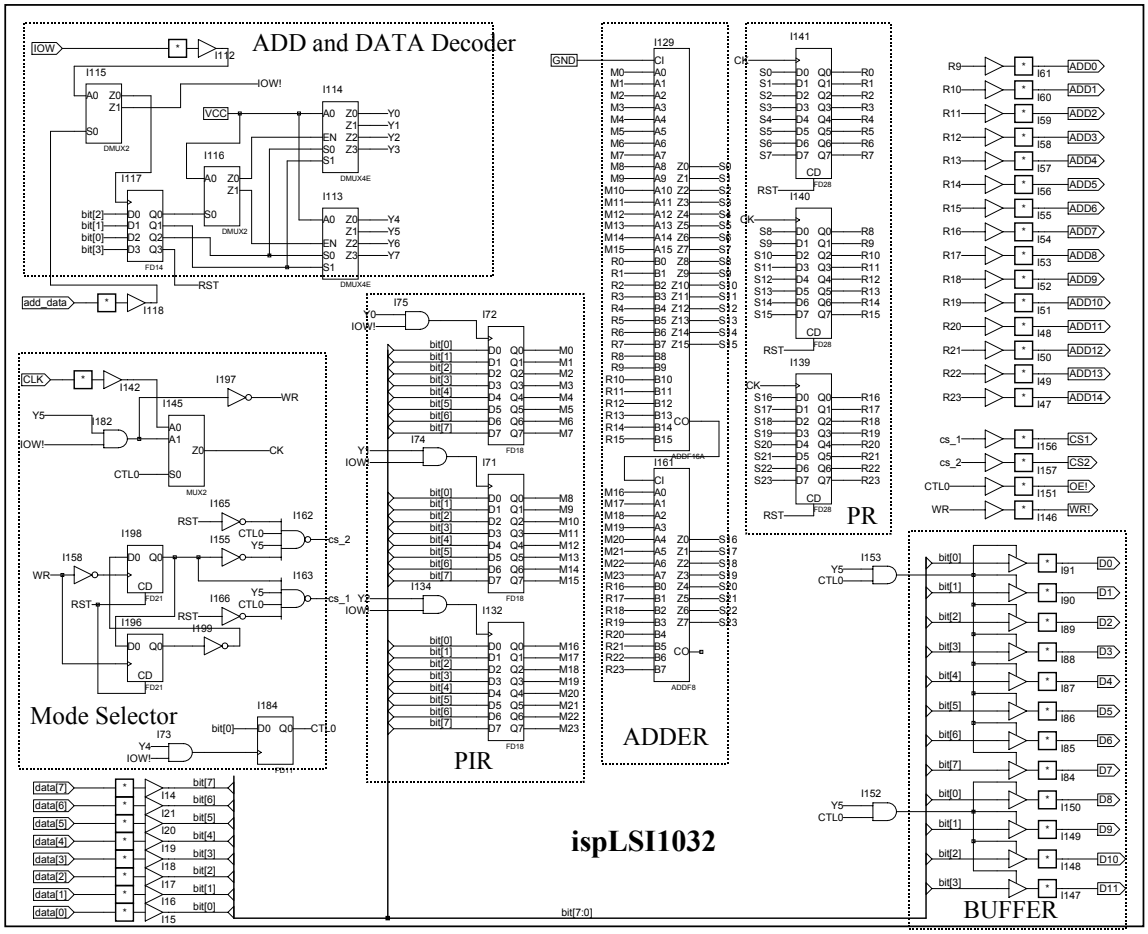

Fig. 3: CPLD inner connections.

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