Extracting of Substrate Network Resistances in RFCMOS

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Abstract:

In this paper substrate network resistances are analyzed and extracted for multi-finger MOS transistors used in RF applications. The commonly used model for MOS transistors in RF applications mainly consists of a substrate resistance network having three resistors. A typical horse-shoe CMOS transistor laid out and all substrate resistances are extracted from I-V characteristics. Device and process simulation results for 0.25μm CMOS technology show that the horse-shoe structure decreases the parasitic substrate resistance by 27%. Additionally, we show that the results obtained from traditional approximation method deviated about 31% from the exact results. Furthermore, with proposed method, the substrate resistance values can be exactly extracted.

1. Introduction

With the fast growth in wireless communication market, RF designers have begun to explore the use of CMOS devices in RF circuits. Accurate and efficient RF MOSFET models are thus required. Compared to the MOSFET modelling for both digital and analog applications at low frequencies, compact RF models are more difficult to develop and do not exist in commercial circuit simulators. A common modelling approach for RF applications is to build sub-circuits based on MOSFET models that are suitable for analog applications. The accuracy of such a model depends on how to establish a sub-circuit with the correct understanding of the device physics in high frequency operation, and how to extract parameters appropriately for the elements of the sub-circuit [4].

A fundamental knowledge of all parameters of the models used for circuit simulations is one of the major prerequisites for a successful design. This is particularly true for the design of analog RF circuits. An efficient and accurate method to directly extract the parameters needed for accurate modelling of transistors in a standard CMOS sub-micron technology for RF applications is presented in [7]. However, the direct parameter extraction results in complicated models which increases the simulation time. The possibility of modelling a CMOS device at high frequencies by utilizing a complicated substrate network and modification of the BSIM3v3 source code has been discussed in [5]. The main part of the sub-circuit model is the substrate network resistance. In this paper, we present a method of extraction of substrate network resistances.

In section 2, modelling of MOS transistors for RF applications is presented, and sub-circuit modelling is introduced. Multi-finger structures of RF transistors are discussed in section 3, also several typical structures are explained. Section 4 deals with the simulation results. Finally, conclusions are drawn in section 5.

2. MOS TRANSISTOR MODELLING FOR RF APPLICATIONS

Sub-circuit based models, as illustrated in Fig. 1, are the most popular in RF MOS modelling [1]. The source and drain series resistors, which have been calculated in [2] may be added outside the MOS model. Although the gate resistance is not part of the MOS compact model [6], it plays a significant role in RF circuits. Moreover, it consists of two types of resistances as discussed in [2]. The substrate resistors R_{dsb}, R_{db} and R_{ds} model the signal coupling through the substrate. This effect will be discussed in detail in this paper.

The source-to-bulk and drain-to-bulk diodes are also a part of the compact model, though their anodes are connected to the same substrate node. In the compact model the anodes of D_{sb} and D_{db} are connected together, so they are turned off. As such, two external diodes are added in order to account for the substrate resistance existing between the source and the drain diffusions.

The sub-circuit model of Fig. 1 (b) includes two bias-dependent overlap capacitances C_{gs0} and C_{gd0}. However, in some compact models this is not required, for example, BSIM3v3 itself accounts for bias-dependent overlap capacitances. If these capacitances, are extracted correctly, the sub-circuit model finds sufficient accuracy. Pulling C_{gs0} and C_{gd0} out of the compact model also allows for correction in some inaccuracies such as intrinsic capacitances appearing in short-channel devices. The circuit model in Fig. 1 (b) can then easily be implemented in Spice as a sub-circuit.

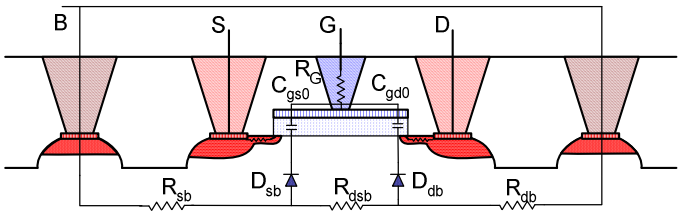

Fig. 1 (a). Cross-section of the RF MOS transistor

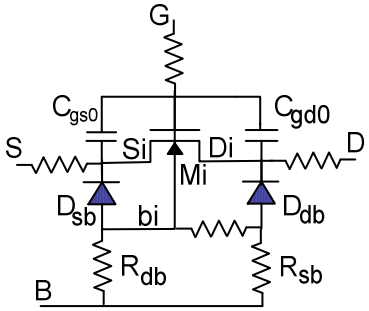

Fig. 1 (b). Schematic of the RF MOS transistor model

3. MULTI-FINGER STRUCTURE FOR RF MOS TRANSISTORS

RF MOS transistors are usually designed as large devices in order to achieve a desired transconductance required to make the transistor operate up to RF. As shown in Fig. 1, they are usually laid out as multi-finger devices, because in deep-sub-micrometer CMOS processes the maximum finger length is limited. As the finger width decreases polyside sheet resistance increases due to grain boundary problems. This is the so called "narrow line effect". Typical devices have more than 10 fingers. The total transistor effective width W_{eff} is then simply $N_f W_f$.

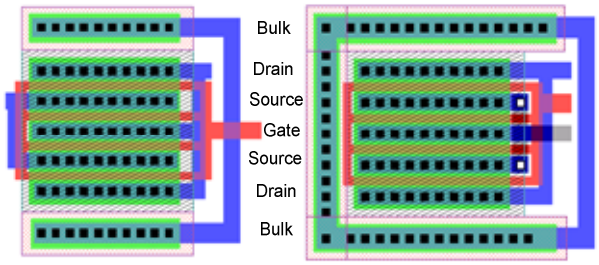

Fig. 2 (a). Multi-finger structure of an RF MOS transistor

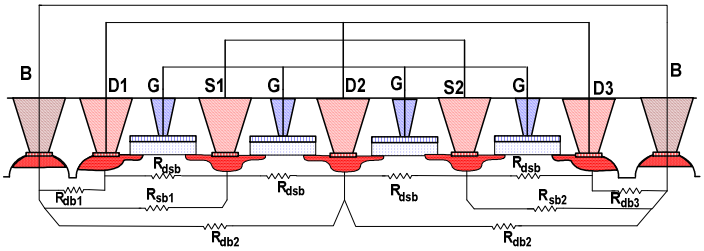

Fig. 2 (b). Cross-section of the multi-finger transistor

Multi-finger transistors may be laid out in different ways as shown in Fig. 2(a). Bulk contacts in Multi-finger transistors are usually laid out on both sides of the transistor. Methods for approximate calculation of substrate resistance are given In [1] and [3]. Obviously, the values of the substrate resistors have a substantial effect on the accuracy of the model. Also accuracy of these methods [1],[3] for extracting substrate resistances decreases for the horse shoe structures. The cross-section of a multi-finger transistor is shown in Fig. 2 (b). Total R_{ds} and R_{db} are made by shunting of all R_{sb1}, R_{sb2} and R_{db1}, R_{db2}, R_{db3}. In [1] R_{ds} and R_{db} are calculated considering only the first and the nearest finger and the rest of fingers are neglected. In the next section we examine the accuracy of this method.

4. SIMULATION RESULTS

Because of the minimum channel length and the minimum distance between the bulk and drain (source) contacts, the layouts in Fig. 2 (a) are optimum for substrate network resistances; they have also been checked by design rules. These layouts with the same geometry are given to a device simulator [8]. The related vertical cross-section and the mesh grid are shown in Fig. 3. The mesh grid is fine in regions where potential changes rapidly, while it is coarse in the other regions.

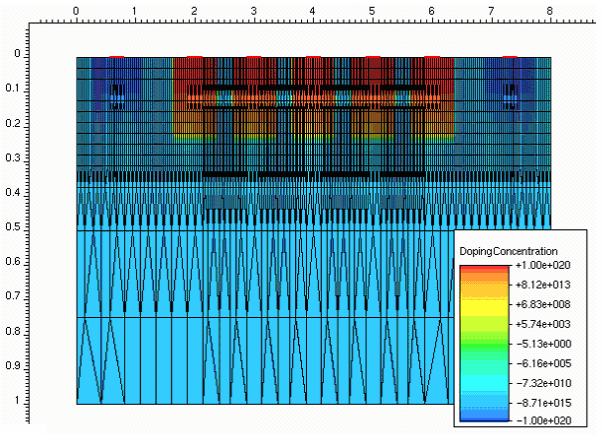

Fig. 3. Mesh gird of transistor cross-section in Mdraw

Resulted I-V characteristics have been used for extracting each finger resistance. In this simulation, resistance values between the bulk and the source (drain) contacts are extracted by sweeping bulk-source (drain) voltage. In order to extract the resistance value between each finger and the bulk, first, the current flow of only drain 1 was taken into account and then the rest of the fingers were added one by one. Fig. 4 shows the I-V characteristics for these fingers.

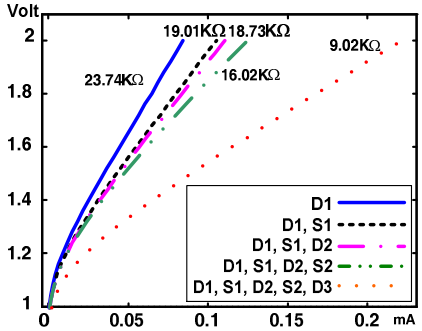

Fig. 4. I-V characteristics of fingers in the multi finger transistor in the vertical cross-section

Resistance values in Fig. 5 are calculated from the extracted I-V characteristics in Fig. 4. Also, 4th finger resistance can be predicted to be around 1MΩ/□.

As mentioned in [1] for horse shoe layout structures, the extra bulk contact branch in the left side of the transistor decreases the substrate network resistance. To obtain resistance values in this case all simulations were run both with horizontal and vertical cross-sections of multi-finger transistors. Vertical cross-section simulation results are shown in Fig. 4 and Fig. 5. Also Fig. 6 and Fig. 7 show horizontal cross-section simulation results. In the horizontal cross-section simulation, dc voltage was swept for each contact. As shown in Fig. 6, after the 4th contact is accounted for, the resistance is negligibly affected so that it reaches to a constant value.

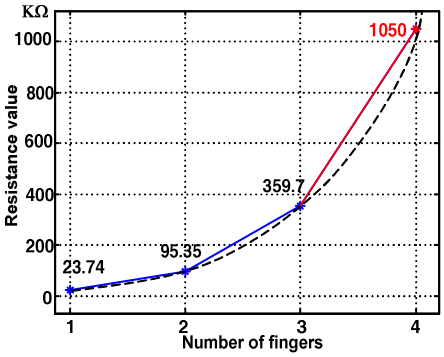

Fig. 5. Resistance values as a function of number of finger

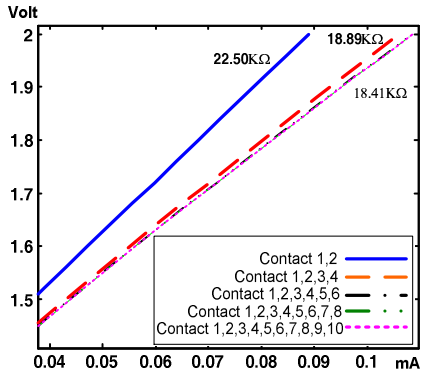

Fig. 6. I-V characteristics of fingers in multi finger transistor in horizontal cross-section

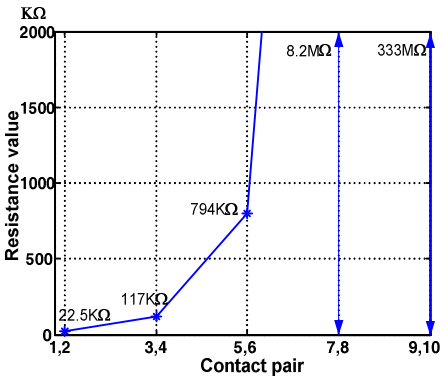

Fig. 7. Resistance values of each contact pair

Values of resistance per unit length for all fingers of Fig. 2 (a) are simulated and summarized in Table. 1. Underlined values in Table. 1 are extrapolated from the simulation results. The total vertical resistance per unit length for the horse-shoe layout structure with more than 5 fingers is about 8.6KΩ.

Finger No.	Resistance per unit of Finger 5	Resistance per unit of Finger 7	Resistance per unit of Finger 9
1	23KΩ	23KΩ	23KΩ
2	95 KΩ	95 KΩ	95 KΩ
3	359 KΩ	359 KΩ	359 KΩ
4	143 KΩ	1 MΩ	1MΩ
5	20 KΩ	359 KΩ	10M Ω
6	-	143 KΩ	1 MΩ
7	-	20 KΩ	359 KΩ
8	-	_	143 KΩ
9	-	_	20 KΩ
Total	9 KΩ	8.7 KΩ	8.6 KΩ

Table. 1. Resistance per unit length for each finger in vertical cross-section

Contact Number	Resistance per unit
1,2	22.5KΩ
3,4	117KΩ
5,6	794KΩ
7,8	8.2MΩ
9,10	333MΩ
Total	18.4KΩ

Table. 2. Resistance per unit length for each contact pair in the horizontal cross-section

Table. 2 contains the horizontal resistance per unit length of all contact pairs for any finger of horseshoe layout structure. Thus, using these two tables, the substrate resistance network for each arbitrary horseshoe RF transistor could be precisely extracted. For example extraction method for resistances of substrate networks with 9-finger and 10-finger RF transistors are illustrated below. Dimensions and geometry for a 9-finger and 10-finer RF transistors are shown in Fig. 8. Vertical resistance values are calculated from equations (1),(2) and agree closely for 9-finger and 10-finger transistors. Horizontal resistance values are calculated from equations (3),(4) for the 9-finger and (5),(6) for the 10-finger transistor. In transistors with odd number of fingers, R_{sb} and R_{db} exhibit large difference in resistance values.

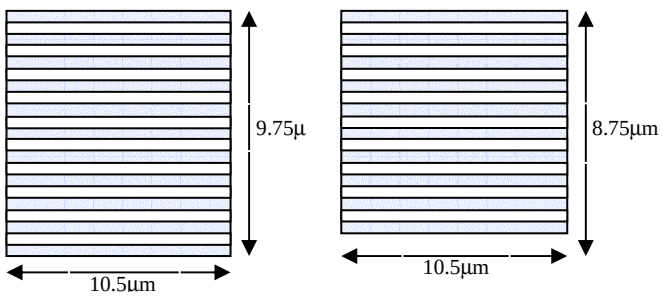

Fig. 8. Dimensions of 9 and 10 finger RF transistor

$$R_{db}(ver) = R_{db}(ver.\ per\text{-}unit) / 10.5um \quad (1)$$
$$R_{sb}(ver) = R_{sb}(ver.\ per\text{-}unit) / 10.5um \quad (2)$$

$$R_{db}(Hor) = R_{db}(Hor.\ per\text{-}unit) / (8.75um \times (4/10)) \quad (3)$$
$$R_{sb}(Hor) = R_{sb}(Hor.\ per\text{-}unit) / (8.75um \times (6/10)) \quad (4)$$

$$R_{db}(Hor) = R_{db}(Hor.\ per\text{-}unit) / (9.75um \times (5/10)) \quad (5)$$
$$R_{sb}(Hor) = R_{sb}(Hor.\ per\text{-}unit) / (9.75um \times (5/10)) \quad (6)$$

Resistance values are listed in Table. 3. It is obvious that vertical drain and source resistances for 10-finger transistors are almost equal, but for 9-finger, they show a large difference. Also, horizontal drain and source resistances are different for 9 and 10-finger transistors, but with increasing the number of fingers, this difference between horizontal drain and source resistances values decrease.

	9-finger		**10-finger**	
	Vertical	**Horizontal**	**Vertical**	**Horizontal**
R_{db}	**0.85 KΩ**	**5.1 KΩ**	**1.7 KΩ**	**3.7 KΩ**
R_{sb}	**4.84 KΩ**	**3.5 KΩ**	**1.5 KΩ**	**3.7 KΩ**

Table. 3. Total vertical and horizontal resistance value for 9 and 10-finger transistor

10-finger	**R_{sb}**	**R_{db}**	**comment**
Calculation in [1]	**2.2KΩ**	**2.2KΩ**	**Resistances reported 31% higher than simulation result**
Simulation result for Fig. 2 without third branch of bulk contacts	**1.51KΩ**	**1.7KΩ**	-
Simulation result for horseshoe	**1.16KΩ**	**1.16KΩ**	**27% improvement in simulation result**

Table. 4. Final resistance values

5. CONCLUSION

In this work, we have extracted the substrate resistances using a device simulator [8]. These simulation results have shown that the presence of third branch of the bulk contacts in one side of a transistor in addition to the top and bottom bulk contact rows of the transistor layout, decreases substrate parasitic resistance by 27%. Also, it has been demonstrated that preceding approximation method [1],[3] evaluate parasitic resistance 31% higher than simulation results.

6. ACKNOWLEDGMENT

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7. REFERENCES

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