A CAD application for optimising the bandwidth in the structured design of negative-feedback amplifiers by using the open-loop gain-poles product

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Abstract – Structured design of analogue electronics has been devised as an alternative methodology of design that resorts to basic concepts of circuit theory and general electronics in order to achieve a hierarchy-driven design process. On the contrary to traditional methods of design, where a previously designed circuit is used as initial guess in the design procedure, structured design has as starting point an ideal solution. Such a solution does not exist, therefore the final (and feasible) solution must be obtained through a method that uses hierarchy on its full extent. This paper introduces a MAPLE-based application which is aimed to optimise the bandwidth of negative-feedback amplifiers by resorting to the open-loop gain poles-product. The symbolic evaluation of the involved transfer functions results in more insight in the design procedure.

Key-Words: – Design-automation, Analogue design, Symbolic Analysis Applications

1 Introduction

The design of analogue electronic circuits has often been classified as an art under the background that no systematic procedures or methodologies have been developed. Usually, analogue designers resort to their own experience by applying a series of thumb rules in order to generate the circuit that meets the specifications. The experience is recast in an encyclopedic knowledge that can be consulted when the designer faces the challenge of a new design. In order to obtain the new design, modifications are achieved on an already existing circuit oriented to fulfill some specific features. Unfortunately, this scheme results very cryptic and difficult to handle for students.

Analogue structured design starts from an ideal solution, which can be easily understood by students because it resorts to basic concepts of circuit theory and electronics.

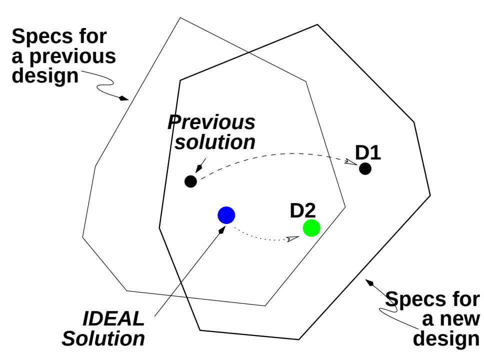

Figure 1: Structured design vs traditional design

However, the ideal solution does exist only on the paper, but it is not feasible. The final solution is accomplished by incorporating modifications to the ideal solution until the specs are fulfilled.

Figure 1 depicts these concepts. The traditional designs starts from a solution that fulfilled a previous set of specifications and ends up with the design **D1**, while structured designs starts from an ideal solution — which obviously fulfills both sets of specifications — and generates the design **D2**.

Among others, the structured design is oriented to optimise aspects such as noise, distortion and bandwidth (BW) [1, 2]. This paper is devoted to the aspects of bandwidth optimisation within the scope of the structured design methodology applied to the design of negative-feedback amplifiers.

2 The ideal solution: the nullor

For the design of amplifier circuits, the structured design methodology resorts to the concept of nullor in order to achieve the ideal solution. The nullor is a two-port singular electric component. The input port is a nullator, and the output port is a norator, as given in the figure 2.

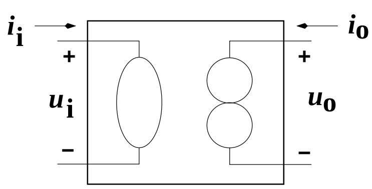

Figure 2: The nullor

At the input, the nullator has a branch relationship that zeroes in on both voltage and current at the origin, i.e.:

$$i_i = 0 \qquad u_i = 0$$

At the output, the norator has a branch relationship that allows both variables, voltage and current, to take any value, i.e.:

$$i_o = \times \qquad u_o = \times$$

Therefore, the output variables of the nullor are defined by the environment.

One interesting property of the nullor that becomes particularly useful in the design of amplifiers is that its $\boldsymbol{K}$ matrix has the form:

$$\boldsymbol{K} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \qquad (1)$$

which results in the next definitions of transfer functions:

$$\begin{aligned} \mu &= \tfrac{1}{A} = \tfrac{u_i}{u_o}\Big|_{i_o=0} = \infty \\ \gamma &= \tfrac{1}{B} = \tfrac{u_i}{i_o}\Big|_{u_o=0} = \infty \\ \zeta &= \tfrac{1}{C} = \tfrac{i_i}{u_o}\Big|_{i_o=0} = \infty \\ \beta_F &= \tfrac{1}{D} = \tfrac{i_i}{i_o}\Big|_{u_o=0} = \infty \end{aligned} \qquad (2)$$

i.e. the nullor represents all kinds of amplifying transfer functions having high-gain, noiseless and frequency-independent behaviour.

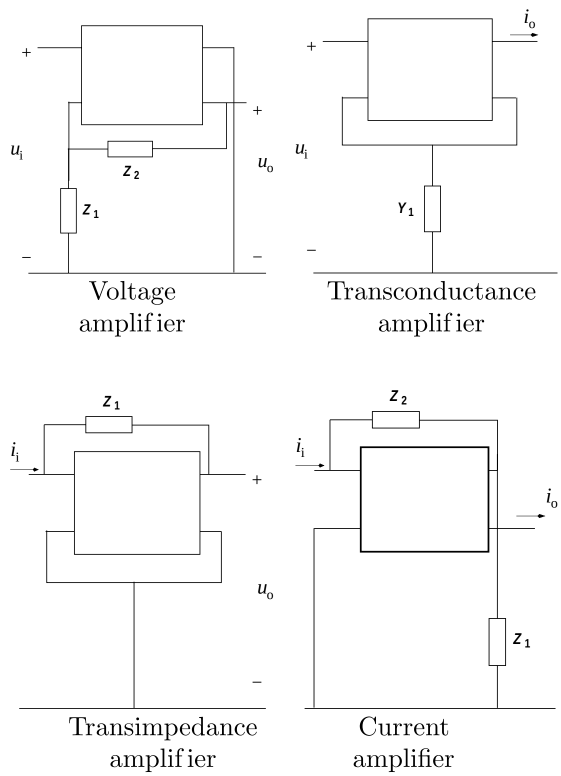

Figure 3: Basic nullor-based amplifier topologies

As a result, the structured design of amplifiers consists in a step-by-step modification of the nullor until this is fully implemented with real devices, such as transistors.

3 Structured design

Basic finite-gain topologies are generated by combining the nullor and passive components [1, 3] as shown in the figure 3. The corresponding $\boldsymbol{K}$ matrices for these topologies are given by:

$$
\boldsymbol{K}_{A_V} = \begin{bmatrix} A_V & 0 \\ 0 & 0 \end{bmatrix} \quad \boldsymbol{K}_{A_G} = \begin{bmatrix} 0 & A_G \\ 0 & 0 \end{bmatrix}
$$
$$
\boldsymbol{K}_{A_R} = \begin{bmatrix} 0 & 0 \\ A_R & 0 \end{bmatrix} \quad \boldsymbol{K}_{A_I} = \begin{bmatrix} 0 & 0 \\ 0 & A_I \end{bmatrix} \tag{3}
$$

where the ideal gains are defined as:

$$
A_V = 1 + \frac{Z_1}{Z_2} \qquad A_G = -Y_1
$$
$$
A_R = -Z_1 \qquad A_I = 1 + \frac{Z_1}{Z_2} \tag{4}
$$

Expressions in equation 3 denote in fact ideal transfer functions.

Under the schemes above, a negative feedback amplifier can be seen as the connection of two blocks, one is considered as the plant to be controlled and a second one constitutes the feedback system. The plant is in fact the nullor, which should be implemented by high-gain, active devices, such as transistors. The feedback system is constituted by the passive networks formed by the resistors. This description yields the *asymptotic-gain model* of negative-feedback amplifiers [4, 3], which is depicted in Figure 4.

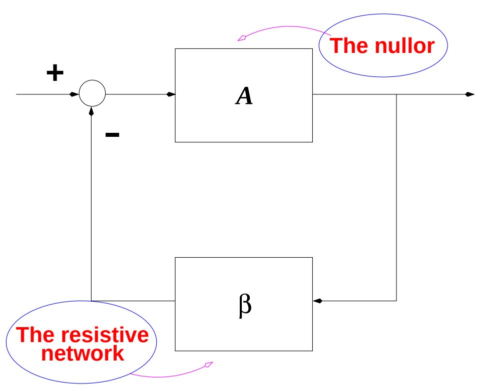

Figure 4: Asymptotic gain model

Because the first stage of the amplifier drives the largest levels of noise, the first stage of the nullor implementation is designed for an optimal noise behaviour. Because the output stage of the amplifier drives the largest swing of signal, the last stage of the nullor is designed for a minimum level of distortion — due to clipping. Finally, the middle stage of the nullor is designed to achieve the bandwidth optimisation. This procedure is schematically shown in the figure 5, where the BJT symbols denote in fact the small-signal model of the bipolar transistors.

After this is completed, the design of the amplifier can be considered done at signal-level, and the bias circuitry has still to be implemented.

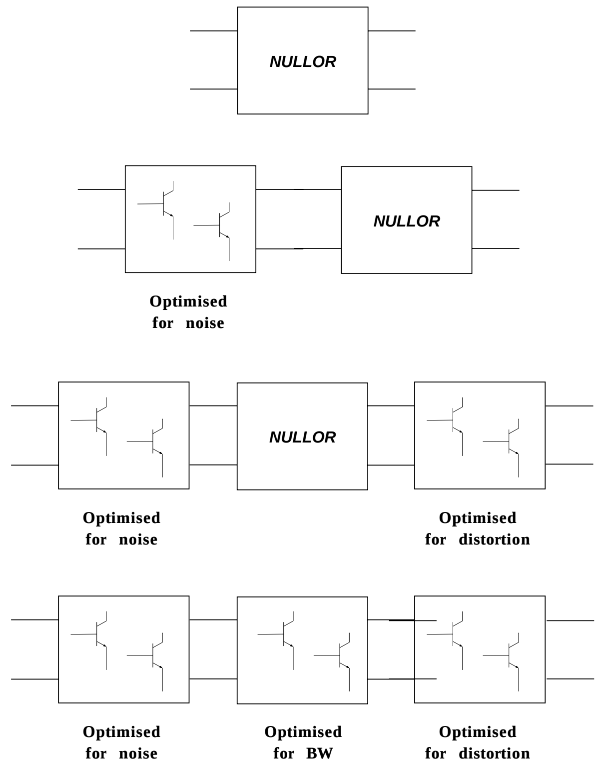

Figure 5: Synthesis procedure of the nullor

The synthesis procedure leads to the fact that the ideality of the nullor has been steadily and systematically replaced by the feasibility of the devices — BJTs in figure 5, which means that the gain expressions given in equation 3 are not valid any longer. Instead, the resulting transmission matrices can be expressed as:

$$
\boldsymbol{K}_{A_V} = \begin{bmatrix} A'_V & \delta_B \\ \delta_C & \delta_D \end{bmatrix} \quad \boldsymbol{K}_{A_G} = \begin{bmatrix} \delta_A & A'_G \\ \delta_C & \delta_D \end{bmatrix}
$$
$$
\boldsymbol{K}_{A_R} = \begin{bmatrix} \delta_A & \delta_B \\ A'_R & \delta_D \end{bmatrix} \quad \boldsymbol{K}_{A_I} = \begin{bmatrix} \delta_A & \delta_B \\ \delta_C & A'_I \end{bmatrix} \tag{5}
$$

where the ideal gains have been replaced by new expressions (denoted with 's), and non-zero entries appear now in the transmission matrices.

4 Bandwidth considerations

The nullor synthesis is carried out in the next order: (i) the stage (input stage) for noise, (ii) the stage (output stage) for distortion, and (iii) the stage (middle stage) for bandwidth. It clearly results that the design for BW considerations counts on two previously designed parts of the whole amplifier.

The transfer function of the amplifier is given as:

$$A_t(s) = A_{t\infty}\frac{-A(s)\beta}{1 - A(s)\beta} \tag{6}$$

where $A_{t\infty}$ is the asymptotic loop gain.

The open-loop gain is the product $A(s)\beta$, which determines the maximal attainable bandwidth [2]:

$$f_{n_{max}} = \sqrt[n]{LP_n} = \sqrt[n]{\left|[1 - A\beta(0)]\prod_{i=1}^{n} p_i\right|} \tag{7}$$

However, this frequency may not fulfill the BW specification which causes to design the middle stage by following the steps recast in Figure 6.

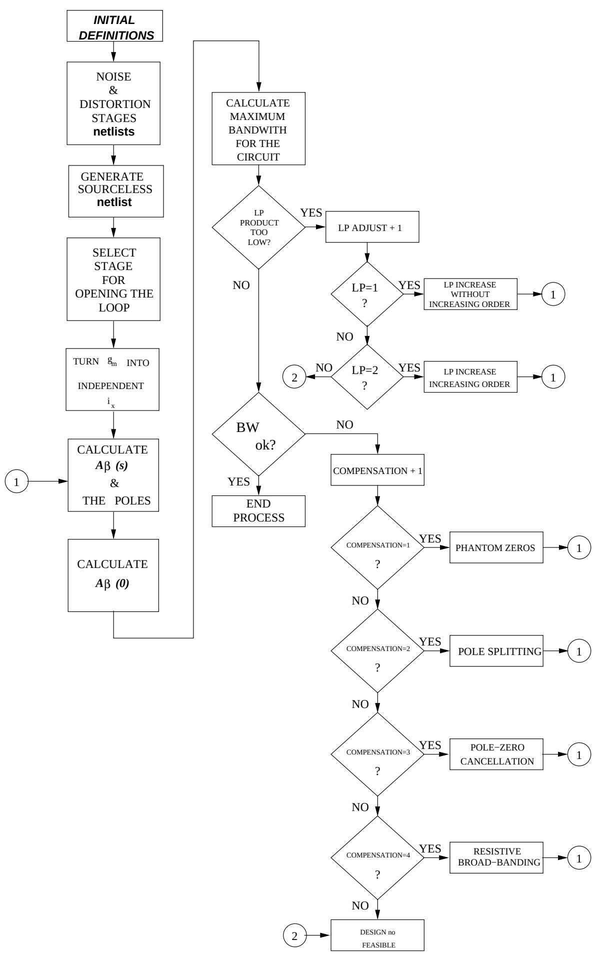

Figure 6: Flow-diagram for optimum BW design

Because the designer/student needs to get more *insight* on the procedure described in Figure 6, we have resorted to use symbolic analysis techniques [5, 6, 7] in order to determine the expression of the open-loop gain-poles product.

This can be achieved by using a traditional MNA formulation, which has been easily tailored for this specific problem. Currently, a MAPLE-package has been developed. It uses a SPICE-like grammar to define the netlist as the nullor synthesis progresses, which allows the user to carry out SPICE simulations on the final design. Completely analytic expressions for the involved transfer functions are used to determine which are the key-parameters for achieving an optimum BW. In addition, the GUI facilities of MAPLE are used to display the Bode plots.

The main features of the package can be recast as follows:

- An input syntax à la SPICE is used.
- Closed expressions are obtained.
- Several complexity levels for the transistor models are available. Besides, the user is able to add their own models in a very simple way.
- Semi-symbolic calculations are also included.
- Bode plots are also generated.

5 Example

The synthesis of the nullor in the design of a transimpedance amplifier is used to illustrate the use of the open-loop gain-poles product in order to obtain an optimum bandwidth. The first scheme is the starting configuration shown in the figure 7. The amplifier has a capacitive source and a resistive load.

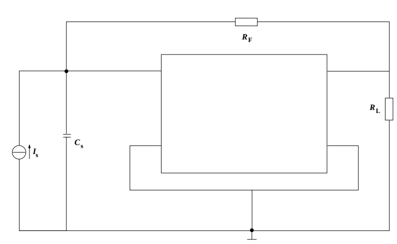

Figure 7: A transimpedance amplifier

The resulting transmission matrix is associated to the ideal solution, i.e.:

$$\boldsymbol{K} = \begin{bmatrix} 0 & 0 \\ -R_F & 0 \end{bmatrix}$$

The second scheme results from the synthesis of the input stage of the nullor by a common-emitter stage, as shown in the figure 8.

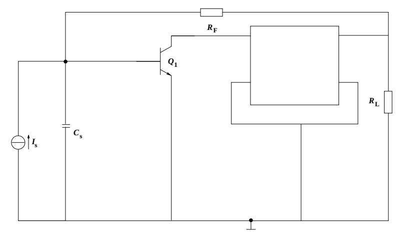

Figure 8: Synthesis of the input stage

The synthesis of the output stage of the nullor is accomplished by a differential stage, which yields the circuit given in the figure 9.

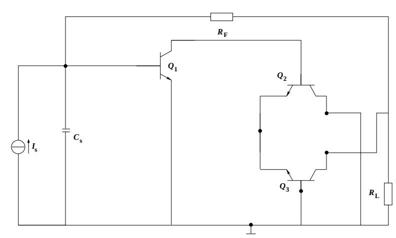

Figure 9: Synthesis of the output stage

At this point, the BW optimisation is achieved by following the procedure depicted in Figure 6. The small-signal model to be used is shown in figure 10, which includes the capacitance C_π. However, the tool is able to use more complex models, by simply calling them from a built-in library.

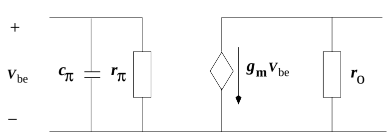

Figure 10: Model used for the BJT.

The symbolic expression for the open-loop gain is given by:

$$A\beta(s) = \frac{-R_L g_{m_1}\, g_{m_2}\, r_{\pi_2}\, r_{\pi_1}}{(1 + s\, C_{\pi_2}\, r_{\pi_2})(R_L + r_{\pi_1} + R_F + sR_L\, C_{\pi_1}\, r_{\pi_1} + sR_L\, Cs\, r_{\pi_1} + s\, C_{\pi_1}\, R_F\, r_{\pi_1} + s\, Cs\, R_F\, r_{\pi_1})} \tag{8}$$

The open-loop gain (at dc) and the poles are given as:

$$A\beta(0) = \frac{\beta_1 \beta_2 R_L}{R_L + r_{\pi_1} + R_F} \tag{9}$$

$$p_1 = \frac{-1}{r_{\pi_2} c_{\pi_2}} \tag{10}$$

$$p_2 = \frac{-(r_{\pi_1} + R_L + R_F)}{r_{\pi_1}(R_L + R_F)(C_s + C_{\pi_1})} \tag{11}$$

The figure 11 shows the magnitude in dB of the closed-loop gain of the amplifier. The designed gain is 40 dB at dc.

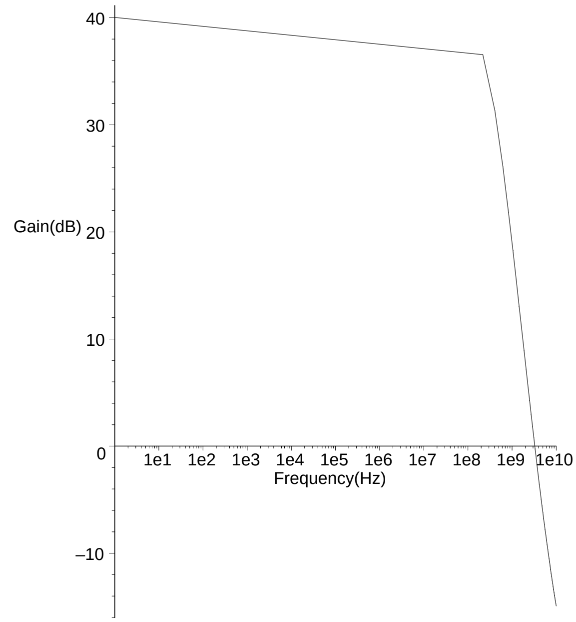

Figure 11: Bode plot of the closed-loop gain.

6 Conclusions

A symbolic-oriented method for the calculation of an analytic expression of the LP product has been presented. This method can be easily incorporated to a design automation environment for high-performance negative-feedback amplifiers. The calculation of the open-loop gain as well as the LP product and the sensitivity functions are built-in a MAPLE-based circuit simulation program that is SPICE compatible.

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