Low Voltage Analog Fuzzy Logic Controller with Continuous Time Programmability

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Abstract: - Nowadays, Fuzzy Logic Systems (FLS) have been used extensively in many applications, mainly in control applications. Adaptive control systems are those that achieve a better performance compared with classic controllers. Due to this, an analogue fuzzy controller has been designed and presented. It presents a great programmability, being able to program up to 5 parameters for the membership functions. The inference is Sugeno type, being able to control the values for each singleton. The programming is carried out in continuous time. Since some systems operate in voltage mode, a novel voltage to current converter and a current to voltage converter are presented. A fuzzy logic controller with 25 rules, 2 inputs and 1 output was designed and simulated using a standard CMOS AMS-0.8µ technology.

Key-Words: - Fuzzy, Continuous Time, Analog, Programmability, Low Voltage

1 Introduction

In the last years the application of Fuzzy Logic has been extended beyond Classical Process Control. A Fuzzy Logic Controller (FLC) can be implemented with different techniques: analogue or digital, in current mode or voltage mode, continuous time or discrete time. Digital implementations can provide a great programmability but the speed can be limited for an acceptable power consumption level, if compared with their analogue counterparts. In this work, a continuous time programmable analogue FLC for embedded systems is presented. All the presented blocks are totally analogue, achieving a continuous time programming. In these implementations is common the use of analog to digital converters (ADC's) to perform the programming of the chip [1]. So, if it's required to implement an adaptive system completely analog it should be thought of the way of programming these analog blocks without converters. It has been shown that analogue current mode FLCs lend themselves to simple rules evaluations and aggregation circuits that can work at a reasonable speed [2]. Often membership, fuzzifiers and defuzzifiers circuits are being designed for these circuits interact normally with signals in voltage mode [2, 3, 4, 5]. For these reasons the FLC was designed in current mode to perform all the process of inference. To process signals in voltage mode at the inputs and outputs of the FLC, a transconductor amplifier and a transresistor amplifier were designed. Because most of the cells are based on current mirrors, the controller's design is very simple.

2 Fuzzy Logic Controller

Because it offers a good trade-off between simplicity and accuracy, a zero-order Sugeno architecture (consequents and singletons) was chosen. Figure 1 shows the block diagram of a two-inputs, one-output, 25-rules for the controller designed.

2.1 Programmable Membership Function Circuit

Based on the block diagram shown in Figure 2 (where Nx and Px are N or P type current mirrors respectively), a Programmable Membership Function Circuit (PMFC) was proposed. In this circuit I_{ref}, I_1 and I_2 can be easily programmed. The problem arises when the slopes *m1* and *m2* must be modified. Since the slope depends on the gain of the current mirror, a programmable gain current mirror (PGCM) must be implemented. For this fact, can be used the circuits proposed in [6] instead of ADC's [1]. Figure 3 shows the PGCM used.

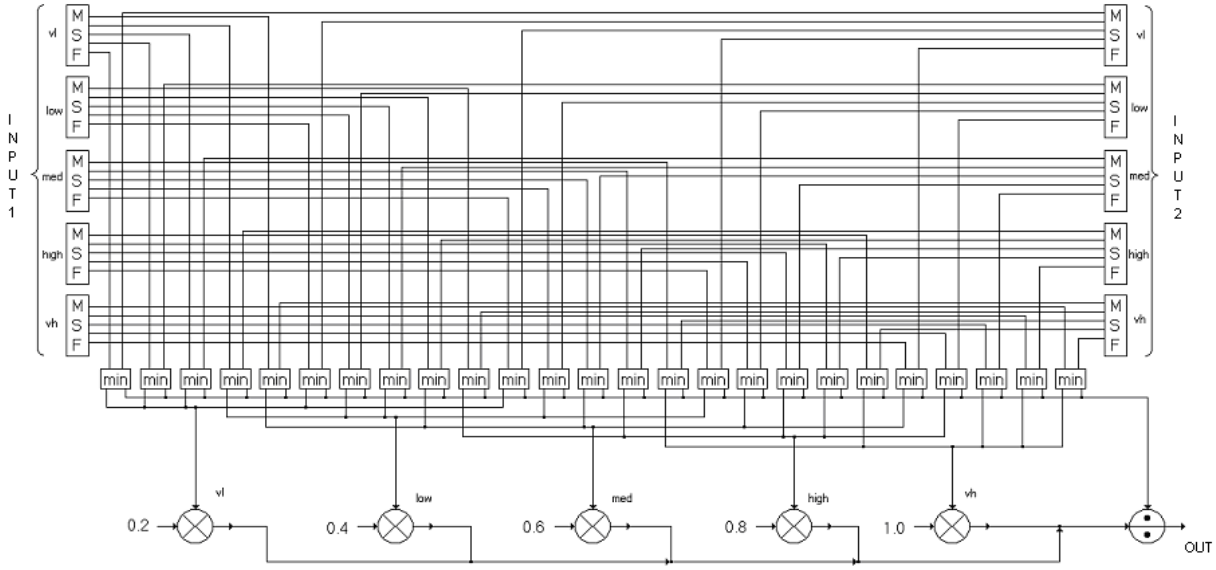

Fig. 1 Block Diagram of the simulated System.

The parameter that can be controlled is I_c. Depending on the differential pair's polarization, the current mirror will have a linear or no-linear gain. If it's operated in strong inversion a non-linear variation of the gain is obtained. If it's operated in weak inversion a linear variation of the gain is obtained. Figure 4 shows the resulting PMFC. Sometimes exist the need to work with signal in voltage mode. Since the signals are processed in current mode, a linear transconductor based on the floating gate technique [7] was proposed. Figure 5 shows the circuit of the proposed transconductor. The basic idea is to work the transistors *M3* in the triode region. It can be done if the adequate weight to the capacitor for V_b is give it to set a gate voltage of $V_{th}+V_{dsat}$, and set $V_{dsat3}<V_{dsat}$. *M2* must be sized large enough to force $V_{dsat3}<V_{dsat}$. The following equations were derived from the analysis of the circuit:

$$V_g = \frac{C_1}{C_t}V_i + \frac{C_2}{C_t}V_b = a_1 \cdot V_i + a_2 \cdot V_b \qquad (1)$$

$$I_d = \beta\left[\left(V_{gs} - V_{th}\right)V_d - \frac{V_d^2}{2}\right] \qquad (2)$$

$$I_d = \beta\left[\left(a_1 \cdot V_i + a_2 \cdot V_b - V_{th}\right)V_d - \frac{V_d^2}{2}\right] \qquad (3)$$

$$I_d = \beta \cdot a_1 \cdot V_i \cdot V_d + I_{offset} \qquad (4)$$

$$I_{offset} = \beta\left(a_2 \cdot V_d \cdot V_b - \frac{V_d^2}{2}\right) \qquad (5)$$

From (3) can be seen that if $a_2 \cdot V_b = V_{th} + V_{dsat}$, and $V_{dsM3} \le V_{dsat}$, thus $I_d = I_{dM3}$ will be a linear function of V_i. From (4) note that there is a dc component; this can be eliminated as shown in the circuit. The current source I_b must be equal to I_{offset} of equation (5). At the output of the controller could be needed a current to voltage converter. A typical converter is shown in Figure 6. The system implemented have *0A* as logical level "0" and *10μA* as logical level "1" at the input. To provide output voltages around of 1 volt the floating linear resistance needed is about *100KΩ*. This can be a problem when this resistance is implemented in an IC due to its large value and consumed area. Thus, replacing the floating linear resistor with the voltage to current converter proposed, a near rail-to-rail current to voltage converter can be obtained. Figure 7 shows the resulting circuit.

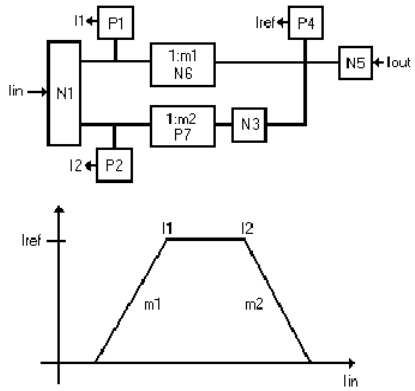

Fig. 2 Current Mode Membership Function Circuit.

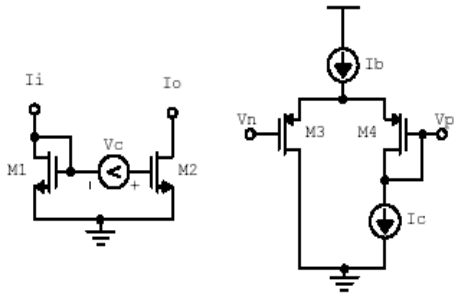

Fig. 3 Programmable Gain Current Mirror (PGCM).

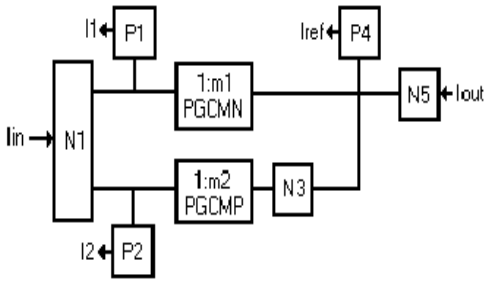

Fig. 4 Programmable Membership Function Circuit.

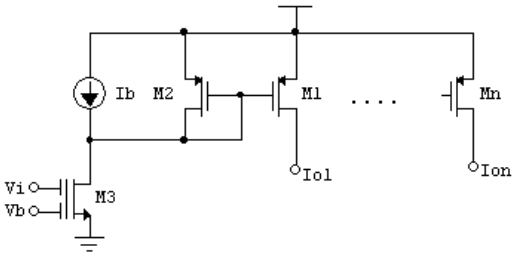

Fig. 5 Linear Transconductor using Floating Gate MOS Transistors.

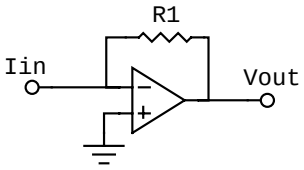

Fig. 6 Typical Current to Voltage Converter.

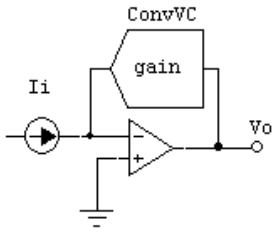

Fig. 7 Current to Voltage Converter using a Voltage to Current Converter.

2.2 Min-Max Operators

The circuits presented in [8] were adopted for Min-Max operators. As can be seen only current mirror were used. These circuits like those of the PMFC are biased by the input signal. Since the mirrors of these circuits don't operate all along, a decrement of the power consuption is expected. This is an advantage for implementations for low voltage applications. Min-Max circuits are shown in Figure 8.

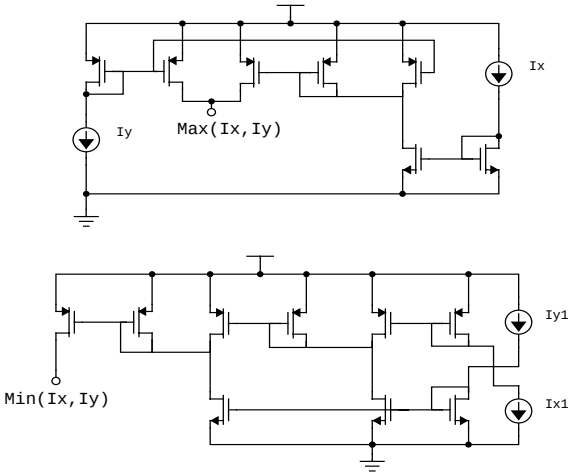

Fig. 8 Min-Max Operators.

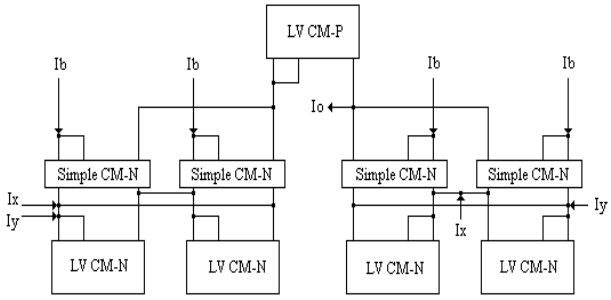

Fig. 9 Multiplier.

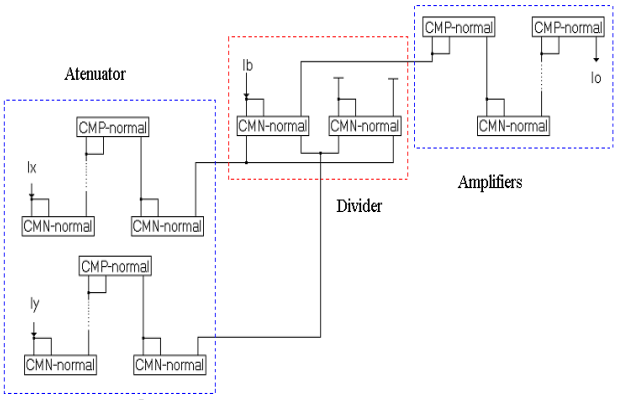

Fig. 10 Divider.

2.3 Consequents and Defuzzifiers

Since, *singletons consequents* only scale or multiply the antecedent by a factor $0 \leq C_i \leq 1$. A multiplier or a PGCM can be used to scale the signals. The multiplier circuit was proposed in [9]. The original version of the multiplier uses normal current mirrors. In this case normal current mirrors were replaced with low voltage current mirrros. The divider presented in [10] is used in the defuzzification. The divider needs to operate in weak inversion. In order to use currents in the μA rank, exist the need to attenuate the signal at the input of the divider and amplify it later at the output, if it is necessary. Figures 9 and 10 show the multiplier and divider respectively.

3 Simulations and Results

In the simulated controller each PMFC have five control parameters (breakpoints I_1, and I_2; slopes m_1, and m_2, and I_o magnitude). Input ranges are: $0A \leq I_{in} \leq 10\mu A$, and $0V \leq V_i \leq 1.2V$. The complete system is supplied with 1.2V. Figures 11 and 12 show the response of the PMFC for a current input and a voltage input respectively. As can be seen, the programming of several slopes is achieved in both types of circuits. In every current input can be added a voltage to current converter in case of the systems only work with voltages at the input. The controller was compared with a simulation in MATLAB for a typical surface with 5 symmetrical memberships equally spaced, min circuits as logical operators and 5 multipliers for the singletons. Figure 13 shows the surface for the system simulated in MATLAB and figure 14 shows the surface for the system simulated in CADENCE enviroment with a technology of 0.8μm (AMS). The resulting surface is a good approximation of the ideal surface. In table 1 are summarized the principal characteristics of the controller.

Table 1. Controller's characteristics.

Voltage Supply (Vdd)	1.2V
Current Bias (Ib)	10μA
Number of inputs	2
Number of outputs	1
Number of rules	25
Membership Programmability parameters	5
Operation in Voltage or Current Mode	
Singletons Programmability	
Fixed Fuzzy Rule Base for embedded systems	

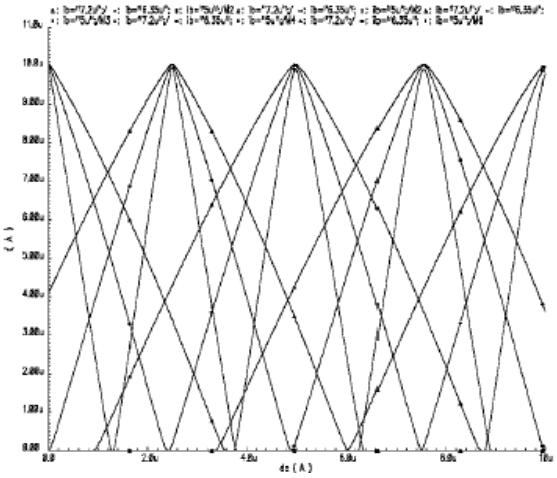

Fig. 11 Simulation results for PSMFC with current inputs.

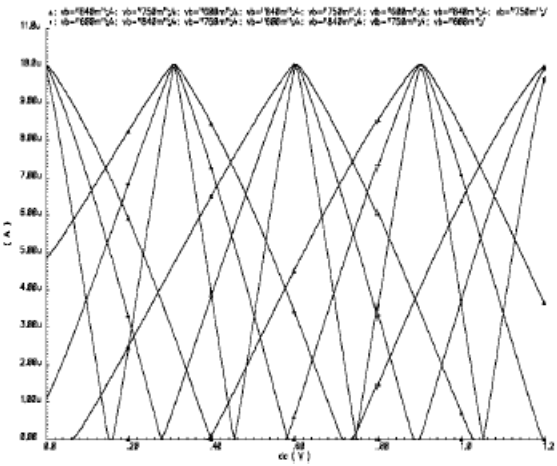

Fig. 12 Simulation results for PSMFC with voltage inputs.

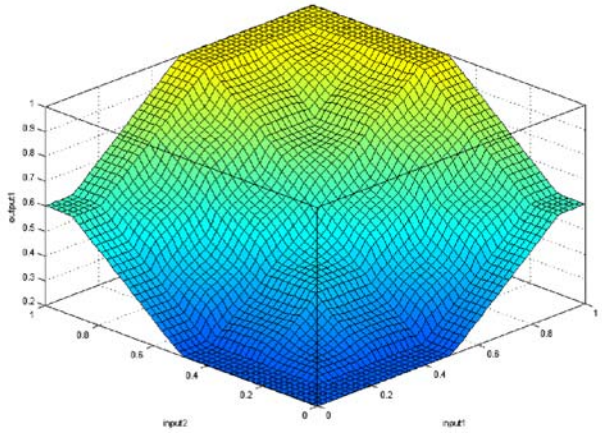

Fig. 13 Matlab Simulation.

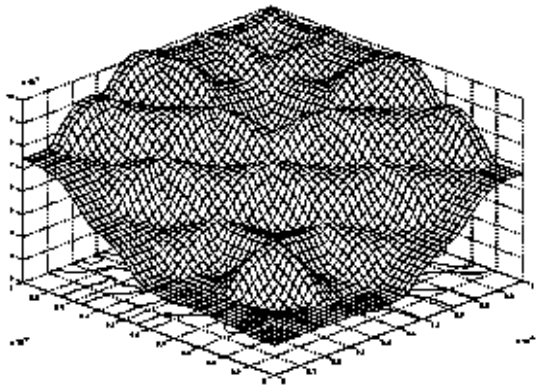

Fig. 14 Circuit Simulation.

4 Conclusion

In this paper an Analog Fuzzy Controller has been presented. All its parameters can be simultaneously tuned in continuous time. The design is based on the simplest current-mode processing. In order to obtain very compact solutions for complete fuzzy systems. Current mode processing offers a good trade-off between performance and simplicity of the design. But, external voltage processing can be achieved by using linear transconductor and transresistor amplifiers. A zero-order Sugeno architecture was designed and its performance was compared with Matlab simulations obtaining a good performance. The controller was designed in a AMS CMOS 0.8μm technology operating at *1.2V* and a I_b*=10*μ*A*.

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