Analog Circuit Synthesis: A Proposed Approach to Design VFs

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Abstract: An automatic methodology focused on the synthesis of voltage followers (VFs) at the transistor level is introduced. The synthesis procedure is executed in four basic steps: selection of a generic cell composed of nullators; the manner in which a norator is added to form joined nullator-norator pairs; addition of the biasing circuitry and finally; synthesis of each joined pair by a BJT or a MOSFET. The best transistor-circuit design is selected among all the generated combinations according to their frequency response calculated using SPICE.

Key-Words: - Analog Design Automation, Circuit Synthesis, Transistor Circuits, Biasing Techniques, Nullor.

1 Introduction

Fully automated design of analog circuits remains quite complicated due to their topological complexity [1]. That is, there is no simple rule neither to describe nor to establish the number of possible topologies even with few components [2]-[4]. Although several efforts has been devoted to enhance the capability of synthesis for several active devices [1]-[8], the selection of a correct topology along with the biasing problem, constitutes the most complicated part of analog design automation at the transistor level of abstraction [1],[7],[10]. The basic idea in selecting topologies can be referred to the synthesis method given in [3], which explores all combinations in connecting generic two-terminal elements, namely: impedances, nullators, and norators. However, that method is not performed at the transistor level.

The method given in [7] sets the guidelines to aid the automatic synthesis by generating the small signal design and by adding the bias circuitry at the transistor level. Henceforth, this work introduces the manner in which an automatic system generates the design of VFs at the transistor level by manipulating the interconnection relationships of nullators and norators, which are shown in Fig. 1. In this manner, in section 2 are introduced several generic topologies to implement a VF. In section 3, it is described where and how to add norators to form joined pairs [7]. The manner in which the biasing circuitry is automatically added is introduced in section 4.

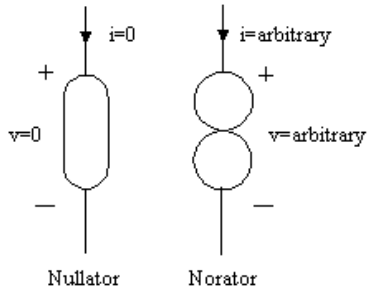

Fig. 1 The nullor is composed of a nullator and a norator

The synthesis of joined nullator-norator pairs by using either BJTs or MOSFETs is shown in section 5. The proposed algorithm and an example in synthesizing VFs is given in section 6. Finally, the conclusions are summarized in section 7.

2 Generic cells

Analog design automation at the transistor level of abstraction can be devoted to the synthesis from a set of generic cells [1]-[8]. The first synthesis-step can be related to the generation of the small-signal design, which can be done by coupling generic cells [2],[6]-[8]. In this manner, the analog design automation of VFs can be done by modeling their ideal behavior by using nullators [7], like a single nullator, two nullators, or four nullators, as shown in Fig. 2.

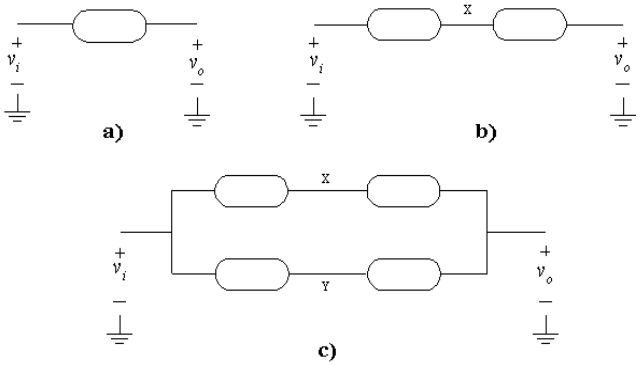

Fig. 2 Generic cells to implement a VF.

3 Forming joined nullator-norator pair

This section introduces how an automatic system adds one norator (P) to a nullator (O) to form a joined pair suitable for biasing and synthesis purposes. Lets consider the VF shown in Fig. 2a, to form a joined pair there exist three combinations as shown in Fig. 3. Since a norator is basically used to stabilize output variables [3], the joined pair shown in Fig. 3a is not suitable for biasing purposes, because by synthesizing the joined pair by a BJT or a MOSFET [7], v_i being connected between the emitter-collector or source-

drain terminals, resulting an impractical topology. The others joined pairs could be suitable for biasing purposes, since by applying symbolic analysis [9], ideally $v_o = v_i$. The number of combinations to add a norator to a nullator is established by (1), where n denotes the number of norators. From the multiple combinations, the ones suitable for biasing purposes are selected by applying heuristic reasoning rules [7].

$$combinations = 3^n \quad (1)$$

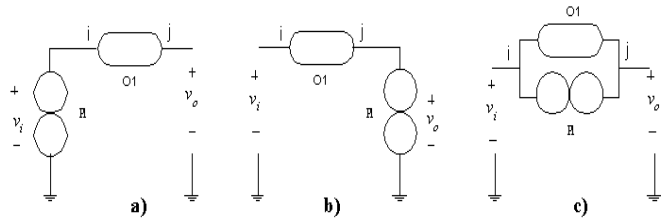

Fig. 3 Adding a norator to a nullator: (a) at node i, (b) at node j, and (c) between nodes i and j.

4 Addition of the biasing circuitry

The design of the biasing circuitry can be divided in two steps: Addition of voltage and current bias levels. The addition of the biasing circuitry to the VF shown in Fig. 3b, which nodes are generated as shown in Fig. 4a, is done as follows [7]: The data-structures of nullators and norators including their names and nodes are shown in Table 1. The addition of a dc global-bias voltage-source creates the global nodes (3,0), as shown in Fig. 4b. Searching combinations to connect nullators to node (3), for O1 there are 2 combinations, however neither node 1 nor node 2 should be connected to node 3, because they are related to the driving ports. Searching combinations to connect norators to node (3), for P1 there are 2 combinations, node 2 is discarded since it forms a joined pair with O1. Therefore, node 0 is relocated as shown in Fig. 4c, where a resistor R is inserted where P1 was connected to measure v_o. There is one possibility to add a dc local-bias voltage-source to node 1 by superimposing a voltage signal [8], as shown in Fig. 4d. It is not necessary to add bias current-sources since the circuit is fully biased. By applying the method given in [10], the uniqueness is guaranteed, so that the biasing design equations are given by (2). V_{P1} can be one half of V_{GBS} to drive symmetric excursion. From the nullator properties, the voltage across R equals to V_{LBS}. However, in real applications the voltage across O1 equals to either V_{BE} or V_{GS}, at the transistor level. For the VF shown in Fig. 3c, it is impossible to obtain a biased circuit. So that, although 3 combinations were generated, only one was well suited for biasing purposes.

$$I_Z = \frac{V_{GBS} - V_{P1}}{Z},\ V_Z = V_{LBS} - V_{O1} \quad (2)$$

Table 1 Data-structure of nullators and norators

Nullator	nodes	Norator	nodes
O1	1,2	P1	2,0

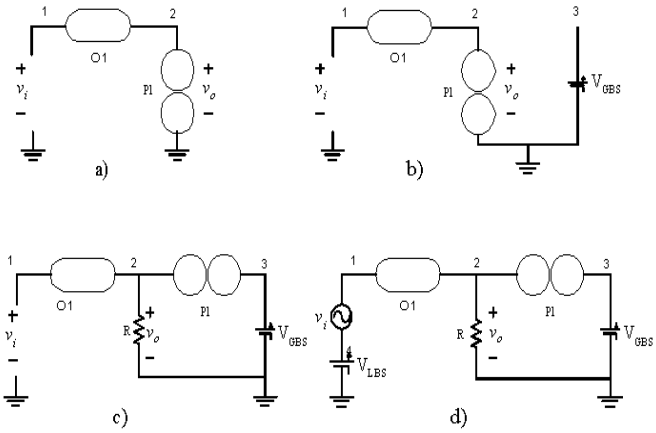

Fig. 4 Biasing the nullor circuit from Fig. 3b.

5 Synthesis of transistor circuits

From Fig. 4d, the net-list of the nullor circuit is given in Table 2. The joined pair formed by O1 and P1 is synthesized by a BJT and a MOSFET, as shown in Fig 5a and Fig. 5b, respectively. The kind of transistor: NPN or PNP for BJTs, and N-channel or P-channel for MOSFETs is selected by following the dc current direction of V_{GBS} to the reference node. Finally, the selection of a transistor model and its sizing is done by applying the methods in [1],[6],[11].

Table 2. Net-list of Fig. 4d

Element	Nodes
V_{GBS}	3,0
V_{LBS}	4,0
V_i	1,4
O1	1,2
P1	2,3
R	2,0

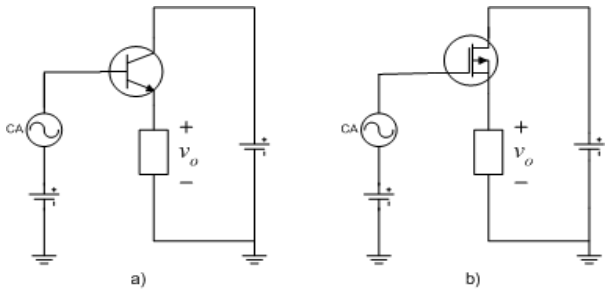

Fig. 5 Synthesis of the nullor circuit shown in Fig. 4d.

6 Proposed synthesis methodology

The proposed algorithm is sketched in Fig 6. By using (1) to the VF shown in Fig. 2c, the synthesis of 6 of the 81 combinations are shown in Fig. 7. These topologies are adjusted according to the design equations given in [12], to be simulated in SPICE. The results of the AC analysis are displayed in Fig. 8.

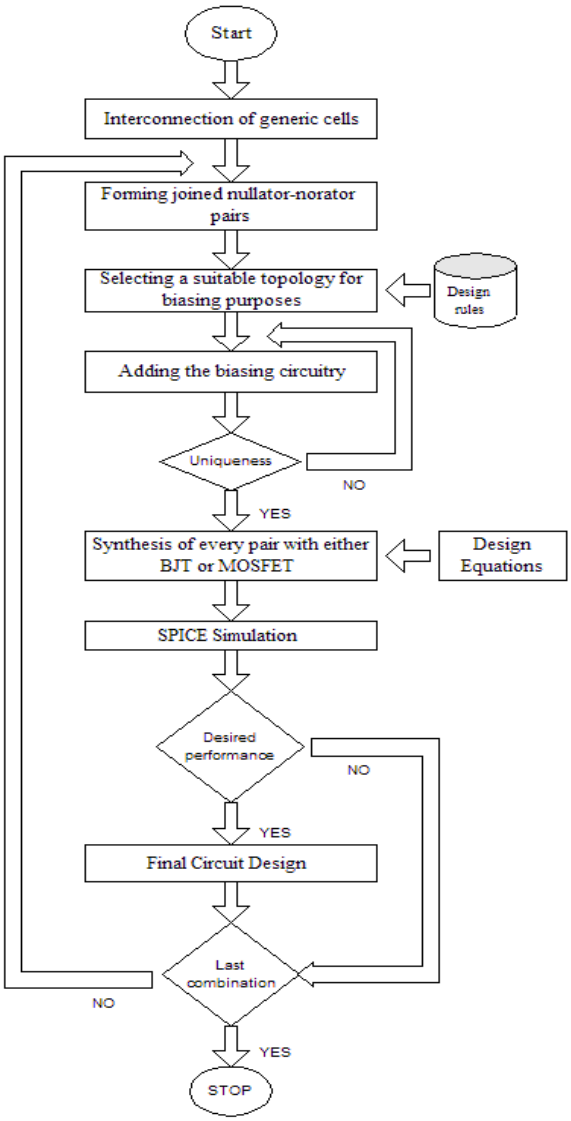

Fig. 6 Flow chart to the synthesis of active devices.

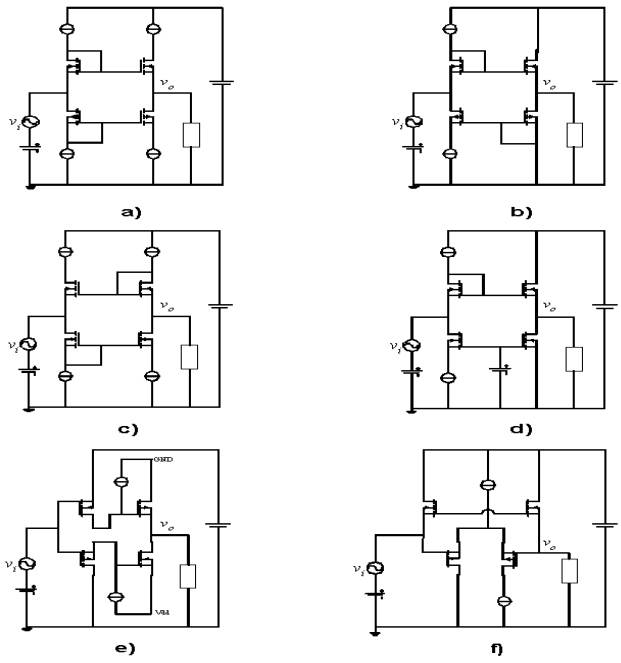

Fig. 7 Synthesis of the VFs from Fig. 2c.

7. Conclusion

It has been described an automatic methodology focused on the synthesis of VFs. The synthesis procedure has been divided in four basic steps from which optimization techniques can be applied to the final circuit designs in order to obtain the better behavior and high performance of them.

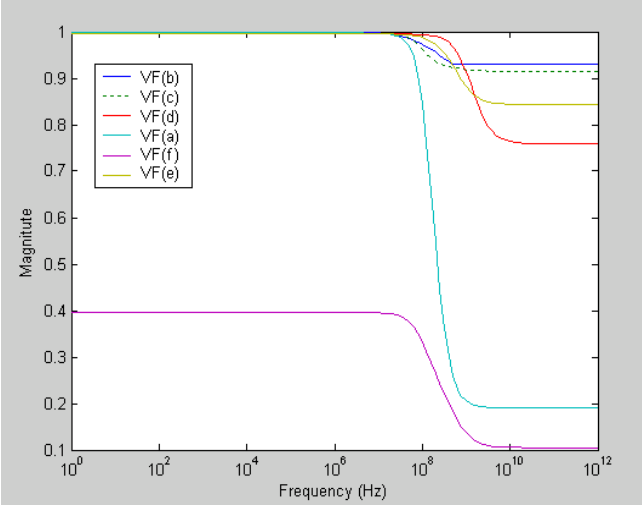

Fig. 8 Frequency response of the VFs.

Acknowledgment

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