

# Interactive System for the Symbolic Analysis of Analog Circuits

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**Abstract:** - An interactive system called SIASCA which automates the calculation of symbolic expressions (SEs) representing the dominant behavior of analog circuits, is introduced. SIASCA includes a more general class of active devices whose behavior is modeled at different levels of abstraction using nullors in order to enhance the capability of symbolic analysis to calculate simplified SEs.

**Key-Words:** - Symbolic Analysis, Analog Design Automation, Frequency Response, Nullor.

## 1 Introduction

Symbolic analysis is focused on the calculation of simplified SEs [1]-[6], which represent the dominant behavior of an analog circuit. The calculated SEs help the designer to gain insight and get an inference about the behavior of a circuit. Furthermore, it is very much needed that the calculation of SEs be guided towards an interactive design process by generating analytical design equations, useful for synthesis and optimization procedures [7]-[9]. In this manner, this paper is focused on the development of an interactive system called SIASCA, which calculates simplified SEs of analog circuits. As shown in Fig. 1, SIASCA includes a more general class of devices, namely: opamps [4], OTAs [5], CCII- [7], BJT and MOSFET. The basic set of primitives [2]: controlled sources, independent sources, resistor, inductor and capacitor are selected from the Elements button. The analog ground sets a reference node to (0), as it is usually done by any circuit simulator alike SPICE. SIASCA has been developed under Visual Java++, while the analysis procedures are implemented using MAPLE 8.0<sup>TM</sup>.

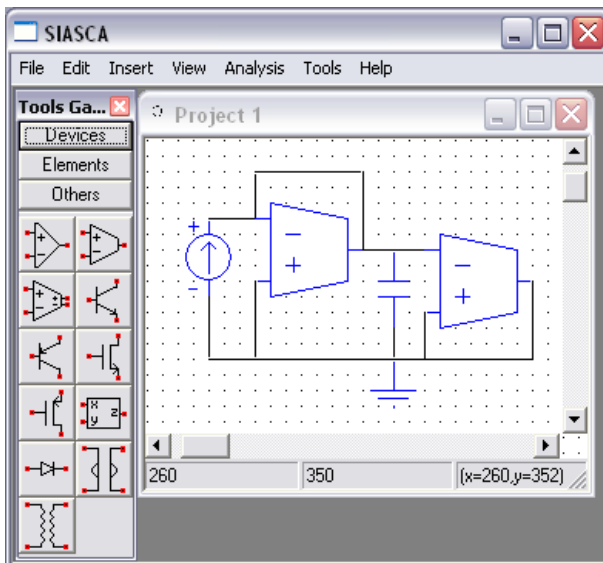


Fig. 1 The graphical user interface of SIASCA.

## 2 The modeling approach

To minimize the complexity in computing SEs using SIASCA, the behavior of all active devices are modeled at different levels of abstraction using nullors [5],[6]. This modeling approach is quite useful to formulate a compacted system of equations (CSEs) [1]-[3]. For example: The behavior of the three terminals MOSFET can be modeled at different levels of abstraction, e.g. the generic MOSFET is shown in Fig. 2a. The addition of the transconductance, output conductance and gate-source capacitor can be added as shown in Figs. 2b, 2c, and 2d.

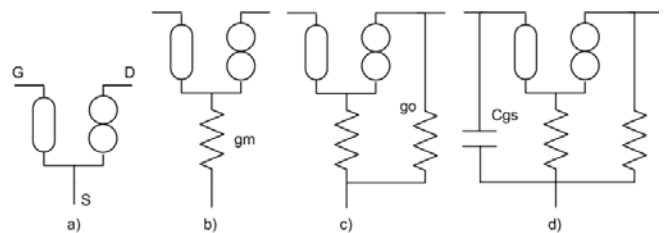


Fig. 2. Modeling the MOSFET using the nullor.

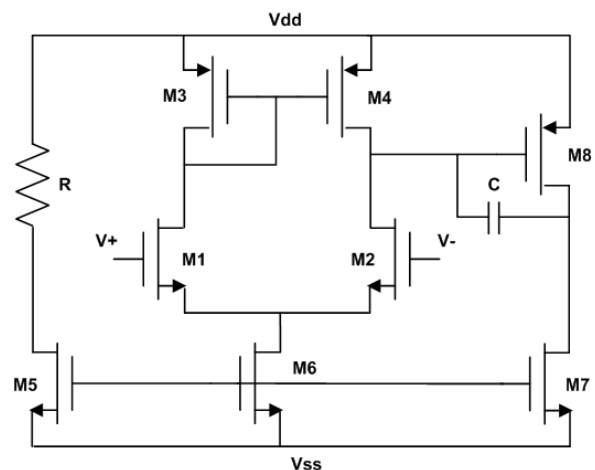


Fig. 3. Miller Operacional Amplifier.

The selection of a correct model which minimizes the computational effort in doing small-signal symbolic-analysis, depends on both the biasing and frequency operating conditions [6]. For example, to calculate

the symbolic transfer function (TF) of the Miller opamp shown in Fig. 3, by using the model shown in Fig. 2d, to replace the eight MOSFETs, the resulting TF would have an order higher than two. On the other hand, by selecting the appropriate model to each MOSFET, as it is described in the following section, the resulting TF would be of order 1 or 2, good enough to characterize the opamp [6].

### 3 The analysis stage of SIASCA

For a nullor circuit, the computation of a SE can be reduced to the manipulation of the nullator and norator interconnection relationships (IRs) [1],[5]. The Cartesian product of the IRs results in the formulation of a CSEs, like by applying the nodal analysis method [2]. The order ( $m$ ) of the CSEs is determined by the number of nodes ( $n$ ), minus the numbers of nullors ( $N$ ) [3]. In this manner, the computation of a CSEs leads us to formulate (1), where the compacted linear admittance matrix is obtained by associating indexes row-column (R,C), from the Cartesian product of the IRs of norators and nullators [5]. IRs of admittances ( $Y$ ) are associated according to (2), where  $i$  and  $j$  denote the nodes.

$$i_{CNA} = Y_{CNA} v_{CNA} \quad (1)$$

$$+ Y_{ij} \forall (i = j) \quad (2)$$

$$- Y_{ij} \forall (i \neq j)$$

The indexes to compute the elements of the matrix in (1), are obtained as follows:

- IRs of norators: From the properties of norators [3], its associated indexes are structured by considering that nodes  $i,j$ , where a norator is connected, are virtually short-circuited, and that indexes are associated to row variables (currents).
- IRs of nullators: From the properties of nullators [2], its associated indexes are structured by considering that nodes  $i,j$ , where a nullator is connected, are virtually short-circuited, and that indexes are associated to col variables (voltage).
- The cartesian product of the IRs of norators and nullators generates the sum of those admittances associated to each pair (R,C), which are searched in the IRs of the admittances.

### 4 Examples

Lets consider the inverting amplifier shown in Fig. 4. To compute its symbolic TF, SIASCA calculates the equivalent nullor circuit shown in Fig. 5. As one sees, the independent voltage source is transformed into an independent current source in order to apply the compacted nodal analysis method [3],[5].

The order of the CSEs is equal to:  $m=n-N=2$ . The matrix in (1) is computed as follows [5]:

- IRs of norators are shown in Table 1. The row-variables are: [(1), (3,4)]. As norator P1 is connected between (2,0) node 2 is eliminated.
- IRs of nullators are shown in Table 2. The column-variables are: [(1,2,4), (3)].
- The Cartesian product of the IRs generates the 4 elements of the matrix in (1):
 
$$(Y_{11} \in Y_{CNA}) = (1,1) + (1,2) + (1,4)$$

$$(Y_{12} \in Y_{CNA}) = (1,3)$$

$$(Y_{21} \in Y_{CNA}) = (3,1) + (3,2) + (3,4) + (4,1) + (4,2) + (4,4)$$

$$(Y_{22} \in Y_{CNA}) = (3,3) + (4,3) \quad (3)$$
- Searching the admittance associated to each pair (R,C) in Table 3, the final formulation of the CSEs is expressed by (4). Its solution by applying Cramer's rule, with  $G=1/R$ , is given by (5).

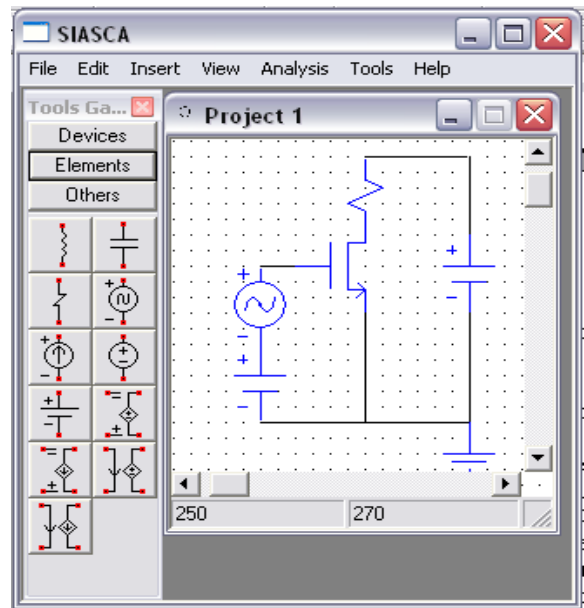


Fig. 4 Schematic capture of a transistor amplifier

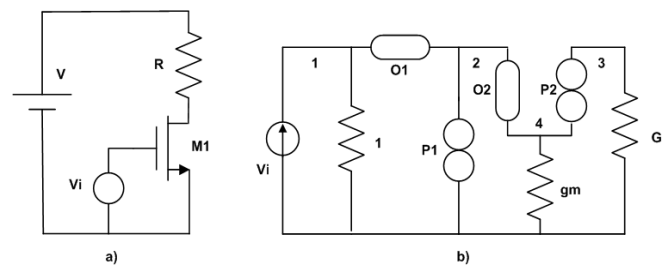


Fig. 5 Small-signal equivalent nullor circuit of Fig. 4.

TABLE 1. IR OF NORATORS

Norator (P)	Associated Nodes
P1	2,0
P2	3,4

TABLE 2. IR OF NULLATORS

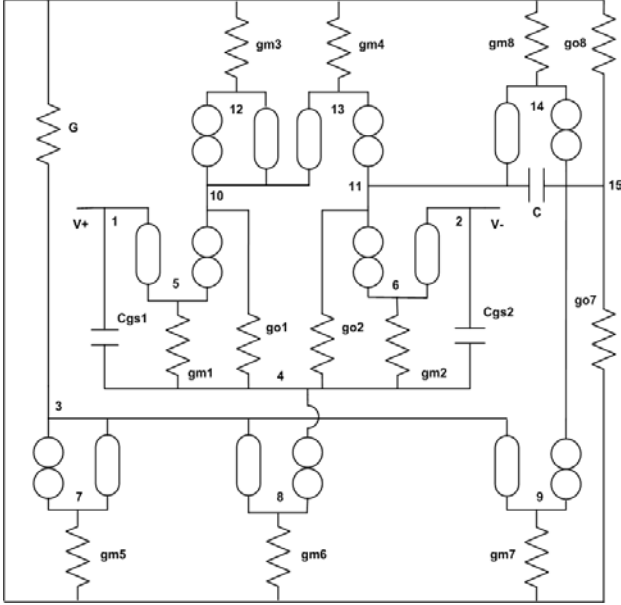
Nullator (O)	Associated Nodes
O1	1,2
O2	2,4

**TABLE 3. IR OF ADMITTANCES**

Admittance	Associated Nodes
G	3,3
gm	4,4
l(vi)	1,1

$$\begin{bmatrix} v_i \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ gm & G \end{bmatrix} \begin{bmatrix} v_{1,2,4} \\ v_3 \end{bmatrix} \quad (4)$$

$$\frac{v_o}{v_i} = \frac{v_3}{v_i} = -\frac{g_m}{G} = -g_m R \quad (5)$$



**Fig. 6.** Miller opamp using nullors

The equivalent nullor circuit of the Miller opamp shown in Fig. 3, is shown in Fig. 6. The order of its CSEs is:  $m=7$ , by applying the MNA method [4], the order increases in one to include the voltage source between (1,2). The CSEs is obtained as follows:

- IRs of norators: (5,10), (6,11), (10,12), (11,13), (3,7), (4,8), (9,15), (14,15). The row-variables are: [(1),(2),(3,7),(4,8),(5,10,12),(6,11,13),(9,14,15)]
- IRs of nullators: (1,5), (2,6), (10,12), (10,13),(3,7), (3,8), (3,9) and (11,14). The column-variables are: [(1,5),(2,6),(3,7,8,9),(4),(10,12,13),(11,14),(15)].
- The Cartesian product generates 49 elements of the CSEs, and the stamp of the voltage source adds 15 elements, so that the CSEs is given by (6).

As one sees, the MOSFETs M7-M8 of the Miller opamp has been modeled by using Fig. 2c, while M1-M2 has been modeled by using Fig. 2d. If 4 terminals MOSFETs were used, the nullor model would be more elaborated [4]. The other MOSFETs has been modeled using Fig. 2b, since they are biasing M1-M2 and M8, mainly. The solution to (6) is computed by considering that:  $gm2=gm1$ ,  $Cgs2=Cgs1$ ,  $gm6=gm5$ ,  $gm4=gm3$ ,  $go2=go1$ . The simplified symbolic TF is given by (7).

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ v_i \end{bmatrix} \begin{bmatrix} sC_1 & 0 & 0 & -sC_1 & 0 & 0 & 0 & 1 \\ 0 & sC_2 & 0 & -sC_2 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & G+g_3 & 0 & 0 & 0 & 0 \\ -g_4-sC_1 & -g_2-sC_2 & g_5 & g_4+g_2+sC_1+sC_2+g_4+g_2 & -g_4 & -g_2 & 0 & 0 \\ g_{m1} & 0 & 0 & -g_{m1}-g_4 & g_4+g_3 & 0 & 0 & 0 \\ 0 & 0 & g_{m2} & 0 & -g_{m2}-g_2 & g_4 & sC_1+g_2 & -sC_1 \\ 0 & 0 & 0 & g_7 & 0 & 0 & g_8-sC_1+g_7+g_8 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{15} \\ v_{26} \\ v_{3789} \\ v_4 \\ v_{10,2,3} \\ v_{11,4} \\ v_{15} \\ v_{15} \\ v_{15} \end{bmatrix} \quad (6)$$

$$TF = \frac{(-g_{m8} + sC)g_{m1}}{sC(g_{o7} + g_{o8} + g_{m8})} \quad (7)$$

## 5 Conclusion

An interactive system called SIASCA to compute simplified SEs in analog circuits has been described. The main advantages of SIASCA are that it includes a more general class of analog circuits and that their behavior is modeled by nullors at different levels of abstraction. The modeling approach minimizes the computational complexity to formulate a CSEs, which is carried out by computing the Cartesian product of the IRs of the norators and nullators. Finally, the method sets the guidelines to choose the correct model to minimize computational complexity, by considering the bias and frequency operating condition of a device.

## Acknowledgment

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