Neural-MOS Threshold Gate as a Way to Design On-Chip Learning Neuron Structures

RAFAIL LASHEVSKY
Hardware Department
The University of Aizu
965-8580
JAPAN

Abstract: - Hardware implementation of artificial neuron networks (ANN) based on MOS-transistors with floating gates (Neuron MOS or νMOS) is discussed. Comparison of two type on-chip learning neurons with digital and analog input weight storing is provided. The main problem in design the neuron with analog input weight memory is tolerance to deviations of circuit elements parameters and supplied voltage deviation. New neuron circuit that can compensate all kind of deviations is proposed and investigated. Design methodology of such a circuit and result of simulation are shown.

Key-words: Neural-MOS structures, νMOS transistors, artificial neural networks, analog voltage weight representation, deviation tolerance.

1 Introduction

Software implementation of Artificial Neural Networks (ANN) is flexible, but advantage of hardware implemented ANN over software realization is very fast performance. The demand to modern ANN is hundreds of neurons and tens of thousands of synapses. The known hardware implemented ANN have sufficiently rigid limitations of the networks parameters. To overcome these limitations is the goal of many researchers. It looks possible because today's microchip design rules is less than $0.2\mu m$ and transistors dimensions minimization after five-six years up to $0{,}06\mu m$ is obvious [1]. As a result the integration and density of transistors on the chip will increase in many times. Together with new so called Neural-MOS structures concept it opens very effective way for Bio-inspired systems [2] based on Intelligence Implementation to Silicon Chip [3] such as ANN and Fuzzy Logic. If the single MOS-transistor is only a switch, the Neural-MOS structure represents multi-input threshold gate and such a gate can be used as neuron with a large number of synapses.

It is known two ways of designing Neural-MOS structures: transistors with floating gate – (*νMOS*) [3], what is voltage-mode Neural-MOS, and *β-driven* threshold element [4,5], what is current-mode Neural-MOS.

Transistors with floating gate looks better for design ANN because of very small static power dissipation, and higher elements parameters and supplied voltage deviation tolerance.

In our previous publication [6] we developed the design methodology of two types threshold gates, based on the floating gate νMOS – static (Fig.1) and clocked (Fig.2).

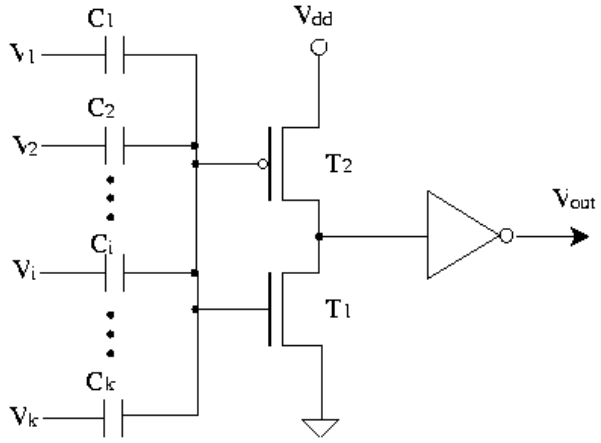

Fig.1 Static νMOS threshold gate

The main advantage of such a methodology is taking into account the elements - transistors and capacitors – parameters deviation peculiar to real chip manufacturing process and in addition the supplied voltage deviation. It was shown that these deviations restricted the number of inputs in static threshold gates described in [7] by the value not more than 10.

The same reasons lead to increasing input capacitors values and as a result chip area occupied by the gate if number of input increases. The last one is because of capacitance relational deviation became less for bigger capacitors.

Increasing input capacities in addition led to increasing dynamic part of consumed power.

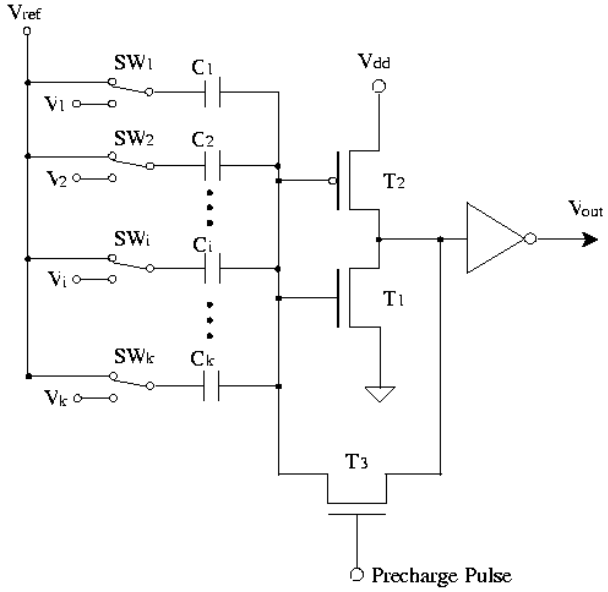

Fig.2 Clocked νMOS threshold gate

The clocked approach proposed in [8] eliminate the influence of transistors parameter deviation, but not the deviation of capacitance's and supplied voltage. As shown in [6] in clocked νMOS threshold gates number of inputs could be increased up to many tens. But the chip area increased, because of additional switches in the each of the gate input.

The parameter deviation influence can be substantially overcame in case of on-chip learning ANN (LANN) by choosing in learning process appropriate input weights value to compensate such a deviation. As a result we can minimize input capacitance value and dramatically (tenths of times) decrease chip area, increase performance and improve the main LANN parameters, such as sum of weights, number of inputs and weight setting accuracy. It was shown in [6], where we discussed neuron with digital way of input weight storing. The disadvantage of digital weight representation is large capacity RAM as an inputs weight memory.

Analog input weight storing in non-volatile EEPROM memory proposed in [9]. Another way of using in the future non-volatile ferroelectric memory proposed in [10]. Disadvantage of weight changing and very long learning time. Input weights change takes up to several microseconds.

We estimated the possibility of design LANN with analog input weight storing, where inputs weight represents by voltage level in the capacitor based analog voltage dynamic memory [11].

Disadvantage of using dynamic memory is necessity of periodically refreshing because of discharging the dynamic memory cell capacitor by parasitic leakage current. This problem can be solved by periodically repeating the learning process, if the holding time is enough. Holding time is the time before weight represented voltage will change on the maximal permissible value. This time depends from memory capacitor and leakage current values. We estimated such a time as hundreds of milliseconds. Because delay time of clocked νMOS structure is tenths of nanoseconds, it is enough time to get weight refreshing.

As another way of weights refreshing, we propose νMOS based multistage voltage comparator (MSVC). The idea of such an approach is periodically comparison the value of analog voltage in dynamic memory with voltage levels corresponding to the different input weight stages. Number of stages defines the weight setting accuracy. If the difference between weight voltage in the memory and voltage stage is small enough, the signal of weight increment is generated. One of the main problem in LANN design is how to avoid the influence of supplied voltage deviation and voltage noises on the circuit behavior, because of the possible voltage difference in learning and working times. Such a difference can lead to incorrect neuron behavior. In case of non-stable supplied voltage we have to restrict sum of weights, number of inputs or weight setting accuracy. As it will be shown, the 1% supplied voltage deviations decrease maximal sum of weights in 4 times and 5% deviations in 16 times. Such a deviations is possible, for example, as the result of noises.

Using SPICE simulation, the maximal sum of weights and number of inputs for proposed LANN was estimated together with time parameters, such as weight holding time and output calculation time.

Design methodology and circuit decision which used to get tolerance to element parameters, dimensions and supplied voltage deviations will be especially important to design LANN based on the future CMOS processes with lesser element sizes and supplied voltages and distinct deviations.

Supplied voltage tolerant LANN could be useful with other types of weight memory, for example with EEPROM or ferroelectric memory.

2 General LANN structure

The neuron with $\boldsymbol{k}$ synapses calculates the threshold function:

$$F = \sum_{i=0}^{k} \omega_i x_i - T$$

Here xi and ωi - input variables and input weights correspondingly, T – function threshold.
Floating gate νMOS structure with k inputs represents the threshold function as:

$$V_{out} = \frac{1}{k}\sum_{i=0}^{k} V_{\omega,i} x_i - V_T = V_f - V_T$$

Here $V\omega,i$ – input voltage represents input weight, V_T – threshold voltage, V_f – the floating gate structure output voltage, $Vout$ – the comparator output voltage.

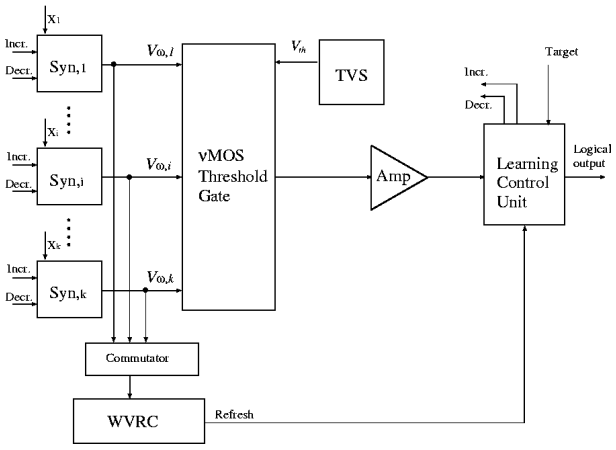

Fig.3 Block diagram for the neuron structure

The neuron in general consist (Fig.3) from a set of main parts:

- synapse circuit (***Syn***) to calculate $\omega i\ xi$, where ωi is represented by $V\omega,\imath$ - the synapse output voltage,
- νMOS threshold gate for Vf calculations (**TG**),
- threshold voltage source (**TVS**),
- amplifier (**Amp**),
- learning control unit to form out the increment/decrement signal in the learning process,
- weight refreshing circuit (**WVRC)** with multistage voltage comparator and commutator for periodically and consequent connection synapses dynamic memory sells to WVRC.

3 Deviation-tolerant LANN structure

As it pointed in the introduction one of the main problem in LANN design is to get the tolerance to supplied voltage deviations. Such a deviation sharply reduces maximal sum of weights.

We have to distinguish three types of deviations: very slow, slow and fast.

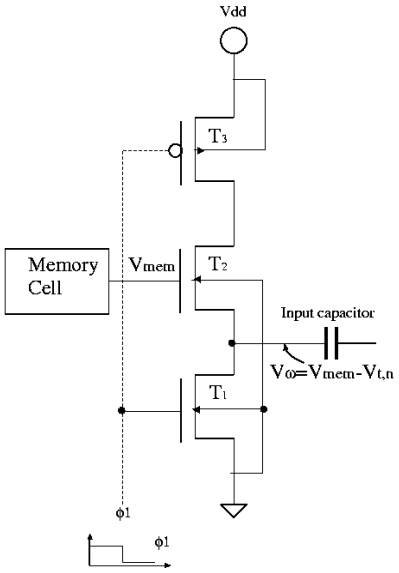

Fig.4 Synapse circuit

The first means we have different voltage in time of calculating different function, the second – in time of calculating one function and the third case - different voltage in time of different clock pulses.

Fig.4 represents the synapse circuit with dynamic analog voltage memory sell (Fig.5).

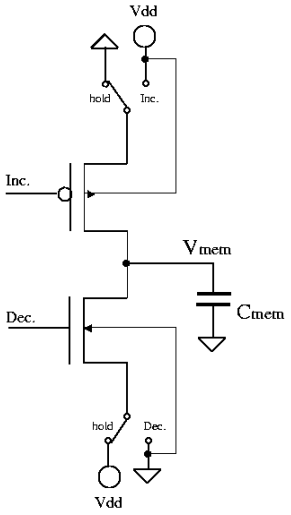

Fig.5 Memory cell circuit

The circuit based on nMOS type source follower. Since the bulk of νMOS is connected to the ground, transistor threshold voltage is stable against *Vdd* deviation. As a result it gives stable synapse output weight voltage. To overcome the influence of the deviation on the **TG** we proposed [11] the circuit decision shown in Fig.6. Floating gate voltage of the **TG** can be calculated as:

$$V_f = \frac{C_{th} \cdot V_{th} - C_\omega \cdot V_\omega}{C_{th} + C_\omega} + V_{ref}$$

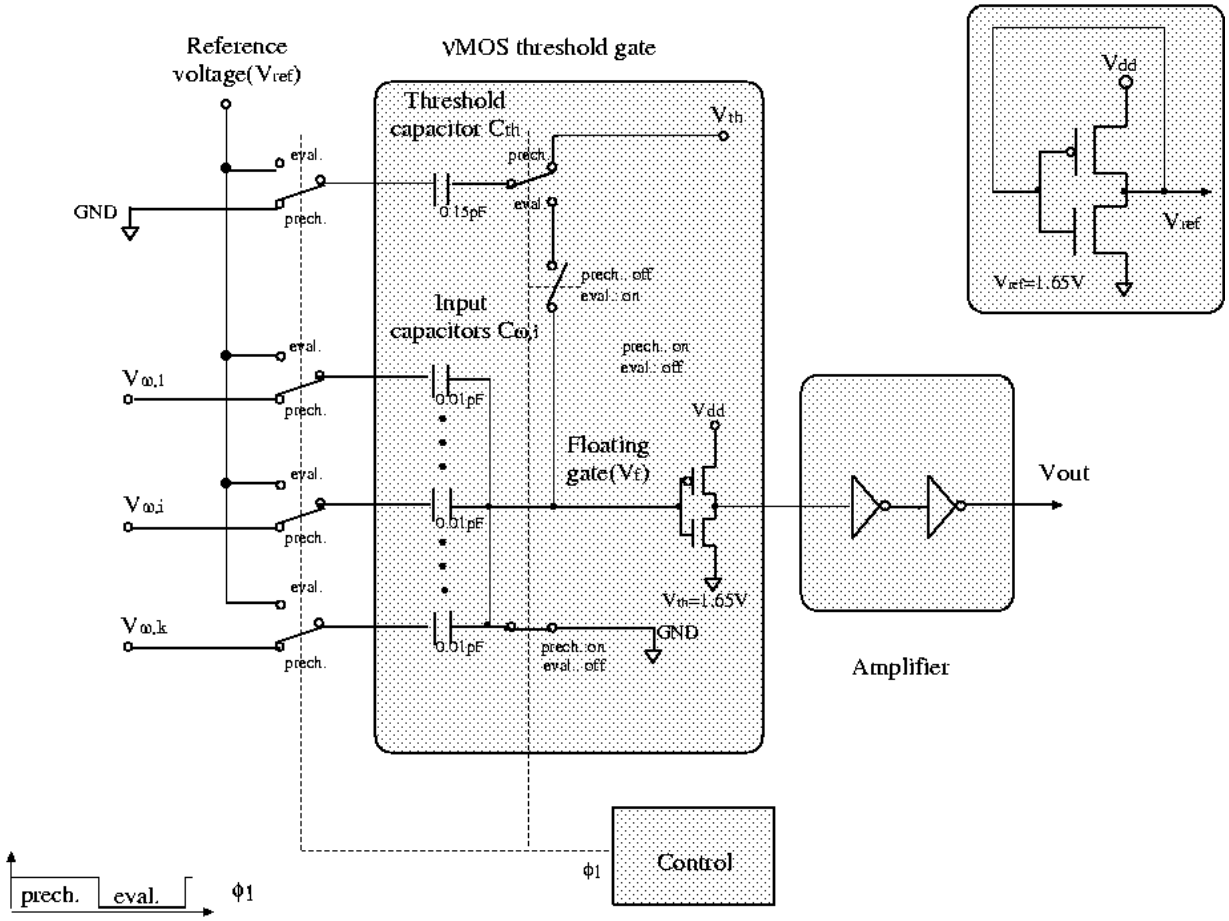

Fig.6 Neuron circuit

Fig.6 shows the new neuron circuit, which is tolerant to supplied voltage deviations.

Since **TG** threshold voltage *Vth* and weights voltages *Vw* both stable against *Vdd* deviations because of using n-type source followers, the equation for getting tolerance to *Vdd* deviations is:

$$\frac{\delta V_f}{\delta V_{dd}} = \frac{\delta V_{ref}}{\delta V_{dd}} = \frac{\delta V_{th}}{\delta V_{dd}}$$

The floating gate voltage deviation in the evaluation phase depends only on the value of the reference voltage in this phase. If *Vref* variations the same as inverter threshold voltage variations, floating gate voltage vary in the same as inverter threshold voltage. It will be in the case of using as the reference voltage source the inverter with shorted out input and output. It is the way to compensate all kinds of *Vdd* deviations.

Using HSPICE simulation we found the maximal sum of weights for the proposed neuron circuit and ordinary clocked νMOS neuron circuit for slow and fast deviations of supplied voltage. Value of deviations changed up to 10%. Maximal sum of weights for the proposed circuit in comparison with circuit without compensation mechanism is shown in Fig.7. There is no advantage of this structure in the case of less then 1% deviation since additional circuit components reduce sensitivity of neuron. Nevertheless if the deviation is more than 1%, efficiency of this circuit is obvious. The maximum

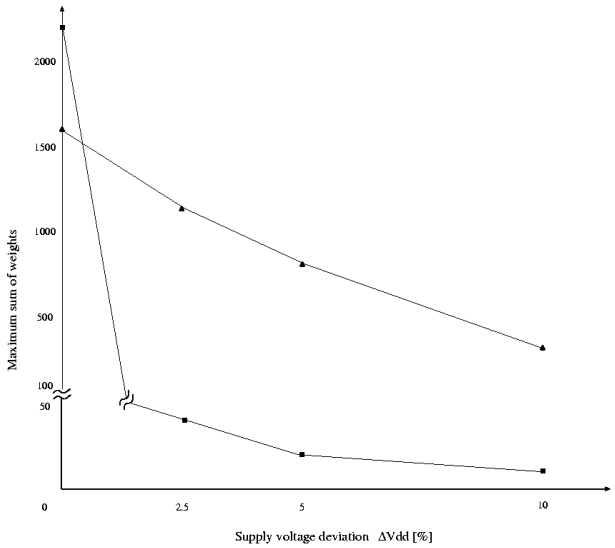

Fig.7 Comparison between proposed circuit and circuit without compensation

sum of weights for 5% deviation is near 800. In contrast for the circuit without compensation the sum of weights only 20.

4 Conclusion

In our research we developed the design methodology for static and clocked threshold gates, which could be used as on-chip learning neurons, taking into account possible deviations of elements (transistors and capacitors) parameters and supplied voltage [6], [11]. Using such a methodology it was shown that simple static approach has very strong restriction in number of inputs and sum of weights. The more complicated clocked approach is stable against transistors parameter deviation, but not stable against deviations of supplied voltage. Proposed new floating gate circuit opens the way of design the neuron with sum of weights up to 800 in the case of very high supplied voltage deviation up to 5%.

References:

[1] Yan Borodovsky, Lithography – this amazing technology. *International Symposium on Future of Intellectual Integrated Electronics*, Sendai, Japan, March 14-17,1999, p.p23-24.

[2] EricVittoz, Bio-inspired system based on analog VLSI. *International Symposium on Future of Intellectual Integrated Electronics, Sendai, Japan, March 14-17,1999, p.p21-22.*

[3] Ohmi T., at al. Integrating intelligence on silicon electronic systems, *Symposium on VLSI Circuit Digest of Technical Papers.*

[4] Yamada T., Ikebe M., Amemiya Y., A current mode nMOS circuit for cellular automation device. *International Symposium on Future of Intellectual Integrated Electronics, Sendai, Japan, March 14-17,1999, p.p383-388.*

[5] Varshavsky V., Beta-Driven Threshold Element, *Proceedings of the 8-th Great Lakes Simposium on VLSI, IEEE Computer Society, Feb.19-21, 1998, p.p.52-58.*

[6] Lashevsky R., Takaara K., Souma M. (1999). The efficiency of neuron-MOS transistors in threshold logic, *Soft Computing 3 (1999), Springer-Verlag, p.p.20-29.*

[7] Shibata T., Ohmi T., A functional MOS transistor floating gate-level weighting sum and threshold operations, *IEEE Transactions. Electronic Devices, ED-39(6), 1444-1455.*

[8] Ozedemir H., Kepkep A., Pamir B., Leblebici Y. (1996). A capacitive threshold-logic gate, *IEEE Journal of Solid-State Circuits, 312, (8).*

[9] Shibata T., Ishii H., Ohmi T., A neuron-MOS neural network using self-learning-compatible synapse circuits. *IEEE Journal of Solid-State Circuits, vol.30, No.8, August 1995.*

[10] Ishiwara H.,Yoon S., Tokumitsu E., Fabrication of adaptive-learning neurochips using ferroelectric thin films. *International Symposium on Future of Intellectual Integrated Electronics, Sendai, Japan, March 14-17,1999, p.p249-258.*

[11] Lashevsky R., Sato Y., Deviation-Tolerant Floating Gate Structures as a Way to Design an On-Chip Learning Neural Networks. *Soft Computing (2001), Springer-Verlag ,in print.*

[12] Montalvo A., Gyurcsk R., Paulos J., Toward a General-Purpose Analog VLSI Neural Network with On-Chip Learning. *IEEE Transections on Neural Networks, vol.8, No.2, March 1997.*