# A Four-Quadrant Analog Multiplier Biased at 1.2V Working in Current-Mode

ALEJANDRO DÍAZ-M.[1], JUAN CARLOS SÁNCHEZ-G.[2] ,
MIGUEL GARCÍA-A.[1] and ESTEBAN TLELO-C.[1]
[1]Departamento de Electrónica - INAOE
Luis Enrique Erro No. 1 Tonantzintla, Puebla. P.O.Box 51 and 216. 72000

[2]Instituto Politécnico Nacional, SEPI Culhuacan
Santa Ana 1000, San Fco. Culhuacan, Coyoacan, México.
MEXICO
ajdiaz@inaoep.mx

*Abstrac*: - Analog multipliers are widely used in fuzzy logic, analog signal, and parallel processing systems. The most important is that, since low-voltage applications have become popular, several efforts have been oriented to improve the performance of the proposed designs. In that way, a design of a current-mode four-quadrant analog multiplier, based on the translinear principle, and biased at 1.2V, is presented. Simulation results using HSPICE show an improvement on the linearity. The proposed circuit was designed using CMOS technology of 0.8μm process parameters from AMS.

*Key-Words*: - Analog circuit, multipliers, low voltage, current-mode, translinear mos.

## 1 Introduction

Portable electronic systems have become popular for cosmopolitan lifestyle; thus, analog designers have been focused several efforts towards the development of low-voltage design methodologies. At the same time some proposed techniques are oriented to design low-voltage analog integrated circuits, it has been pointed out the need of considering higher performance and low cost. In that way, the modern electronic industry is now demanding for both: novel low-voltage circuits, and novel techniques, as well as low cost fabrication process [1] [2].

An analog multiplier can be designed by using the translinear principle, which is a very good mathematical tool for synthesis processes. Additionally, translinear circuits have inherently low-sensitivity to temperature variations, and furthermore, they are well suited for low-voltage applications. In order to apply the translinear principle to the proposed topology, all MOSTs were biased at saturation levels as stated in [3]. It is also shown in this paper, how the linearity of the proposed design is improved. It is demonstrated by simulating the analog multiplier in HSPICE and by obtaining the FFT.

## 2 The Basic Current - Squaring Circuit Using MOSTs

A basic circuit implementation of an analog multiplier using MOSTs is shown in Fig. 1. Basically, the multiplier is composed of two current-squaring circuits [2][3]. The output current $I_{out}$, can be expressed by equation (1).

$$I_{out} = 2I_B + \frac{I_{in}^2}{8I_B} \tag{1}$$

Equation (1) is valid only when all MOSTs are working in saturation, and having all the same W/L relationships. However, if the MOSTs work in saturation, then the input current will be limited. If $I_{in} = 0$, the drain currents $I_D$ of $M_1$, $M_2$, $M_3$ and $M_4$ will be all the same and

equal to $I_B$. If $I_{in}$ is incremented by either positive or negative levels, then $I_D$ of $M_1$ and $M_3$ remain within a constant value. However, $I_D$ of $M_2$ increases while $I_D$ of $M_4$ decreases, and vice-versa. The highest value of the input-current is reached when either $I_2$ or $I_4$ is equal to zero. As a result, the input-current is limited by the values imposed by equation (2).

$$-4I_B \le I_{in} \le 4I_B \tag{2}$$

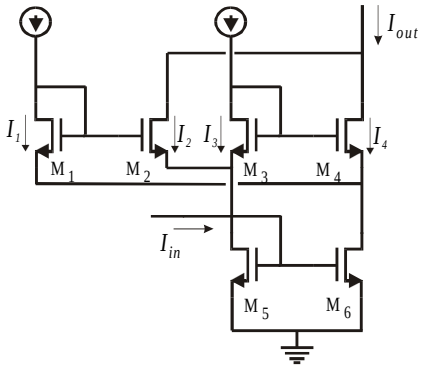


Fig. 1. A translinear current-squaring MOST-based circuit.

## 3 Current-Squaring Circuit Modified for Low-Voltage

The analog multiplier circuit shown in Fig. 1 presents several drawbacks. Among the most important is that the branch that is composed of M3 and M5 limits the minimum supply voltage. Therefore, the minimum supply voltage can be calculated by

$$V_{DD\min} = 2V_{GS} + V_{DSsat} \tag{3}$$

where $V_{GS} = V_T + V_{DSsat}$. If $V_T \approx$ 0.6V, and $V_{DSsat}$=0.2V, then, the minimum is $V_{DD} \geq$ 1.8V.

A modification to the circuit of Fig. 1 can be done by replacing $M_3$-$M_5$ by a low-voltage current mirror as the one shown in Fig. 2 [1]. For this circuit, the input-current is supplied to the source of M3, in order to obtain a low input-impedance, and a low voltage-level at the input. The newer power supply requirements for $V_{DD}$ are

$$V_{DD\min} = V_{GS} + V_{DSsat} \tag{4}$$

in this way: $V_{DD} \geq$ 1V.

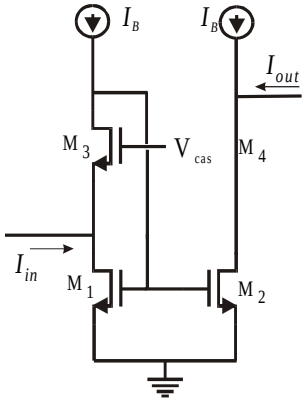


Fig. 2. Low voltage current mirror.

Using this topology, the new analog multiplier satisfies the low-voltage requirements, and it is also suitable for systems requesting massive processing such as: neural networks, and fuzzy logic. The proposed current-squaring circuit suitable for low-voltage applications is shown in Fig. 3. For that circuit, the branch with the higher supply voltage requirements is formed by $M_1$ and $M_6$, thus, the minimum VDD is given by:

$$V_{DD\min} = V_{GS} + 2V_{DSsat} \tag{5}$$

this means that the power supply should be $V_{DD} \geq$ 1.2V.

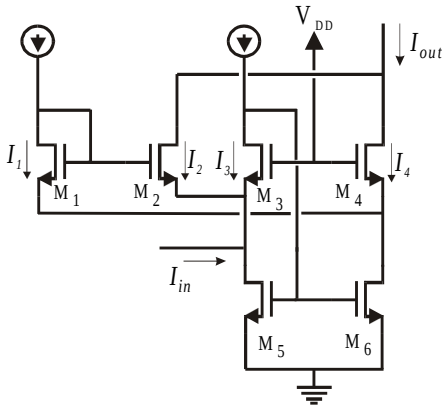


Fig. 3. Low-voltage current-squaring circuit.

## 4 Low-Voltage Four - Quadrants Analog Multiplier

The proposed multiplier is basically implemented with two low-voltage current-squaring circuits, connected as shown in Fig. 4. For that circuit, the output current is measured as the difference of the output-current associated to each squarer circuit; then, the resulting equation for the output current is:

$$I_o = \left(I_x + I_y\right)^2 - \left(I_x - I_y\right)^2 = 4I_xI_y \qquad (6)$$

The W/L relationships of the MOSTs from the multiplier are equal to 56µm/4µm. The circuits was implemented by using the 0.8µm technology parameters from AMS, and considering that:

$$V_{Tn} = 0.6\text{V},\ V_{DSsat} = 0.2\text{V} \qquad (7)$$

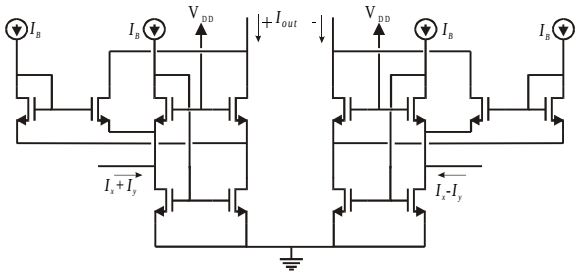


Fig. 4. Low-voltage four-quadrant analog multiplier.

## 5 Simulations Results

Figure 5 shows the frequency response of the low voltage current mirror, which is shown in fig. 2. It can be seen the –3dB frequency is above than 50MHz.

The proposed design was simulated using HSPICE. The results are shown in Fig. 6 and Fig. 7. The DC transfer function is shown in Fig. 6, it can be seen that the multiplier presents a very good linearity within an input current-range between ±10µA. The transitory analysis is shown in Fig. 7. For this simulation the multiplier was connected as modulator, and the frequencies for the input signals were 1MHz and 100kHz.

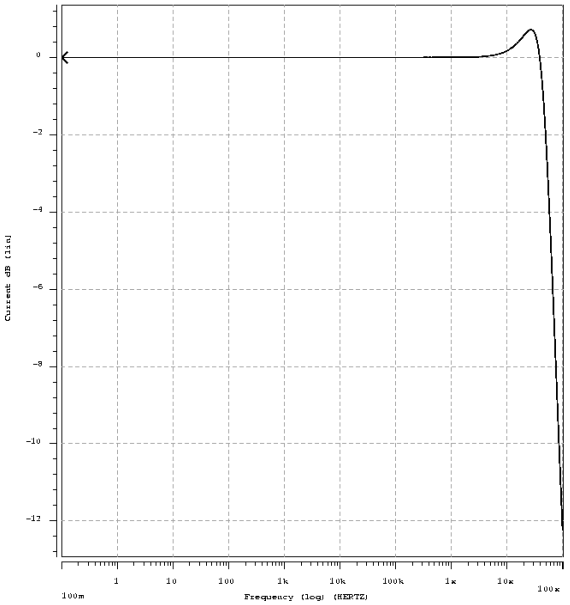


Fig. 5. Frequency response of the current mirror.

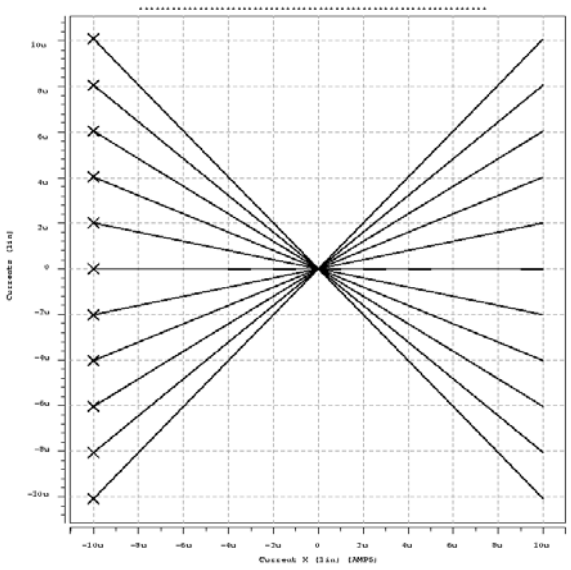

Fig.6. DC transfer function characteristics.

Figure 8, shows the Power Spectral Density (PSD) obtained by the FFT transitory simulation at a frequency of 1megHz. Finally, a resume of the simulated performance, and bias condition are shown in table 1.

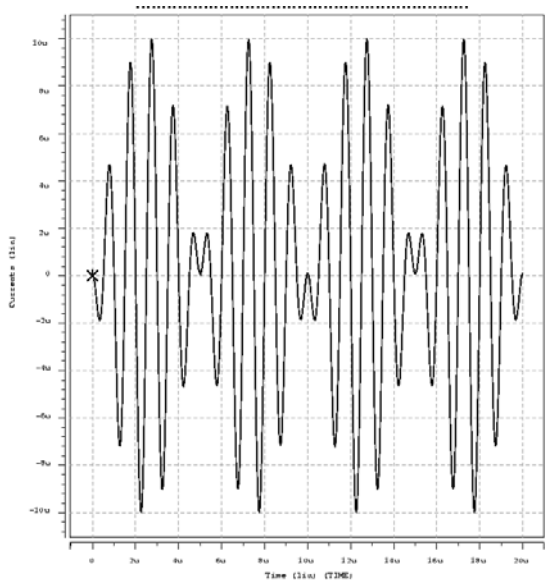

Fig. 7. Transitory analysis using the multiplier as a modulator.

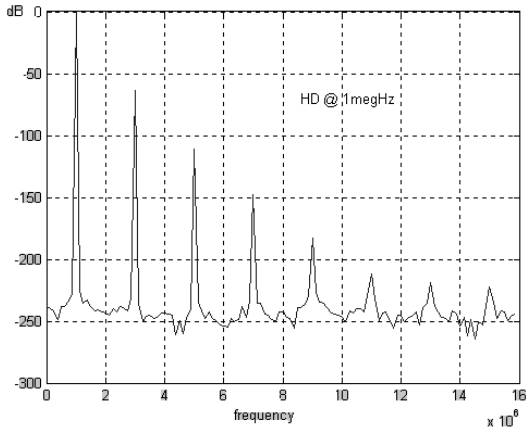


Fig. 8. PSD analysis at 1megHz.

| | |
|---|---|
| Vsupply | 1.2V |
| Input Current Range | ± 10μA |
| THD (at 1 MHz) | -63dB |
| Output Range | ± 10μA |

Table 1. Performance

# 6 Conclusions

The design of a current-mode four-quadrant analog multiplier based on the translinear principle has been presented. The topology is suitable for low-voltage applications, and it was demonstrated by biasing it at 1.2V, however, good performance are obtained operating with 1V. The proposed multiplier was composed of two basic low-voltage current-squaring cells, which results in a simple and compact topology suitable for massive analog processing applications, such as adaptive filtering, neural networks and fuzzy logic. The design was implemented with the 0.8 μm technology parameters of AMS, and simulated with HSPICE.

*Acknowledgements:*

This work was supported by CONACyT project J34573-A.

*References*

[1] R. J. Wiegerink, "A CMOS Analog four-quadrant Current Multiplier". *Proceedings ISCAS*, pp. 2244-2247, 1991.

[2] Shouli Yan and E. Sánchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial", IEICE Trans. Fundamentals, vol. E83-A, No. 2, pp. 179-196, Feb. 2000.

[3] R. J. Wiegerink, *Analysis and Synthesis of MOS Translinear Circuits*, Kluwer Academic Pu.,1993.