Design an X-Band Frequency Synthesizer for Microsatellite Systems

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Abstract— **This paper describe the design of an X-band frequency synthesizer that can be applied to microsatellite transmitter system. We discusse the effects of the phase noise in each component in the circuit (VCO, phase detctor, TCXO, dividers and loop filter) and the reference spurs on the noise performance system. The effect of the carrier recovery PLL in demodulation on the level of the single-sideband (SSB) phase noise is also included in the analysis. In the simulation, we consider the characteristics of commercially available components.**

Index Terms— **PLL, reference spurs, recovery, phase noise.**

I. Introduction

Today's transmitter subsystem in earth imaging microsatellite systems demand higher communication quality, higher data rates to be capable to transmit pictures or data with a quality quite appropriate, higher frequency operation and more channels per unit bandwith. Low power consumption and small size are required for this equipement. All of these constraints combine to make the whole design including component selection and evaluation quite challenging. One portion of this design that is very critical with regard to all of the requirements mentionned above is the synthesized oscillator [1]. This work explores the design of an X-band frequency synthesizer that can be applied to microsatellite transmitter subsystem. The article discusses the design of the phase locked loop (PLL), and the phase noise in each component in the circuit (votage controlled oscillator (VCO), phase detector, temperature componsated crystal oscillator (TCXO), dividers, and loop filter). In the simulation, we include also the reference spurs and their effect on the noise performance of the PLL frequency synthesizer.

An X-band VCO requires a low noise, high frequency prescaler to bring its output frequency into the range of existing PLL for phase locking. Now, frequency multipliers and dividers are available to simplify the design and implementation of X- and Ku-band synthesizers. In the simulation, we consider the characteristics of commercially available components. The high stability crystal reference oscillator is a 10 MHz TCXO from Voltronics, the phase locked loop is a National Semiconductor 2326 component, capable of phase locking a VCO between 500 MHz and 3 GHz. For this reason, to extend the frequency range in the X-band frequencies, a (12 GHz, 1/8) prescaler was used from Hittite.

II. Design and Theory

Figure 1 shows the PLL's linear model with feedback. This PLL is called an integer-N system. This means the VCO frequency and the crystal reference are some integer multiple of the reference frequency.

The PLL consists of a high stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2326, a voltage controlled oscillator, and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, and programmable frequency dividers. The passive filter is desirable for its simplicity, low cost, and low phase noise.

If the input signal to the PLL is

$$r(t) = A \sin\left(\omega_r t + \theta_r\right) \tag{1}$$

and the output signal for the VCO is assumed to be

$$y(t) = B \cos\left(\omega_y t + \theta_y\right) \tag{2}$$

and, if we also assume that $\omega_y=\omega_r$, the output from the phase detector is expressed as

$$e(t) = K_P\left(\theta_r - \frac{\theta_y}{N.P_1}\right) \tag{3}$$

$$= K_P.\theta_e$$

where, θ_r, θ_y and θ_e are respectively, the input phase, output phase and phase error, and K_P is the phase-detector/charge-pump gain factor.

The VCO is assumed to be a linear device whose output frequency varies proportionnaly to the loop filter voltage $V_f(t)$, and is expressed by

$$f_{VCO} = f_0 + K_{VCO}.V_f(t) \tag{4}$$

where f_0 is the free-running frequency, and K_{VCO} is the VCO's gain factor or tunning coefficient expressed in MHz/V. Since phase is the integral of angular velocity, the VCO is modeled as

$$VCO(s) = \frac{K_{VCO}}{s} \tag{5}$$

Figure 2 shows the third order low pass-filter introduced in this model by its transfer function $F(s)$ and described by equation (6) applicable to this system that require the third pole for additional reference suppression.

$$F(s) = \frac{V_f}{e} = \frac{Z(s)\frac{1}{s.C_3}}{Z(s) + R_3 + \frac{1}{s.C_3}} \tag{6}$$

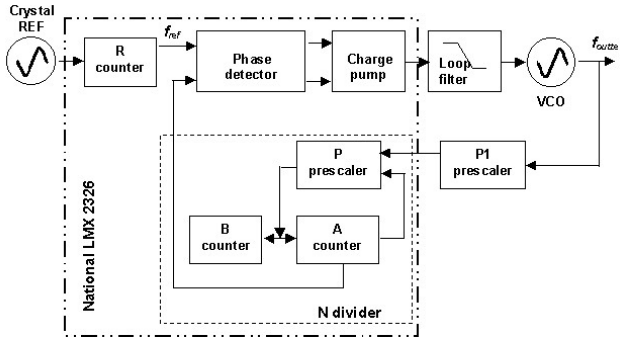

Fig.1 Block diagram of the designed frequency synthesizer

Where *Z(s)* describes the transfer function of the second order loop filter given by

$$Z(s)=\frac{1+s.R_2C_2}{s.(C_1+C_2+s.R_2.C_1.C_2)} \quad (7)$$

Combining these transfer function gives the open-loop gain

$$T(s)=K_P.F(s)K_{VCO}/(N+P).s \quad (8)$$

To achieve optimal circuit performance, the phase noise should be evaluated for proper loop design and it will impact many critical operating characteristics of the synthesized oscillator including adjacent channel power. Phase noise in a PLL can originate from a number of sources. The well know noise sources are specifically crystal reference (TCXO) noise, phase detector noise and VCO phase noise. If the TCXO is used, phase noise data should be obtained from the manufacturer so that reference values can be used with the models. A simple approximation for this noise source due to the crystal reference itself, as with any oscillator, is that is inversely proportional to offset frequency [2].

Higher order approximations are required for more accuracy, but the 1/f approximation is a good starting point for this study.

The VCO noise can be modeled as a simple approximation inversely proportional to offset frequency from the carrier. The noise of the VCO is effectively high-pass filtred by the PLL providing rejection of phase noise or phase error within the bandwidth, but leaving VCO noise well outside of the loop bandwidth unaffected. The VCO noise is given by [3]

$$S_{\theta VCO}(f)=K_{VCO0}+\frac{K_{VCO2}}{f^2}+\frac{K_{VCO3}}{f^3} \quad (9)$$

Where the three coefficients in the VCO noise equation were determined to yield the specific noise at the particular offsets from the carrier.

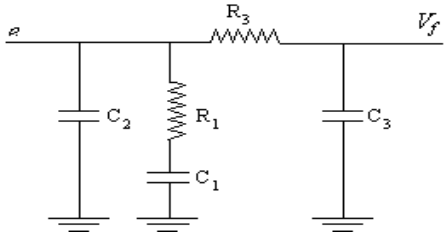

Fig.2 Designed loop filter circuit

The phase detector noise represents the internal noise floor of the phase/frequency detector and frequency dividers within the PLL. For the National Semiconductor synthesizer used in this work, the phase detector noise floor is given for an effective reference frequency of 1 Hz. This noise is shaped by the closed loop transfer function *G(f)* of the synthesizer as [4]

$$S_{\theta pd}(f)=10^{\frac{S_{\theta pdref}+10.\log\left(\frac{fref}{1Hz}\right)}{20}}.G(f) \quad (10)$$

It is well know that the reference sidebands and spurious outputs play a major role in determining the noise properties of the PLL frequency synthesizer. Reference spurs are unwanted noise sidebands that can occur at multiples of the comparison frequency, and can be translated in the transmitter subsystem by the mixer to the desired signal frequency. The power of the reference spur is expressed by [2]

$$SpurGain(F_{spur})=20.\log\left[\frac{K_{VCO}.F(s)K_P}{s}\right] \quad (11)$$

where, F_{spur} will be assumed to be a multiple of the comparison frequency.

Aside from spur gain, the spurs noise are also caused by mismatches and leakages in the charge pump of the PLL. These two factors in the charge pump can cause an ac modulation on the tuning line of the VCO, which can be viewed as FM modulation. This FM modulation gives rise to reference spurs. The spur level is given by [2]

$$Spur=10.\log\left[10^{LeakageSpur/10}+10^{PulseSpur/10}\right] \quad (12)$$

Where the Leakage Spur is the domimant term of reference spurs caused by the leakage effects at lower comparison frequencies, however, the mismatches is the dominant factor at high comparison frequencies.

III. Results and Discussions

For the design described in this work, a matlab program is used to simulate the circuit. In the simulation, we use the characteristics of a National Semiconductor model LMX2326 programmable frequency synthesizer and a VCO with a 50V/MHz sensivity. The VCO used is from General Microwave, which utilizes a high performance transistor operating in the fundamental, rather than the doubling push-push mode. A commercial 10 MHz temperature componsated crystal oscillator from Voltronics with a specified noise of approximately –110 dB/Hz at an offset frequency of 10 KHz is used. The PLL using LMX2326 component, is capable of phase locking a VCO between 500 MHz and 3 GHz. For this reason, to extend the frequency range in the X-band frequencies, a (12 GHz, 1/8) prescaler was used from Hittite. The HMC363 prescaler is a low noise Divide-by-8 Static Divider with InGaP/GaAs heterojunction bipolar transistor (HBT) technology and has a phase noise of -153 dBc/Hz at an offset frequency of 100 KHz, which helps the user maintain good system noise performance. In practice, the PLL can be programmed via a latop computer and parallel port cable. The frequency

changes were done using software provided by National Semiconductor, which the PLL serial-control data are controlled by three inputs (data, LE and clock). For regulating the channel frequency, the serial data input is designed to control the 15 b of the R counter and 18 b of the N counter (which includes 7 b from the A counter and 11 b from the B counter). In our example, we require a frequency range of 8025 to 8175 MHz and a channel spacing of 1 MHz. So, for the reference divider (R counter) equal to 10 (00000000001010)b and the N counter equal to 1010 : (A counter =18 (0010010) and B counter =31 (00000011111)), the output frequency resulting (P_1x(32xB+A)x reference frequency) is equal to 8080 MHz. Figure 3 and Fig. 4 show, respectively, the phase noise plots of each component (VCO, TCXO and phase detector) and the total phase noise with and without the resistor noise sources. We note that the references spurs are not included in the total phase noise. The results show that within the loop bandwidth (10 Hz-10 KHz) of the synthesizer, the level of the reference oscillator is higher because the closed loop transfer function is very large in magnitude and it drops off rapidly when it reaches the loop bandwidth. The results also show that the resistor noise contribution is very small to the synthesizer output (Fig. 4). In the goal to demonstrate that the noise of the VCO is high-pass filtred by the PLL, providing rejection of the phase noise or phase error within the bandwidth. Fig. 5 shows the loop error response. This function is obtained by connexion between the open and the closed loop responses.

In this work, the loop filter design is a very critical part of the PLL synthesizer. In general, a low loop filter cutoff frequency does not supress phase noise at close-in frequencies because the closed loop negative feedback region in narrowed. In adddition, it makes the PLL response slower and the setting time of frequency switching (PLL lockup time) longer and also as result, the PLL spurious is supressed. Conversely, increasing cutoff frequency provides faster PLL response, shorter PLL lockup time, the PLL output signal is frequency-modulated and contains high level spurs.

The output spectrum and the transient response plots are displayed in Fig. 6 and Fig. 7, respectively, for a performed loop filter design where the spurious level, phase noise and frequency transient are evaluated under various conditions.

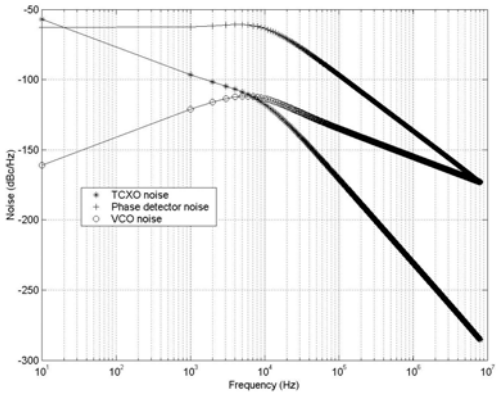

Fig.3 TCXO, hase detector and VCO noises

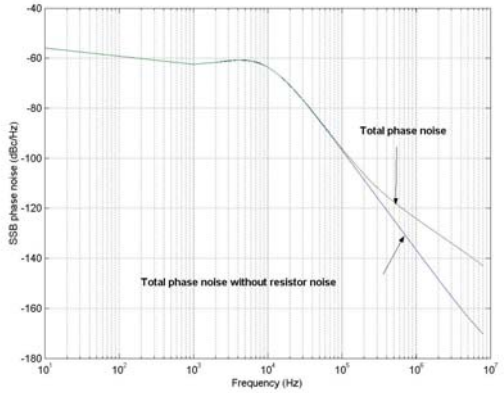

Fig.4 SSB phase noise with and without resistor noise

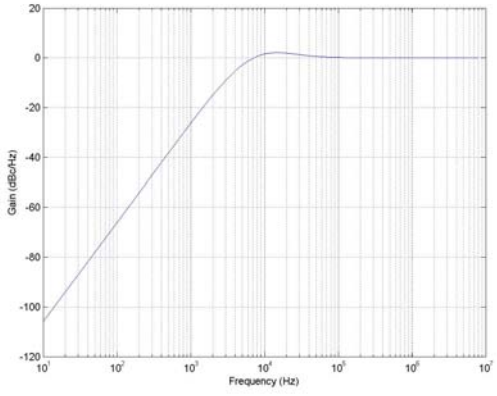

Fig.5 Loop error response

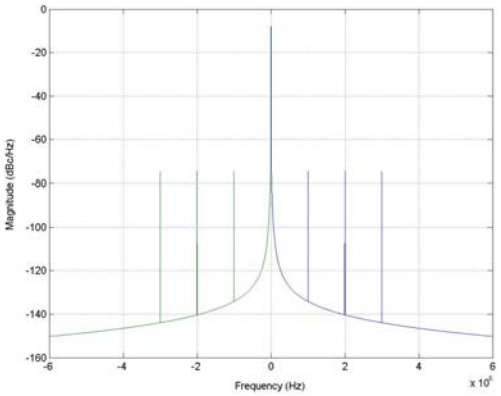

Fig.6 PLL output spectrum

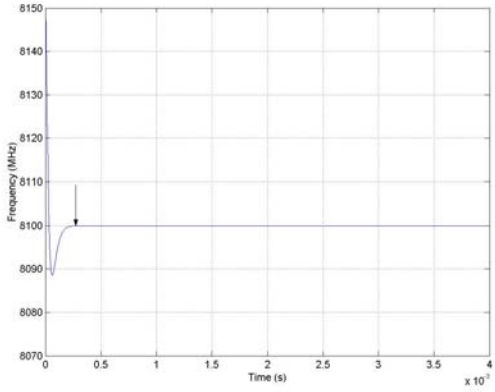

Fig.7 PLL transient response

Figure 8 shows the effect of the carrier recovery PLL in demodulation on the level of the single-sideband (SSB) phase noise and demonstrates the phase noise rejection properties of the carrier recovery PLL. The carrier recovery PLL supresses the 100 degree deviation at 100 Hz down to a level that eliminates crossings of the decision bondaries. Integration of this curve on both sides of the carrier results in an rms phase noise of 0.01 radian, and a margin of signal-to-noise ration (S/N) of 17 dB.

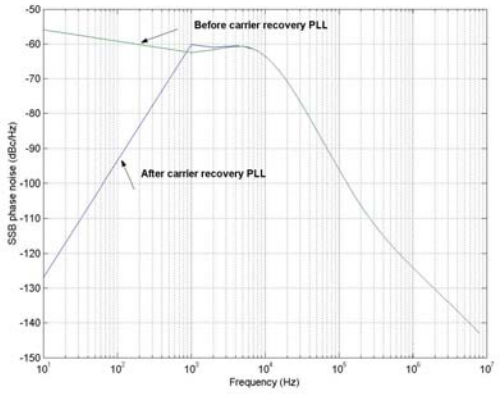

Fig.8 Noise before and after carrier recovery in demodulation

IV. Conclusion

A simple design of an X-band frequency synthesizer that can be applied to microsatellite transmitter systems has been presented. This paper has discussed the phase noise in different sources of the PLL and their effects on the noise performance system. The results indicate that for a frequency range of 8025 to 8175 MHz and with a carrier recovery of 0,6 KHz, the PLL gives an rms of 0,01 radian and a signal-to-noise ratio of 17 dB.

V. References

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