Image Generation in Microprocessor-based System with Simultaneous Video Memory Read/Write Access

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Abstract: In this paper we present a new architecture of video memory data handling in microprocessor-based systems. This architecture is a solution for the real time image processing systems which requires a significant recording time. The solution is based on a simultaneous video memory read/write. This operation is ensured by hardware splits of video memory in separate capacities and by association of a selecting circuit. This later offers a state port and two communication ports. The first communication port is used for reading and the second for writing.

Key words: Video image generation, simultaneous video memory read/write, software/hardware System, microprocessor-based systems.

1 Introduction

The video image generation in microprocessor-based systems is ensured by the video card or the graphic card. A video card is composed of several function units working in coordination. The starting point of any image is always from the video RAM. This latter is a memory RAM that is on the video card and contains the image information to be displayed.

To generate a video image on the basis of a video RAM, the different components of the video card should complete the reading of its entire memory with a frequency being able to reach 75 cycles per second [1] figure 1. During this reading process, no simultaneous access is authorized. This gives the possibility of a writing process only during the time of the return line and frame. Under these operating conditions, the realization of a display device for real time image processing systems, which requires a significant recording time, remains very complicated.

In this paper, we present a hardware/software solution [2] to enlarge the recording access time. This solution consists in designing a display system which allows a simultaneous reading/writing access.

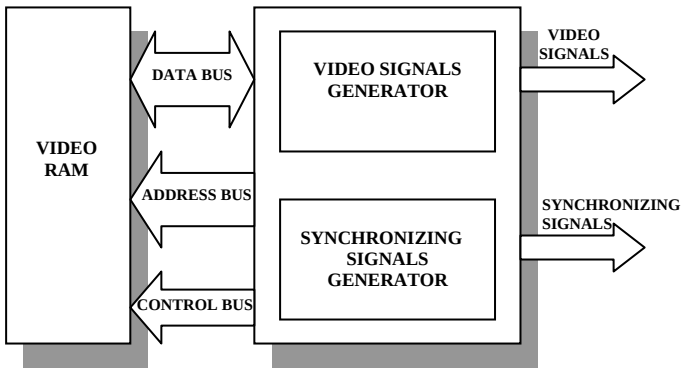

Figure 1. Graphic card block diagram

The suggested architecture is composed of a hardware part and a software part. The hardware part is based on the memory capacity part of the video RAM with separate buses and on the association of a simultaneous selecting circuit. The software part ensures the data transfer to the display system and the recording synchronization with the video RAM reading cycle.

2 Image generation in the video card

The image, which represents the video card output signals, is the result of repeated readings of the video RAM with a Digital-to-Analog conversion (DAC) [3] of the enabled data. The maximum time for the writing on this RAM during the frame is given by the following relation.

$$T_w = T_{fr} + T_{lr} \times N_l \qquad (1)$$

$\boldsymbol{T_{Fr}}$: The time of return frame.
$\boldsymbol{T_{Lr}}$: The time of return line
$\boldsymbol{N_L}$: The number of lines within the frame

The ratio of the writing time over the total time of the video frame generally varies from 10% to 15% and can be written in the following form:

$$W_r = \frac{(T_{fr} + T_{lr} \times N_l)}{T_f} \qquad (2)$$

$\boldsymbol{T_F}$: The total time of the frame.

3 Image generation with simultaneous access by two levels

The image generation system with simultaneous access by two levels represents the basic architecture of our system. This architecture of visualization uses a video RAM made up of two RAMs. Both RAMs can be selected separately; one can be selected in reading and the second in writing and vice versa. Figure 2 represents the block diagram of the hardware part of this system.

The hardware part of our system is composed of four units: Interface Unit, Selection Unit, Reading Unit and Digital-to-Analog Conversion (DAC) Unit. The Interface Unit can use two types of addressing: the Extended Physical Addressing [4] or the Fast Physical Addressing [5]. The Selection Unit is connected to all the units and the video RAM. The Connection to the interface is made up of a state bus, a control bus, an address bus and a data bus. The link to the reading unit is made up of a control bus and an address bus. The connection to the conversion unit is ensured by a one-way data bus which transfers the selection unit data to the conversion unit.

In this architecture of simultaneous access, the ratio of the writing time over the total time of the video frame varies from 100% to a minimal value $\boldsymbol{W_{r2}}$. The ratio $\boldsymbol{W_{r2}}$ is given by the following relation.

$$W_{r2} = \frac{1}{2} + \frac{W_r}{2} \qquad (3)$$

By using the relation (2), the expression of $\boldsymbol{W_{r2}}$ could be written in the following form:

$$W_{r2} = \frac{1}{2} + \frac{(T_{fr} + T_{lr} \times N_l)}{2T_f} \qquad (4)$$

Using the values of $\boldsymbol{W_R}$ of section 2, the ratio $\boldsymbol{W_{r2}}$ varies from 55% to 57,5%.

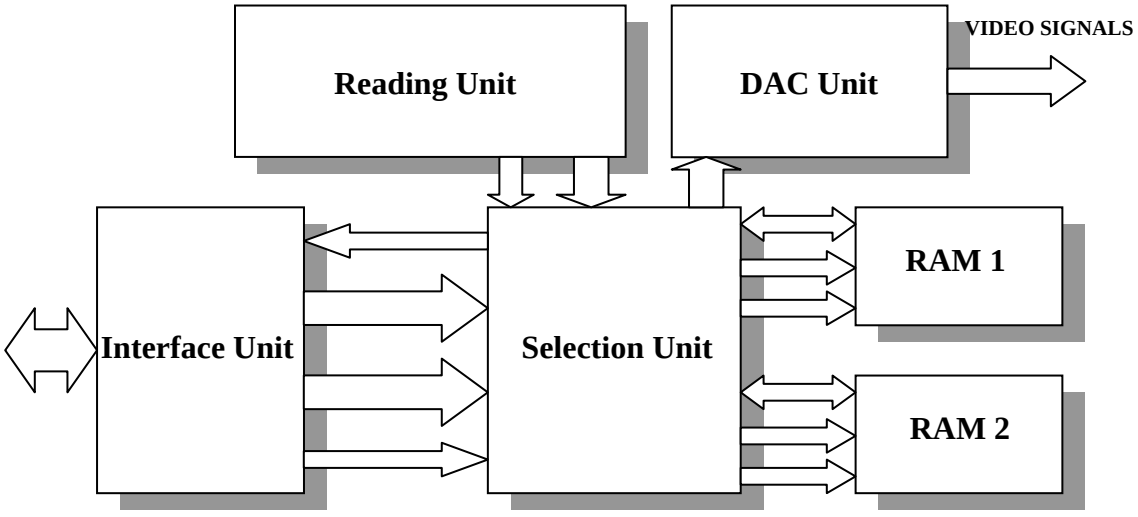

Fig 2. Two levels system block diagram

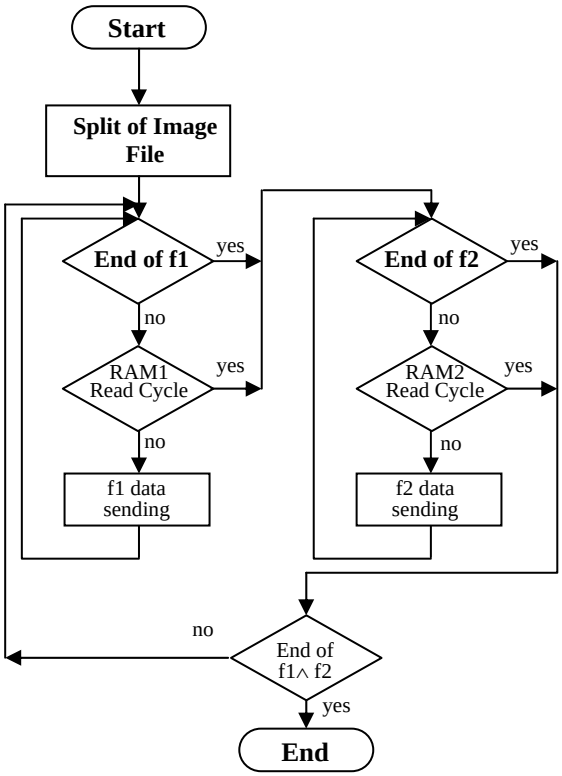

Fig 3. Two levels system flow chart

The software part is designed to carry out a process of permanent recording on the video RAM of this architecture. In the case of a simultaneous access by two levels, the image file is split up into two parts: f1 and f2. File f1 represents the higher part of the image and file f2 the lower part. The software allows the switching between sending data of file f1 and file f2. The synchronization of sending data is related to the selection state of RAMs in our system. Figure 3 illustrates the main flow chart of the software part.

4 Image generation with simultaneous access by several levels

The principle of the image generation with simultaneous access by several levels is similar to the principle of construction in two levels. In this structure of visualization, our system uses a video RAM made up of several RAMs. The figure represents the block diagram of the hardware part of this system. This is made up of four units: Interface Unit, Selection Unit, Reading Unit and Digital-to-Analog Conversion (DAC) Unit.

The connection between the units uses the same structure of the two levels system. The size of the state bus depends on the number of the used RAMs. The link between the selection unit and the used RAMs is ensured by several buses: each bus is composed of a data bus, an address bus and a control bus.

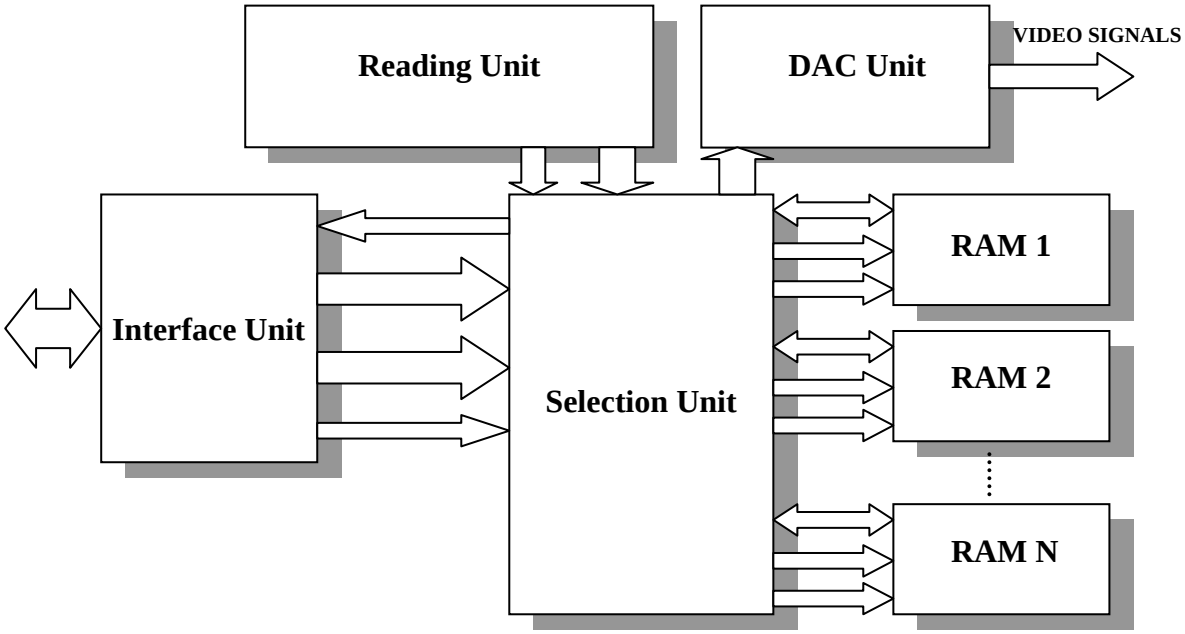

Fig 4. N levels system block diagram

This architecture gives a ratio of the writing time over the total time of the video frame varies from 100% to a minimal value W_{RN}. The ratio W_{RN} is given by the following form:

$$W_{rN} = (1 - \frac{1}{N}) + \frac{W_r}{N} \qquad (5)$$

N: Represent the number of the RAMs used in our system.

By using the relation (2), the expression of W_{RN} is written in the following form:

$$W_{rN} = (1 - \frac{1}{N}) + \frac{(T_{fr} + T_{lr} \times N_l)}{T_f \times N} \qquad (6)$$

By using the formula (6) and a value of W_R equals to 10%, W_{RN} can take several values according to N. Table 1 presents the values W_{RN} for N varies from 1 to 100.

The software part of the simultaneous access by several levels splits up the image file into several parts. The result gives N files (f1, f2, f3....., F_N). The switching of sending data is done by N files. The synchronization of the sending of data is related to the state of selection of the N RAMs, which compose the video RAM of our system. Figure 5 presents the principal flow chart of the software part of the system at several levels.

Table 1: W_{RN} values

N	1	2	3	4	5	6	7	8	9
$\mathbf{W_{RN}}$	10%	55%	70%	77,5%	82%	85%	87,1%	88,75%	90%
N	20	30	40	50	60	70	80	90	100
$\mathbf{W_{RN}}$	95,5%	97%	97,75%	98,2%	98,5%	98,7%	98,87%	99%	99,1%

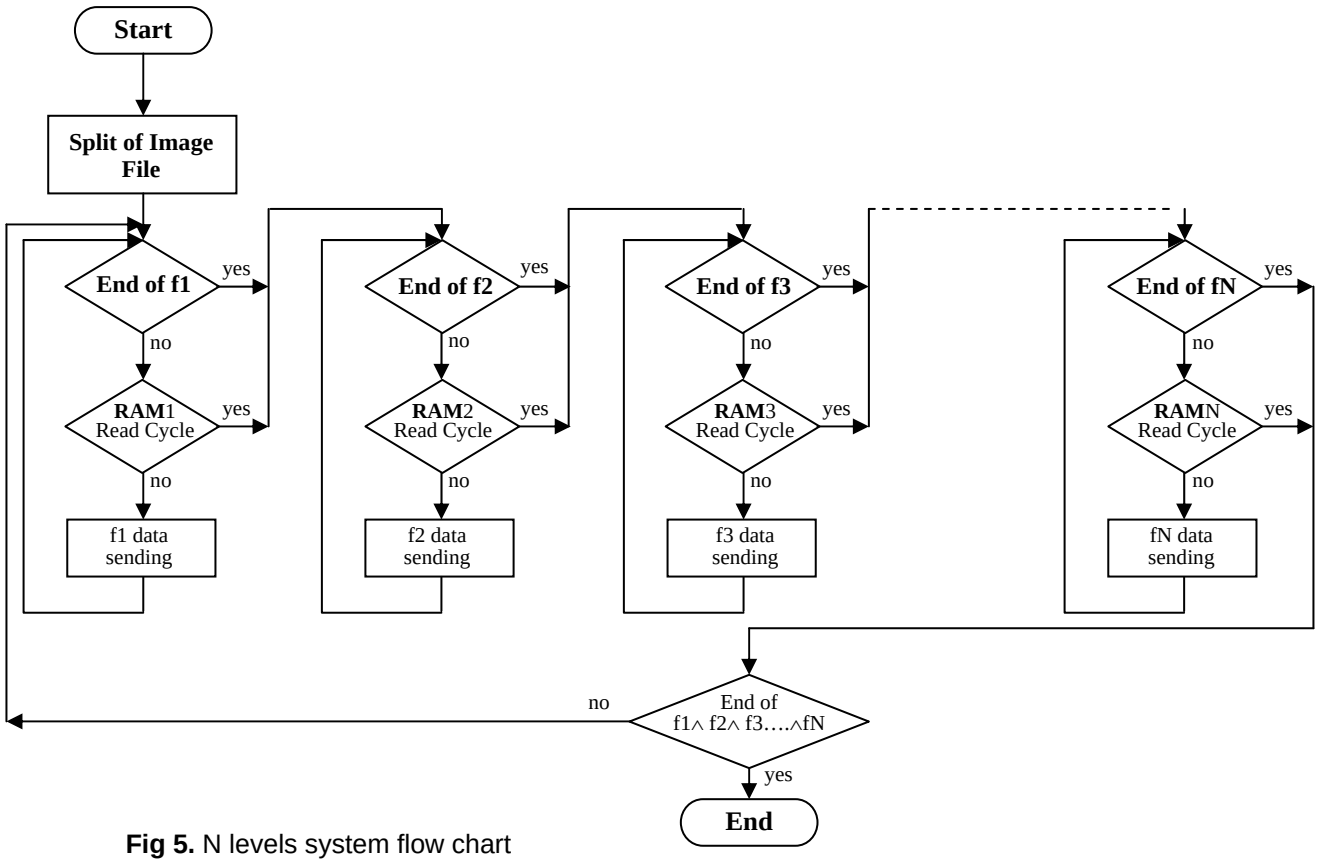

Fig 5. N levels system flow chart

5 Conclusion

The generation of the images in the video cards connected to the microprocessor-based systems uses repeated readings of the video memory contents. In this paper, we have exposed the main principles of the simultaneous access. We have presented the structure at two levels and then the structure at several levels.

The first practical tests have given a recording rate of 95% for the two levels system and a rate of 98% for the three levels system. Structures higher than three levels have given rates lower than that of three and two levels. This characteristic is due to the complexity of the circuitry and the software processing time that is significant for the several levels systems.

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