Design and Simulation of a 4 GHz Folded-Cascode CMOS LC Quadrature VCO for RF Image-Reject Transceivers

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Abstract:- This paper describes a novel low phase-noise CMOS folded-cascode QVCO (quadrature voltage controlled oscillator) design using the TSMC 0.18μm 5M1P CMOS process technology. The startup behavior of the proposed QVCO indicate that, the QVCO is free of bi-modal oscillation (frequency ambiguity). The VCO operated at 4GHz with a tuning range of 3.7 to 4.2 GHz. The QVCO consumed around 4mA from a 1.8V supply. Phase noise simulations indicate a phase noise of –160dBc/Hz at an offset of 600KHz form the carrier (@4GHz) which is favorable compared to recent QVCO designs.

Key-words: - Quadrature VCO, phase noise, CMOS, folded cascode, negative resistance.

1 Introduction

Image-reject transceivers used in today's advanced radio architectures require accurate quadrature RF Voltage Controlled Oscillator (VCO) signals. A quadrature LC VCO is an ideal candidate for such application due to their inherently low phase-noise behavior. The combination of a direct connection and a cross connection between two LC VCOs forces the two VCOs to oscillate in quadrature. Following the basic quadrature VCO design by Rofougaran *et. al* [2], in recent literature, several new quadrature VCO (QVCO) structures has been reported. These efforts include augmentation of telescopic-*like* cascode structures to the basic differential VCO structure[5][9]. In this work we report another novel modification of the QVCO structure where a PMOS folded cascoding structure is used for providing the mutual input excitations(couplings) for quadrature generation. In addition to the phase noise reduction effect of cascoding [9], the inherent low-noise behavior of the PMOS device (lower hot carrier induced drain current noise [1]) in this proposed cascoding structure would further reduce the phase noise contributions introduced by the coupling device. Also, in this novel structure, a grounded center-tapped inductor is used for the LC tank of the VCO, instead of, the supply-center tapped inductor VCO structures in most QVCO structures [2][5][9]. This provides the advantages of reduced power supply noise which can greatly effect the linearity of cohabiting data-converters in a mixed signal VLSI chip. In addition, this topology has the advantage of reduced leakage currents into the standard p-substrate (also connected to ground). The capacitance of the LC tank is provided with PMOS depletion-mode varactor devices.

2 Novel QVCO Topology

Fig. 1(a) shows the circuit diagram of our proposed QVCO topology. Two LC-tank VCOs are provided with a direct & a cross connection forcing the two VCO's to oscillate in quadrature. In order to achieve bi-modal oscillation-free[2][5] quadrature oscillations, the core positive feedback NMOS latch transistors & the PMOS coupling transistors are connected in folded-cascode structure, so that the current flowing into the LC tank is only the drain current of the PMOS coupling device. The bias voltages Vbias1 & Vbias2 are such that PMOS triode regime loads & the NMOS triode regime tail provide low resistance path to the supply rails. The source node of the cascoding PMOS coupling device being shielded [7] from the drain output of the VCO is then held at almost the VDD rail. Now let phasors $\vec{I}$ and $\vec{Q}$ be respectively the steady-state outputs of the I-VCO & the Q-VCO with the reference polarities as shown in Fig. 1(a). Then, the phasor currents into the LC tanks of the I-VCO and the Q-VCO can be approximated to be respectively $g_m\vec{Q}$ and $g_m\vec{I}$, with g_m being the large signal transconductance (triode regime transconductance) of the coupling PMOSFETs. For quadrature operation it is well-known that $\vec{Q} = \pm j\vec{I}$ [2][5]. As a result the steady-state LC resonator impedance (LC tank + the negative resistance

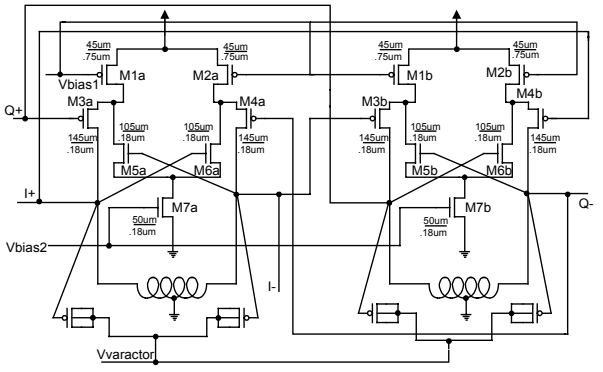
latch) = $\frac{1}{\pm jg_m}$. In an LC resonator with a low quality factor (**Q**) lossy inductor (& assuming achievable high **Q** tank capacitor), this is only possible at one frequency, given by:

$$\omega \approx \frac{R}{L}\sqrt{(\frac{1}{|G_M| * R}) - 1} \qquad (1)$$

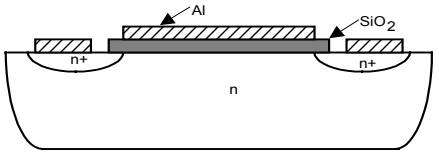
where R is the series resistance of the lossy inductor & $|G_M|$ is the absolute value of the average negative resistance of the cross-coupled latch devices. This is the frequency at which the negative of the equivalent parallel conductance of the LC tank is equal to the average negative resistance $-|G_M|$ generated by the cross-coupled devices across the cascode outputs. It is to be noted that with large signal operation the cross-coupled NMOS devices & the PMOS cascode coupling devices are turned "OFF" for a part of the period [7] & sustained oscillations take place only at a frequency for which the average negative resistance is equal to the negative parallel resistance of the tank. Hence there is expected to be no bimodal oscillation in this circuit. ***Non-linearity & Phase noise considerations:*** The large-signal operation of the oscillator drives the latch & the coupling devices into slewing mode during part of the period in each cycle, this event generally results in harmonic distortion ("spurs") in the oscillator output spectrum. Substrate noise due to digital switching in mixed-signal IC's also results in harmonic distortion[3] of the VCO output. On the other hand, the primary source of phase noise (short-term random oscillator frequency fluctutations) is the thermal noise of the series resistance of the lossy inductor and the drain current noise. Use of cascoding[9] in conjunction with PMOS coupling in this topology considerably reduces the effect of the drain current noise on the overall phase noise, leaving the thermal noise of tank resistance as the main source of phase noise. The phase noise spectral density can be represented by[8]:

$$\overline{v_n^2} = 4kTR_p(\frac{\omega_o}{2Q\Delta\omega})^2 \qquad (2)$$

where, Rp is the parallel equivalent tank resistance, ω_o is the center frequency of the oscillator & $\Delta\omega$ is the displacement from center frequency. Fig. 2 shows a simple modified model of the LC quadrature VCO following the model in [4].



(a)



(b)

Figure 1. (a) Proposed folded-cascode CMOS Quadrature VCO with grounded center-tapped inductors, (b) Depetion mode PMOS varactor cross-section .

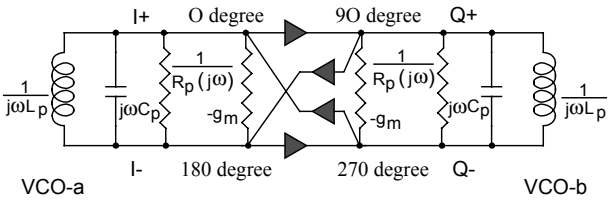
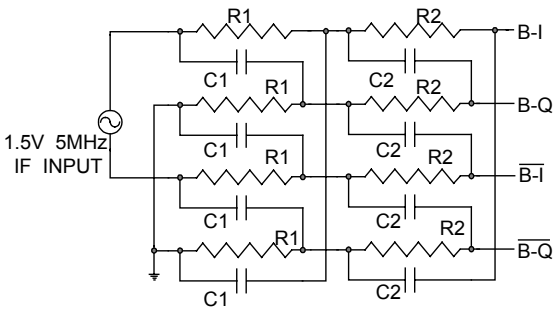
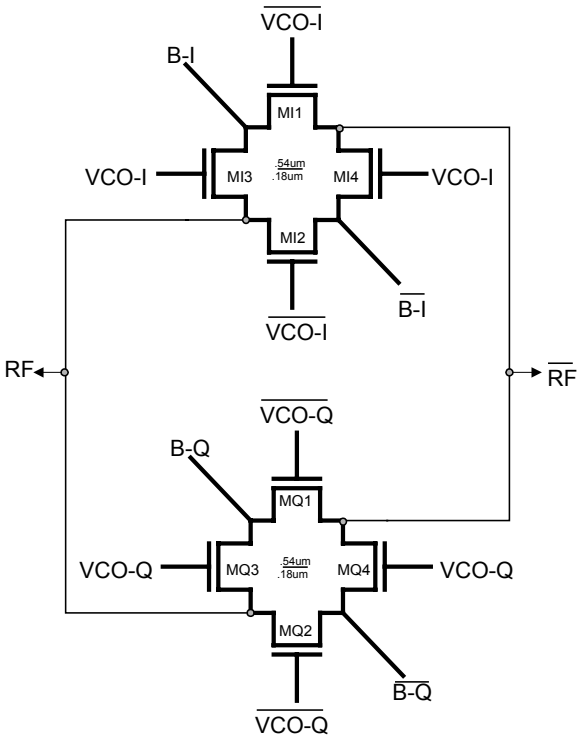


Figure 2. Simple model of LC Quadrature VCO.



(a)



(b)

Figure 3. (a) RC polyphase network for Baseband Quadrature generation, (b) Passive Quadrature Image reject mixer for up-conversion.

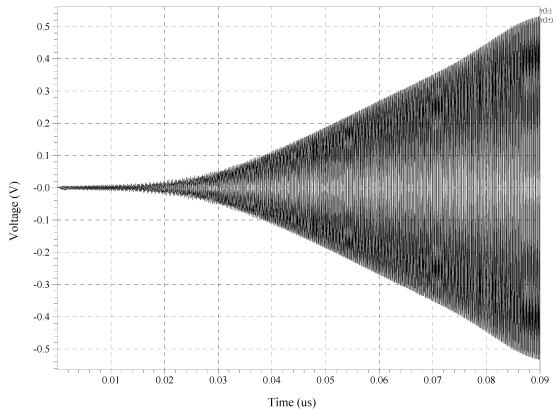


Figure 4. Start-up behavior of the proposed VCO.

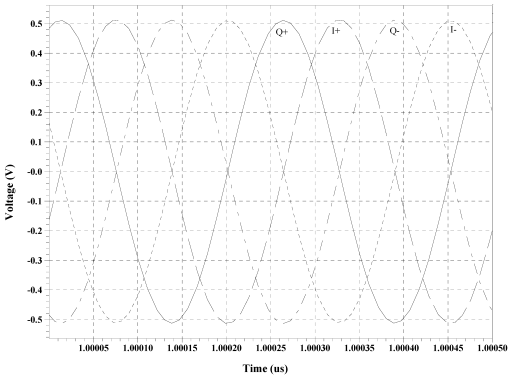


Figure 5. Transient response of the proposed QVCO showing the 4-φ Quadrature Sinusoids at 4GHz.

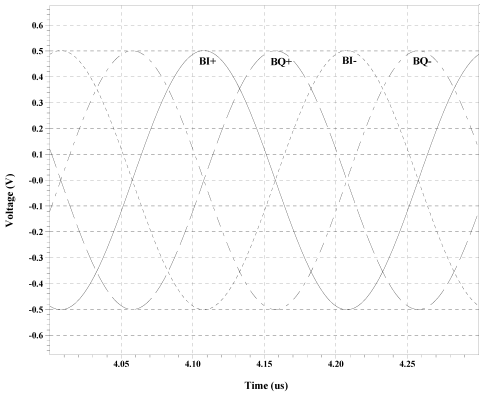


Figure 6. Quadrature Baseband signals (@5MHz).

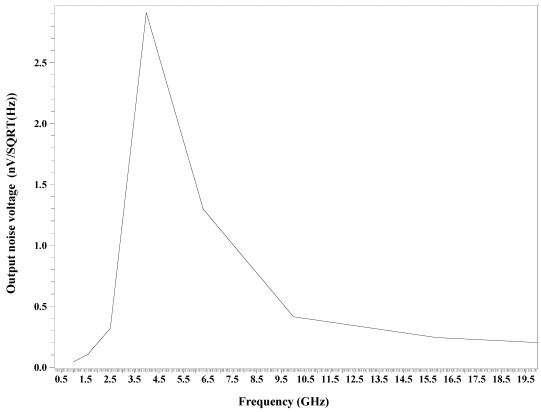


Figure 7. The magnitude of the output noise voltage spectral density function (centered @ 4GHz).

3 Simulation Results

SPICE simulations (using Tanner T-SPICE v.7.0) were conducted on the proposed folded cascode quadrature VCO (FCQVCO) using the TSMC 0.18μm 5M1P CMOS process technology. Operation of an image reject mixer architecture using the proposed FCQVCO was also verified through simulations. Fig. 3(a) shows an RC polyphase network[6] for Baseband Quadrature generation, while, Fig. 3 (b) shows a passive Quadrature Image reject mixer bridge circuit for up-conversion. Fig. 4 shows the transient start-up behavior of the four FCQVCO outputs (Q+, Q-, I+ & I-) which ramps up from zero to maximum monotonically (doesnot bounce up & down during the kick off period). Hence in accordance with [5] this start-up behavior verifies that this topology is free of bimodal oscillations & any resulting frequency ambiguity. Fig. 5 displays the four phases of the *sinusoidal* transient responses of the proposed FCQVCO at 4GHz. By varying the tank capacitance (PMOS depletion-mode varactors) a wide enough fractional tuning range of ≈ 11% (3.75GHz to 4.2GHz) was achieved which compares favorably to other recent QVCO structures[2][9]. Fig. 6. displays the Quadrature baseband signals (BI+, BQ+, BI- & BQ-) generated by the RC polyphase network.

In order to estimate the phase noise of the FCQVCO, inductors with moderate on-chip Q ≈ 5 was assumed. Considering an input referred noise source across the LC tank (due to the thermal resistance of the coil resistance & the input referred drain current noise), the output noise voltage spectral density was determined from T-SPICE simulations. The magnitude of the output noise voltage spectral density function (centered @ 4GHz) is shown in Fig. 7 clearly indicating noise-shaping by the band-pass behavior of the LC tank. Based on the above, phase noise computations with respect to the 4GHz carrier, indicate a phase noise of –160dBc/Hz at an offset of 600KHz form the carrier which is favorable compared to other recent QVCO designs[9]. The FCQVCO exhibited low power dissipation requirements consuming around 4mA from a 1.8V supply voltage, which makes it suitable for wireless radio applications.

4 Conclusion

A novel FCQVCO design has been described and the SPICE simulation results has been reported. The proposed FCQVCO is found to provide frequency ambiguity free oscillations, in addition to good phase noise characteristics & low-power dissipation. This FCVCO design thus compares favorably to other recently reported QVCO designs developed for RF image-reject transceiver applications.

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