Chaos Generator via SCR Relaxation Oscillator

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Abstract: An *SCR* (Silicon Controlled Rectifier) relaxation oscillator was used to produce chaos via Hysteresis Feedback. Evaluating the facts that a chaotic system presents random like motions with high sensibility to initial conditions and there exits a strange attractor, we showed, numerically with PSPICE, that our design present these facts concluding that our system is chaotic.

Keywords: Chaotic Oscillator, Silicon Controlled Rectifier.

I. Introduction:

Recently new designs of chaos generators have been reported (see [1], [2], and [4]-[12]). In [5] the authors presented a novel chaos generator via Hysteresis feedback, which was used in [1] to produce a new Hysteresis chaotic circuit. In [12] a chaotic generator was shown using the Wien-Bridge oscillator.

Motivated by the fact that an oscillator with Hysteresis feedback can produce chaos ([1], [5], [7]), we could design a new chaotic circuit using the *SCR* relaxation oscillator shown in [3]. Numerical experiments with *PSPICE* are shown to prove chaotic behavior of our design using the events that a chaotic system presents random like motions with high sensibility to initial conditions and there exits a strange attractor.

II. Chaotic Oscillator Design

The general representation of a nonlinear oscillator with Hysteresis feedback is depicted in Fig. 1

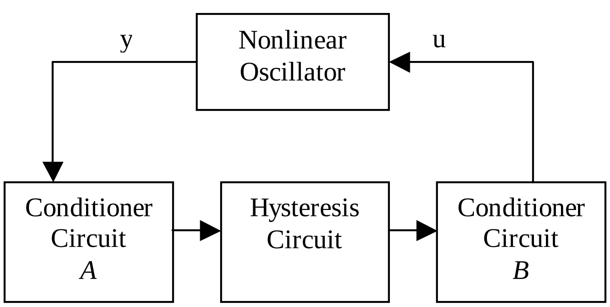

Fig. 1 Nonlinear oscillator with Hysteresis feedback.

From the electronics point of view, the nonlinear oscillator is armed with capacitors and inductors; in this way, the output *"y"* could be a voltage on a capacitor and the input "*u*" could be a current injected to an inductor. In our design, the conditioner circuit *A* is a buffer and the conditioner circuit *B* is a voltage to current converter. The nonlinear oscillator used is show in Fig. 2 and it was adapted from the one designed on [3].

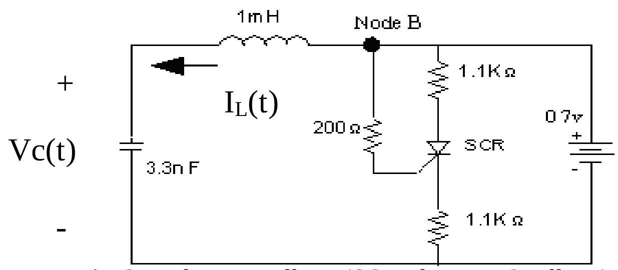

Fig. 2 Nonlinear oscillator (*SCR* relaxation Oscillator).

The conditioner circuit *A* utilized is shown in Fig. 3, which is a buffer follow by offset elimination circuit. The input to the buffer is the capacitor voltage $V_C(t)$.

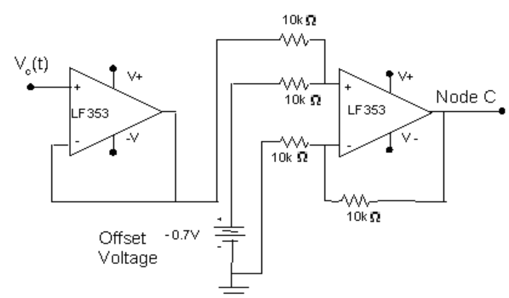

Fig. 3 Conditioner Circuit *A* (*V+=15V, V-=-15V*)

The Hysteresis circuit developed is shown in Fig. 4.

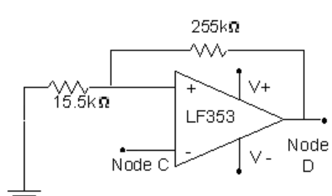

Fig. 4 Hysteresis Circuit (*V+=13V, V-=-13V*)

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Finally, the conditioner circuit *B* armed is illustrated in Fig. 5

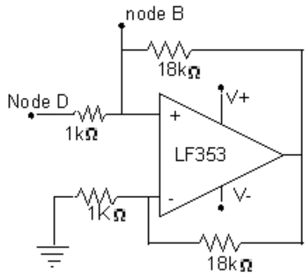

Fig. 5 Conditioner circuit *B* (Voltage to current converter circuit) (*V+=15V, V-=-15V*).

III. Numerical experiments

The whole system shown in Fig. 1 was implemented with *PSPICE*. The *SCR* employed was taken from the library of *PSPICE* with component number *2N5061*. Simulation results for $I_L(0)=0.1\ mA$ and $V_c(0)=0.5V$ are shown in Figures 6, 7 and 8.

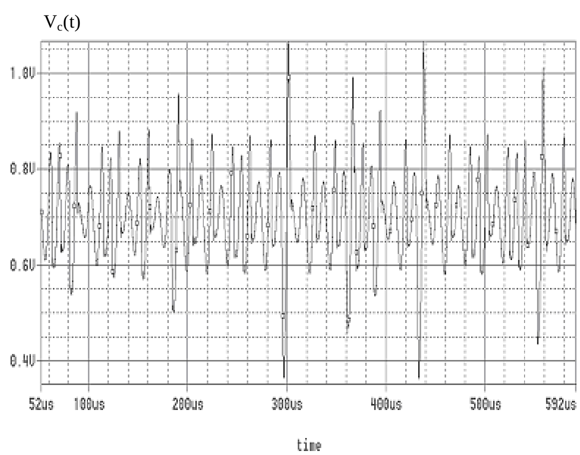

Fig. 6 Capacitor's voltage.

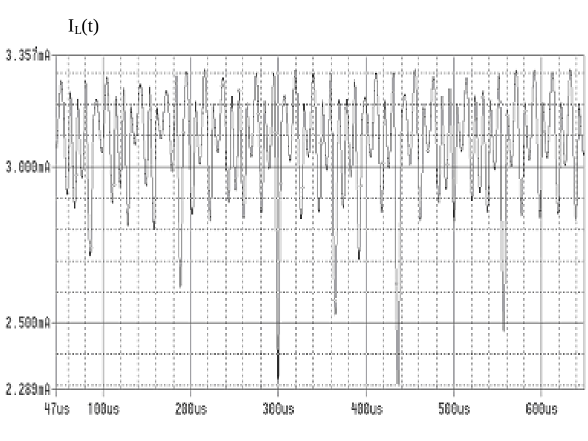

Fig. 7 Inductor's current.

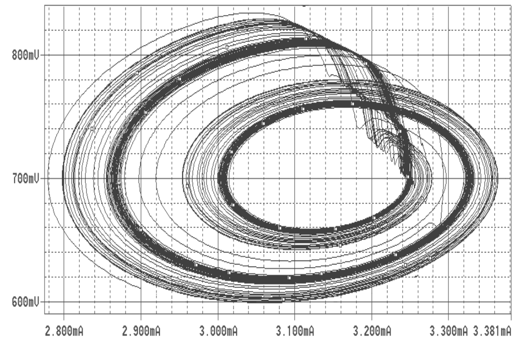

Fig. 8 Phase diagram (capacitor's voltage versus inductor 's current)

Also, we changed slightly the initial conditions in our experiments and we could realized that our design presents high sensitivity to initial conditions; that is, the evolution in time are stronger different in spite of the almost the same initial conditions.

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