Multiphase DC-to-AC 1kW Solar Power Inverter

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Abstract: - In case of low voltage (12 to 24V) solar and battery powered sinus inverter applications a special converter topology for managing the high input current rating is required. Conventional solutions uses paralleled power MOSFETs to realize high current (several 100A) switches. In this paper a synchronized multi phase PWM concept was chosen to rise the over all efficiency of the inverter. In general, both, the DC-to-DC converter and the mains coupled DC-to-AC inverter can be realized as multi phase stages. In our case only the DC-to-DC converter is realized as a multiphase system. In this paper a 12V DC (input) to 230V AC (output) / 1kW transformer coupled solar inverter is proposed. The development of the inverter is described, realization hints are given and the efficiency of the complete inverter is compared to the conventional solution.

Key-Words: - sinus inverter, multiphase, PWM, solar inverter

1 Introduction

Switching mode PWM converters have high efficiency and are used when high output power has to be maintained (e.g. solar and renewable energy applications, etc.), but also in the industrial field of applications. Driving stages for high dynamic actuators and motor drives up to several kilowatts are another field of application. The starting point of our investigations was a project for a solar inverter with the goal of very high efficiency, operating at the 230V / 50Hz AC power grid with an input voltage range from 11V to 14V DC. In this paper a new concept is shown which increases the input and output signal quality to meet high signal quality and reduced EMC problematic.

The main drawback of conventional wide input range, low voltage PWM-sinus-inverters (cf. Fig. 1) is the high amplitude of the current at the lowest required input voltage which leads to an expensive and large design. In the field of solar applications normally an additional external battery is used as a storage element to minimize the 100Hz current ripple at the input of the solar cells leading to a smaller C_{IN}. The advantage of modern high power Elkos (e.g. UltraCaps) will help to overcome this problem in the future. Also, harmonics in the output waveform due to the limited switching frequency of the inverter leads to the requirement of a complex EMC-filter. A high weight of the 50Hz power transformer for voltage level adaptation is not a real problem of fix installed equipment. Modern transformers (e.g. .toroid cores) can reach very high efficiency while producing low losses. Also the costfactor compared to ferrite-components is very moderate. When using an inverter topology similar to Fig. 1 three possible solutions are given:

(a) A high switching frequency in the partial stage, synchronized operation (paralleled design). In this case the filter can be minimized. Drawback in this case are the rising switching losses, which depend on the operating frequency.
(b) A high order input and output filter is used and so the switching frequency (as well as the switching losses) can be reduced. This leads to big inverter volume and weight.
(c) A multi phase PWM structure can be used. In this

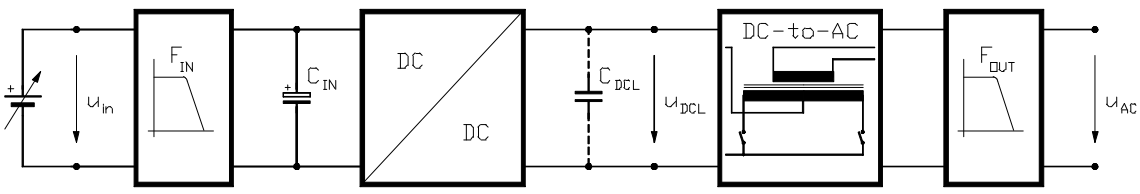

Figure 1: Principle DC-to AC inverter with voltage DC-link

case the effective ripple frequency of the in- and output waveforms is the product of the switching frequency with the number of the output stages. The result is an inverter with reduced current stress in the input capacitor and a reduced filter in the output stage. Due to the shared output current moreover the efficiency is increased significantly.

The solar plant voltage has to be adapted to match the requirements of the input voltage of the DC-to-AC power inverter. In most cases an isolation barrier between the solar cells and the power grid is required, which is realized by the mains transformer, here. A major problem is the amount of the input capacitor, which is connected in parallel to the solar cells. Due to the 100Hz (120Hz) ripple in the output power of a single phase inverter a big input capacitor is required. In solar applications normally batteries are used to handle the current ripple. The problem of the rising dynamic source resistance at higher frequencies can be overcome by using modern high power capacitors (e.g. UltraCaps). The remaining switching ripple is reduced due to the multiphase concept. So the lifetime of the capacitors is further increased.

2 Multi Phase PWM Inverter

To overcome the main drawback of conventional solutions, the very high current in the step-down stages of DC-to-AC inverters at low input voltage ratings, current sharing by parallel connection of the power switches (in general MOSFETs) is used (e.g. S_1 & S_2 in Fig. 2 consist of several discrete power MOSFETs). This solution cannot remove the high current amplitudes in the output inductors and filtering capacitors. An improvement can be achieved by paralleling the whole output stage (switches, inductors and filter capacitors). In such solutions normally synchronized PWM generators (without phase delay) are used. The current sharing has to be controlled by each inverter. Also the problem of the high input current ripple cannot be eliminated when the switching of the power stages occurs simultaneously. A further significant improvement can be implemented by using constant phase delay in between the PWM signal generators of each power stage (c.f. Fig. 3). This leads to a significant reduction of the input and output current ripple of the multiphase stage and therefore to corresponding little input and output filters due to the resulting high frequency of the ripple parameters.

2.1 Converter Overview

In the case of MOSFET power switches, the over all losses of the multiphase inverter topology are reduced significantly. In solar inverter applications especially the partial load efficiency is of major interest. One solution is to reduce dynamically the amount of switching output stages depending on the load current. The result is a significant improvement of the inverter efficiency in the partial load case compared to conventional PWM inverter topologies.

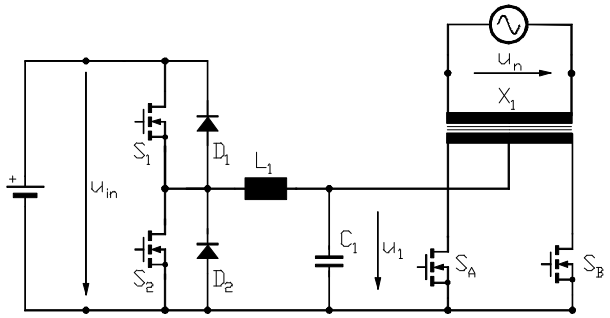

Fig.2. Conventional DC to AC inverter (consisting of variable DC-to-DC and DC-to-AC switch, center tapped transformer topology)

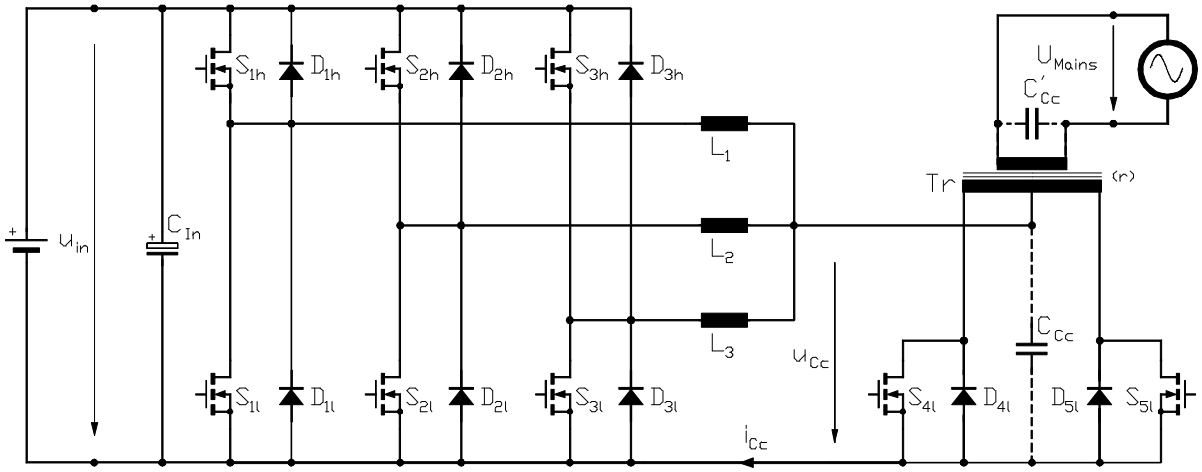

Fig.3. DC to AC inverter with Multiphase step down stages

The new topology (c.f. Fig. 3) is derived from the standard inverter topology (Fig. 2). No additional power switches are required compared to the solution shown in Fig. 2, where the switches S_1 and S_2 consist of three FETs connected in parallel. The splitted output inductor leads to a design, which is more easy to handle.

The topology, depicted in Fig. 3 can be operated in two different modes:

(A) synchronized PWM with no phase delay between the switching stages (conventional mode of operation)
(B) synchronized PWM with constant phase delay between the switching stages, depending on the number of active power pathes

The new topology uses the phase delay PWM mode (b). Each stage is controlled as a current mode converter with 1/3 of the required load current.
Two possible operating modes can be distinguished:

I.Power grid connected inverter

Here, the inverter has to be controlled in a way to produce sinusoidal mains current. The absolute value of mains current can be sensed as i_{Cc}. In this mode of operation no link capacitor (C_{Cc}) is required. Here the two switches S_{4l} and S_{5l} are controlled by the mains voltage polarity. Thus, the circuit can only run at the unity power factor of 1.

II.Local grid inverter (single inverter system or stand alone operation)

To run the inverter as a voltage source a link capacitor (C_{Cc}) is required. Alternatively, the capacitor can be connected in parallel to the mains, using the transformer ratio to achieve a higher value of the capacitor ($r=n_2/n_1$, $C'_{Cc}=r^2*C_{Mc}$). In this mode of operation (depending to the control algorithm) also a power factor not equal to 1 is possible. The pulsating energy has to be stored in the input capacitor C_{In} leading to a huge value (or an external battery). The disadvantage in this case is the increased input current ripple of the solar panels.

In general, the design is especially well suited for unity power factor (0.95 to 1). Only some special circumstances makes sense to use such topologies with a powerfactor outside of this range.

2.2 Efficiency Estimation

To estimate the system behavior a model is built. A conventional Inverter, as depicted in Fig. 2 and a multiphase concept are compared. The conventional system uses three power MOSFETs connected in parallel to reach the power goal of 1kW
Power switch characterization: $R_{DS,ON,100°C.}$=10mΩ, $C_{OSS,Typ.}$=40nF
The modulation ratio d of the converter is controlled to produce sinusoidal output current

$$i_{TR}(t) = i_{L1}(t) = I_{PK} \cdot \cos(w \cdot t) \quad [1]$$

The turn on losses are rated to

$$P_{ON} = I_{(L1)}{}^2 \cdot R_{DS,ON,100°C} \cdot d \quad [2],$$

the switching losses can be represented by

$$P_{SW} \propto 2 \cdot C_{OSS} \cdot \frac{du_o}{dt} \cdot f_{SW} \quad [3],$$

with the switching frequency f_{SW}.

For estimation, the diode-losses are included in an increased C_{OSS}.
The basic converter is designed to deliver an output power of 1kW, driven from a 12V source. Based on an over all efficiency about 90% the power stage has to handle about 1100W at 12V.
Due to the requested input voltage range, the primary voltage of the mains transformer is set to $7.5V_{RMS}$, leading to an input current $I_{IN,RMS}$ of about 150A. The peak current I_{PK} reaches 210A. Due to the low speed dynamic in the current (10ms sinusoidal current) this has to be taken into consideration when components are selected.
When using the conventional (C) system the losses in the power stage lead to

$$P_{ON,C} = I_{(TR)}{}^2 \cdot \frac{R_{DS,ON,100°C}}{3} \cdot d \quad [4]$$

$$P_{SW,C} \propto 2 \cdot 3 \cdot C_{OSS} \cdot \frac{du_o}{dt} \cdot f_{SW} \quad [5]$$

In the multiphase (M) system the output current ITR is three times the current of each power stage. thus, in the same power range I_{L1} decreases to 33%.

$$P_{ON,M} = 3 \cdot \left(\frac{I_{(TR)}}{3} \right)^2 \cdot R_{DS,ON,100°C} \cdot d = \frac{I_{(TR)}}{3} \cdot R_{DS,ON,100°C} \cdot d \quad [6]$$

$$P_{SW,M} \propto 2 \cdot 3 \cdot C_{OSS} \cdot \frac{du_o}{dt} \cdot f_{SW} \quad [7]$$

The switching losses remain unchanged in this first order estimation. As can be seen, the multiphase concept reduces the switching losses to 33% (when using the same components) compared to the conventional system. In case of high current applications this can lead to a drastic improvement of the efficiency. The 1kW sample design derived here operates at 16kHz. The simulated and the measured results are compared in Table 1 (in the model the magnetic losses are neglected, the ohmic losses are added to the switching stage).

2.3 Alternative Aspects

A further improvement can be achieved by using two multiphase stages in conjunction with a center tapped transformer as depicted in Fig. 4. Here only one active switching element is in the main current path leading to drastically reduced conduction losses. Furthermore with rising output current amplitude mostly the current drops through the high-side switches S_{Xh}, leading to a further improvement. The low-side switches S_{1l}, S_{2l}, S_{3l} respectively S_{4l}, S_{5l}, S_{6l} are switched with mains frequency only. If U_{Ma} is positive (leading to a negative U_{Mb}), S_{1l}, S_{2l} and S_{3l} have to be turned on, if U_{Mb} is positive, S_{4l}, S_{5l} and S_{6l} have to be turned on.(In general, it is also possible to use only one switch on each low side.) The upper switches are controlled with a PWM pulse pattern to generate a sinusoidal output voltage U_{Mains}. The main advantage of this application is the improved efficiency in low voltage operation.

In case of an 1kW 12V solar inverter the efficiency can be increased by about 2% compared to a inverter type depicted in Fig. 3. The disadvantage of the high amount of active switches is the main drawback of this concept. Modern power electronic MOSFETs (small devices with high current ratings in low voltage applications) can help such designs to became ready for market.

3 Realization

A principal concept of switching ripple minimization depicted in Fig. 3 was analyzed in detail and a laboratory prototype was breadboarded. The sample inverter was designed for a solar application operating at 12V DC-input (11-14C) and 230V / 50Hz AC-output. Here, only the DC-to-DC converters a point of interest. The transformer based DC-to-AC inverter is very simple and will not be derived in detail.

The output power stages are build up with cheap mass product semiconductors and low cost fix-inductors. Paralleling of the small and rather simple stages lead to a high power inverter with excellent efficiency compared to conventional PWM solutions.

The PWM generator was implemented in a small FPGA (1800 gates equivalent), which is controlled by a simple microcontroller (PIC16C876). The inverter was controlled for a stand alone application, also operation in main connection is possible.

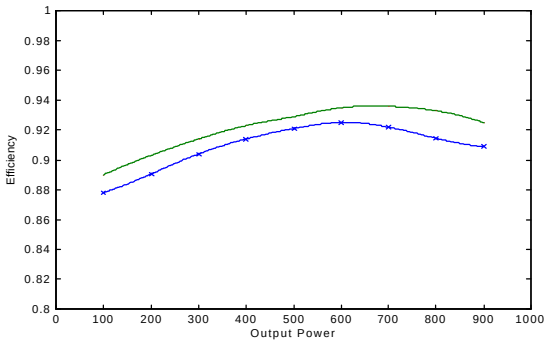

Figure 5: Efficiency comparison: conventional inverter (dashed), multiphase inverter (solid)

The schematic of the prototype is shown in Fig. 3. The mains transformer is realized by a 1kW toroid with four primary tracks operating in parallel (so each switch S_{4l} and S_{5l} consist of four power MOSFETs.).

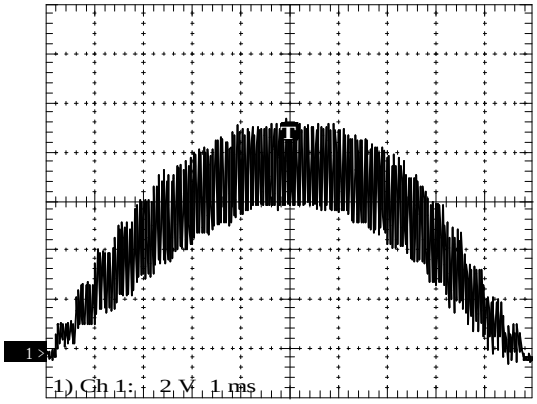

Fig. 6. Output voltage U_{Cc} of the multiphase stage (local grid operation, C_{Cc}=0, C_{Mc}=1uF)

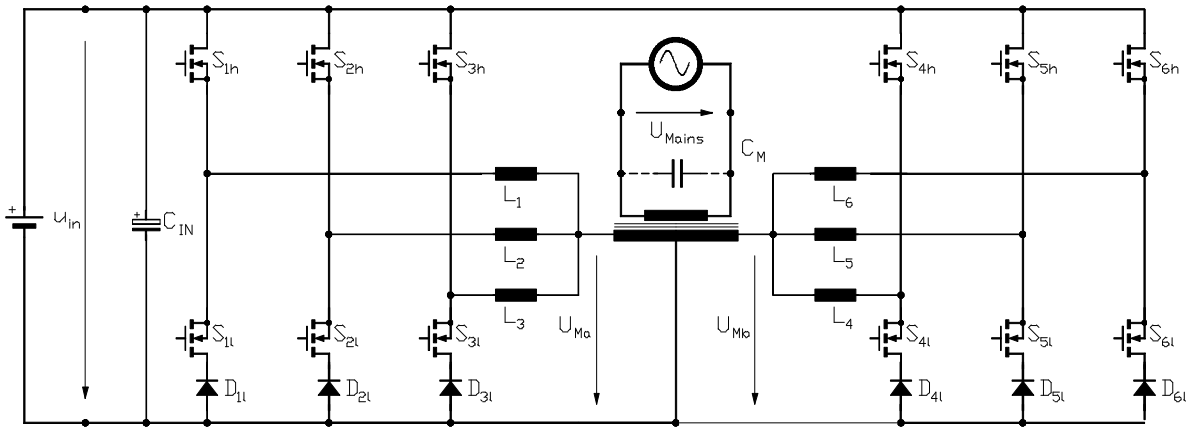

Fig.4. alternative improved DC to AC inverter with two multiphase step down stages

The current measurement is realized with a hall-element. In Fig. 6 the output voltage of the DV-to-DC stage is shown. The converter operates one 500W halogen lamp.

The depicted switching ripple in the output waveform results from the mains transformer. When using the transformer equivalent circuitry (c.f. Fig. 7) it can be seen, that in between the filter capacitor on the secondary (mains side) and the summation junction of the power stages (primary side) the leakage inductors are placed, leading to the depicted waveform. To minimize this behavior an additional capacitor can be placed on the primary side (C_{Cc}) if required.

During the test phase a slightly modified topology was also derived. Here, the primary of the mains transformer also was split into three windings. Due to the core material and its high frequency behavior the switching ripple unfortunately lead in this solution to increased losses in the transformer. But in general this principle can be used to optimize the control of the mains transformer. The multiple current pathes lead to a more effective design and to higher efficiency.

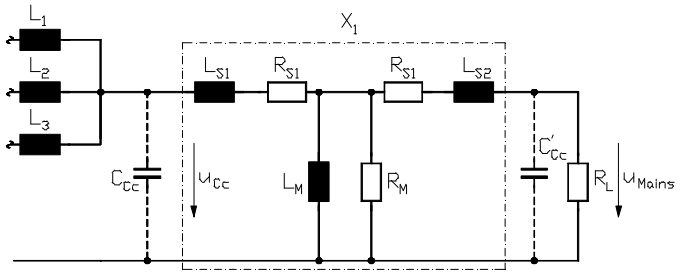

Figure 6: output stage equivalent circuitry

4 Conclusion

The new solution improves the disadvantage of parallel operation of electronic switches in the power stages in conventional converter topologies. The power stage consists of three PWM halve-bridges operating in parallel. Each stage switching at 16kHz with a phase delay of 120° to the previous. The maximum peak current of each output stage of the 12V / 1kW inverter is less than 70A. So very cheap mass products in easy to handle TO247 packages can be used as power switches. Due to the reduced current in each of the stages the efficiency is increased significantly. Because of the improved efficiency e.g. battery lifetime can be increased without any quality reduction. The ripple of the input and output current is shared between the different stages and the amount of input and output capacitors is reduced. The only required energy reservoir is due to the power ripple in the single phase mains. The frequency of the resulting input and output current ripples rises with the number of active stages. This results to a more silent (EMV) design. The inverter presented in this paper is a simple and effective solution for high power low voltage applications. The concept is well suited for wind-, solar- and renewable energy as well as for aerospace applications.

The simple control principle of the multiphase step-down stage can easily be implemented in a simple microcontroller with custom logic support for the pulse pattern generator. In case of a power factor equal to one a maximum power point tracking system can easily be implemented by monitoring the system signals (u_{Cc} and i_{Cc}). The main drawback of the topology is the series connection of two power switches in the main current path. The resulting conduction losses can be reduced by a factor of about 2 when using a modified topology as depicted in Fig. 4. Here a symmetric concept is used. This topology can lead to a further improvement of the inverter efficiency.

As a future aspects the topology can be modified to eliminate the 50Hz mains transformer. The voltage level adaptation can be realized in a multiphase system at switching frequency. So the transformer weight and volume can be reduced. In such a concept the energy storage can also be moved from the low-level input voltage to the 400V DC-link leading to a drastically reduction of the required capacitor (the stored energy is proportional to the voltage squared!).

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