

Analysis and Characterization of GaAs Integrated Digital Circuits

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Abstract: Different GaAs logic families are analyzed and characterized in order to compare their performance. The analysis is performed adopting both depletion and enhancement devices. The study is carried out considering the inverter gate with a fan-out equal to one. The characterization is performed adopting the PSPICE simulator. The analysis shows that the performance of each devices depends on the components dimensions, too. Moreover the study confirms that the depletion devices have higher power consumption than the enhancement ones.

Key-words: logic family, inverter gate, fan-out, logic swing, power loss, propagation delay, rise time, fall time

1 Introduction

In recent years, high speed Integrated Digital Circuits are extensively used in telecommunications and signal processing fields (CPU, memory, etc.). In the environment of the Integrated Circuits (ICs), the market share of the GaAs devices is limited if it is compared to the Silicon one. The less entry in the IC market depends particularly on the high cost of each device due to the higher cost both of the material and of the fabrication process.

Due to the high operating frequency, GaAs IC represent a good choice as compared to Silicon technology. The high performance of the GaAs ICs depends on the electrical property of the material. In fact, the high electron mobility and resistivity makes it suitable to be used in circuits working at higher speed [1] [2].

The MESFET and the HEMT transistors are the basic components for the GaAs logic. Adopting HBT, complementary circuits can be realized which act up to 10 GHz [3]. For the ECL logic and the I²L gate array, HBTs are used. The GaAs HBT circuits have performance better than that of BJTs and Si HBTs, reaching speed of about 100 GHz [4].

In this paper, different GaAs logic families are analyzed and characterized adopting the PSPICE simulator. The comparison among the different logic gates has been performed evaluating some relevant parameters such as logic swing, power loss, propagation delay, rise (t_r) and fall time (t_f), operating frequency.

In section 2, the most know GaAs logic families are briefly presented and the inverter circuit schematics are shown.

In section 3 the results obtained using PSPICE simulator will be presented.

In the last section some conclusions are drawn.

2 GaAs logic families

Modern GaAs logic families use both depletion and enhancement devices.

2.1 Depletion logic

Logical gates adopting depletion transistors have high power consumption and are composed of a relevant number of components per gate. Therefore, the obtainable speed is reduced.

2.1.1 Buffered FET Logic (BFL)

The BFL logic uses depletion components only. In Fig.1 the BFL inverter is shown. The output stage is a source follower to supply enough driving current to the load gates. Due to the presence of a buffer stage and of two DC power supplies, the power consumption is very high.

The inverter gate diagram is easily modified in order to realize more complex gates, connecting in series (in parallel) the driver transistors and in parallel (in series) the pull-up transistors.

2.1.2 Schottky Diode FET Logic (SDFL)

Unlike the BFL logic, in the SDFL GaAs Schottky diodes are placed at the input stage for level shifting purposes (Fig.2). As the diodes current is low, both the diodes area and the power dissipation are reduced. The diodes D_{L1} and D_{L2}

level shift the input voltage in order to provide an output voltage range similar to the input. The output NMESFET B_o provides for the logic inversion, B_L acting as an active pull-up and B_D as an active pull-down.

2.2 Enhancement logic

Logical gates adopting enhancement transistors are quite like NMOS gates and need one supply voltage. Therefore, they have lower power consumption than the depletion logic to the detriment of the logic swing.

2.2.1 Direct Coupled NMESFET Logic (DCFL)

Due to its simpler circuitry and fewer components, the DCFL is the most used logic. In Fig.3, the DCFL inverter is reported. The load device is an enhancement-depletion NMESFET while the output transistor is an enhancement-only NMESFET. Enhancement-only NMESFETs offer great promise as active devices. When NMESFET is used as active device, direct coupled logic gate can be designed without level shifting diodes, requiring only one power supply.

2.2.2 Buffered Direct Coupled FET Logic (BDCFL)

The BDCFL logic is obtained adding to the DCFL logic an output buffer stage (Fig.4) The buffer stage improves the noise margins and makes the propagation delay less dependent on the fan-out and on the capacitive loads.

2.3 Low consumption logic

In the development of multimedia telecommunication systems, having low power consumption and high clock frequency, the use of very low power consumption logic families becomes mandatory. The reduction of power dissipation makes the GaAs IC's able for VLSI implementations. To this aim, the Pseudo Complementary FET logics (PCFL) and the Two – Phase Dynamic FET logic (TDFL) have been developed.

The PCFL logic uses enhancement transistors; the decrease in power consumption is obtained by increasing the area occupancy [5]. In Fig.5, the PCFL inverter is shown.

The TDFL is a dynamic logic having only one supply and two different clocks. Power consumption occurs during the clock switching only. In Fig.6, the cascading of two inverters is shown. The logical levels of the TDFL are

compatible with those of the DCFL and the SBFL families [6].

3 Analysis and simulations

The PSPICE simulator is used to analyze the effects of several parameters on the performance of different GaAs logic families [7]. Inverter gates having fan-out equal to one are considered. The unit fan-out condition is obtained by cascading the inverter gate either with another equal inverter or with a capacitor. For the simulation, $0.5\mu\text{m}$ gate length MESFETs having a doping concentration equal to $2 \times 10^{17} \text{ cm}^{-3}$, are used.

3.1 BFL inverter

To evaluate the performance of the inverter, $\sqrt{3} \text{ V}$ DC power supply is chosen. In Fig.7 the obtained input-output characteristic is shown.

The transient analysis gives the following values: rise-time $t_r=400\text{ps}$, fall-time $t_f=330\text{ps}$, the propagation delays for the high-low transition $t_{pHL}=227\text{ps}$ and for low-high transition $t_{pLH}=117\text{ps}$ (Fig.8). The average delay is 172ps and the power consumption is 1.2mW for each gate. The highest operating frequency results about 290 MHz . Therefore the power-delay product (PD) is about equal to 0.20pJ .

3.2 SDFL inverter

Adopting transistors with low value of the transconductance parameter β (β about equal to 100nA/V^2) the simulation shows that the input-output inverter characteristic is different from the typical one. In fact for low input voltage, the transistor B_L is not able to charge the first stage output capacity and the output voltage remains consequently at a negative value. Changing the transistors dimensions ($W_{BD}=1\mu\text{m}$, $W_{BL}=2\mu\text{m}$, $W_{BO}=20\mu\text{m}$ where W is the gate width), the power consumption for each inverter is 1.04mW and the logic swing is about 2.6V . The transient analysis gives the following values: $t_r=863\text{ps}$, $t_f=300\text{ps}$, $t_{pHL}=67\text{ps}$, $t_{pLH}=419\text{ps}$ (Fig.9). Moreover, the average delay time is 243ps and the cycle frequency is 205 MHz . From the simulation results $\text{PD}=0.25\text{pJ}$.

3.3 DCFL inverter

Simulation results show that transistors having low β values produce little logic swings, due to the high V_{OL} value. To obtain suitable β values, the

thickness of the epitaxial layer is chosen equal to 0.1 μ m. Adopting a depletion transistor having $W=5\mu$ m, the obtained β , C_{GD} and C_{GS} values are 980 μ A/V² and 5fF respectively.

The power consumption is 297 μ W for each inverter and the logic swing is about 2.6V. The transient analysis gives the following values: $t_f=1.05$ ns, $t_r=560$ ps, $t_{pHL}=107$ ps, $t_{pLH}=590$ ps. Moreover, the average delay time is about 348ps and the cycle frequency is 143 MHz (Fig.10). Simulations show that to obtain t_{pHL} comparable with t_{pLH} , the load transistor dimensions have to increase to the detriment of V_{OL} .

The analysis shows $PD=0.1$ pJ.

3.4 BDCFL inverter

To obtain lower delay time, the dimensions of the B_L transistor are greater than the DCFL inverter while the B_o transistor has the same dimensions. The buffer stage makes this choice possible. The obtained power consumption is about 1 mW for each inverter and the logic swing is about 794mV. The transient analysis gives the following values: $t_f=512$ ps, $t_r=473$ ps, $t_{pHL}=194$ ps, $t_{pLH}=90$ ps. Moreover, the average delay time is about 148ps so that the cycle frequency is 352 MHz (Fig.11) and the product $PD=0.15$ pJ.

3.4 PCFL and TDFL inverters

Due to the conduction of transistors during the change of the input values only, simulation results show the reduced value of the power dissipation for the PCFL logic; in fact the obtained power consumption is about 83nW for each inverter. The transient analysis gives the following values: $t_f=824$ ps, $t_r=507$ ps, $t_{pHL}=342$ ps, $t_{pLH}=188$ ps. Moreover, the average delay time is about 265ps and the cycle frequency is 188 MHz (Fig.12).

The TDFL is a dynamic logic therefore has a minimum operating frequency depending to the leakage currents. The devices dimensioning is performed minimizing the charge distribution during the clock transitions. 2 μ m width pass-transistors and 4 μ m width for the other devices have been chosen. 1V DC supply and 500 MHz clock frequency have been used during the simulation. This shows that the inverter acts correctly during the charge distribution, also. In fact, the output voltage of the first inverter is about 0.6V which is considered high level for the second inverter (Fig.13). The energy dissipation per gate is about 5nW, $t_r=150$ ps and $t_f=185$ ps.

4 Conclusion

In this paper, different GaAs logic families are analyzed adopting the PSPICE simulator. The DC and the transient analysis are carried out to evaluate the performance of each logic family. Inverter gates with unitary fan-out are considered as elementary gate. In fact more complex devices can be realized cascading a number of elementary gates suitably.

The analysis shows that the performance of each device depends on the component dimensions, too. Moreover the study confirms that the depletion devices have higher power consumption than the enhancement ones.

So, when low power consumption is mandatory, PCFL or TDFL logic are to be used while when high cycle frequency is needed, enhancement logics families represent the best choice.

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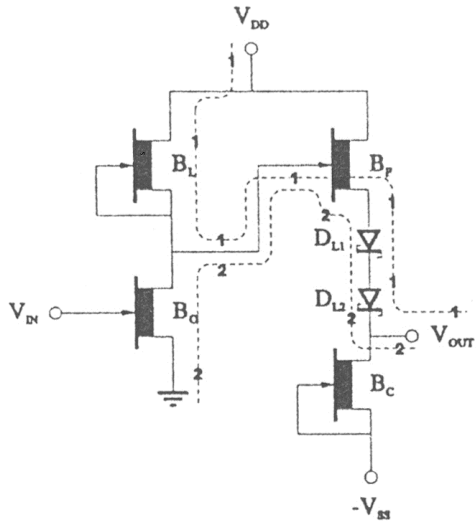


Fig.1 The BFL inverter

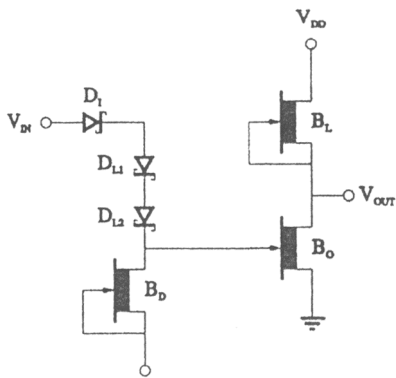


Fig.2 The SDFL inverter

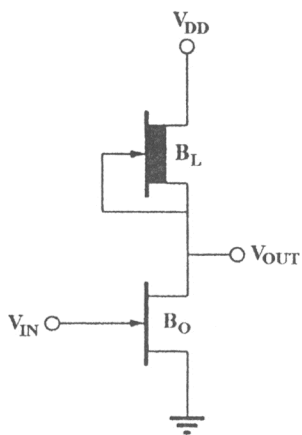


Fig.3 The DCFL inverter

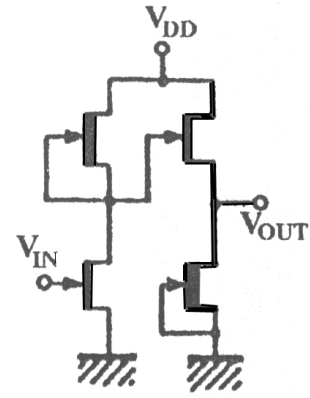


Fig.4 The BDCFL inverter

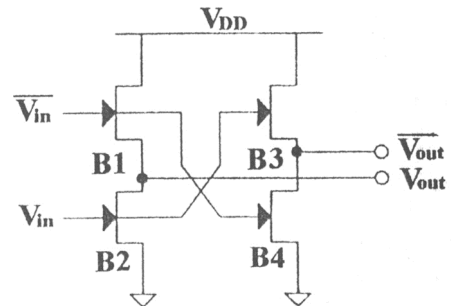


Fig.5 The PCFL inverter

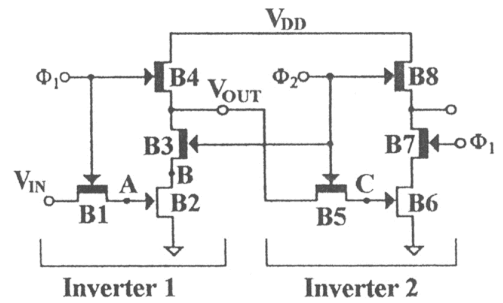


Fig.6 The TDFL inverter with unitary fan-out

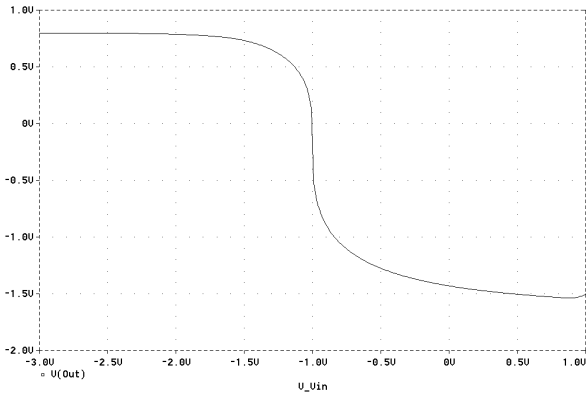


Fig.7 The BFL input-output characteristic

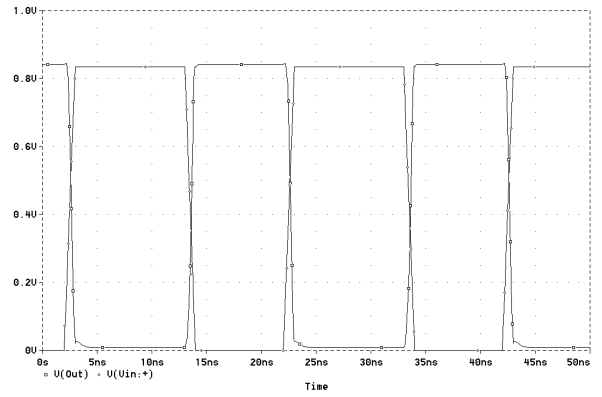


Fig.11 The BDCFL transient analysis

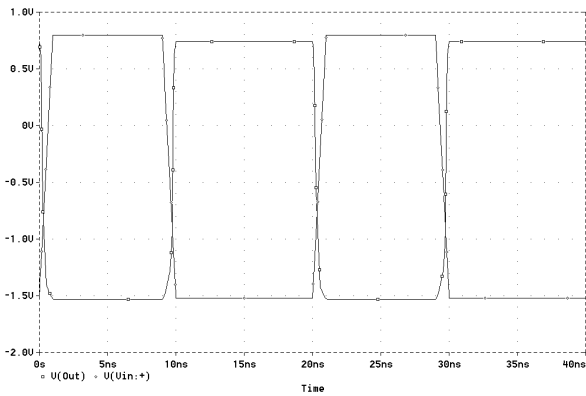


Fig.8 The BFL transient analysis

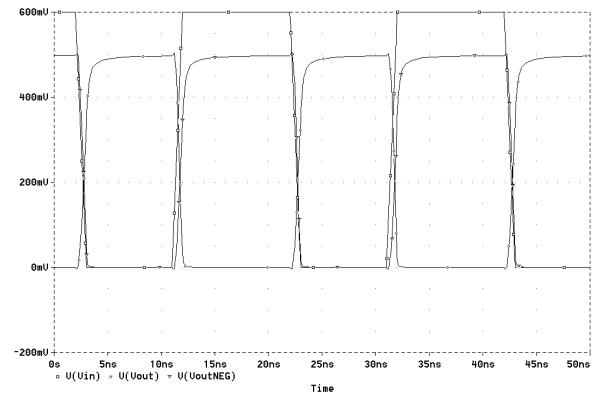


Fig.12 The PCFL transient analysis

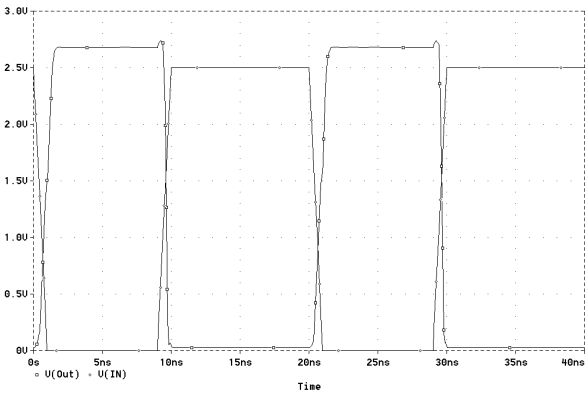


Fig.9 The SDFL transient analysis

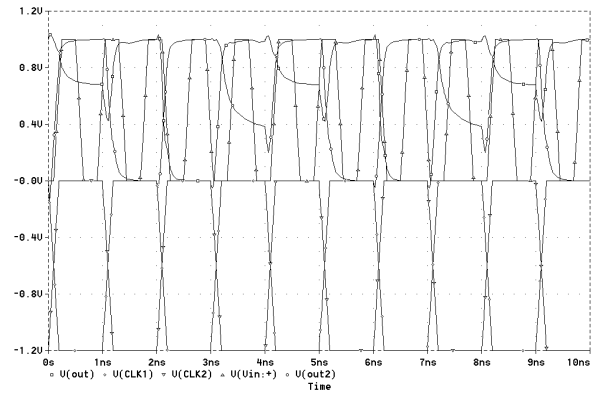


Fig.13 The TDFL transient analysis

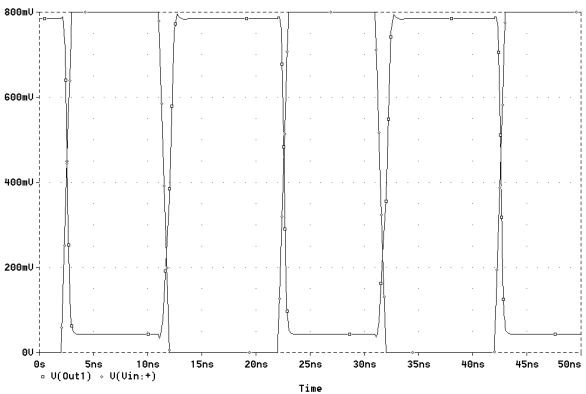


Fig.10 The DCFL transient analysis