Wireless RF Communication Based On TMS320c6713 DSP

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Abstract— In this paper we have presented a wireless Radio Frequency (RF) communication which is based on digital signal processor (DSP) TMS 320C6713. System can process data using DSP processor and transmits processed data using wireless RF module CM2025 which has the programmable carrier frequency in the range 2.3 GHz to 2.5 GHz. This system can use to modulate signals digitally and transmit data, audio and video signals over the wireless medium using wireless RF module. Binary Phase Shift Keying (BPSK) technique or Direct Sequence Spread Spectrum (DS/SS -BPSK) technique is used to for the modulation purpose.

Keywords— carrier ; radio frequency; DSP STAR personal; RF module; modulation;

I. INTRODUCTION

In the past years, we were used the wired technologies for the communication. These wired technologies have the greatest drawbacks of using cable. To overcome these drawbacks, we have been moved to the wireless one. By using the wireless communication technologies, we make our communication as cable free and reliable. The RF wireless communication, as the name suggests, operates at Radio Frequency (30 KHz - 300GHz), these are electromagnetic signal can travel through air medium and does not need line of sight communication. In wireless transmission of data, audio and video signals, in many cases the data which needs to be addressed and transmitted, these signals requires big quantity of data and complicated processing algorithms [1]. To meet this requirement we have used digital signal processor, which can process large data using parallel processing mechanism. Also DSP can perform fixed or floating point operations within fraction of seconds.

In this system ND Tech's DSP STAR Personal Board used as basic processing and controlling unit where, as ND Tech's RF wireless communication module CM2025 is used as wireless transceiver which can externally interfaced to DSP STAR Personal board via CPU expansion board. This board incorporated with TMS320C6713 which is Texas Instrument's DSP processor. It has complete control on wireless data module at the same time it can easily combine data processing and wireless transmission together. In this system data signals are digitally modulated using BPSK technique or its spectrum is spreaded using DS/SS BPSK technique. We can use programmable carrier frequency for modulation in range the 2.3GHz to 2.5GHz. Greatest advantage of this system is that we can use unlicensed ISM band (2.4GHz – 2.5GHz).

II. CIRCUIT DESIGN AND HARDWARE

A. Principle Block Diagram

The block diagram of wireless RF communication system is as shown in Figure 1. In this system TMS320C6713 DSP processor is which is 32 bit floating point. Processor performs basic operation and controls the transmission of data, voice and video siganal with the help of plug in RF wireless communication module which has two separate antennas for transmitter and receiver. The DSP processor controls or accesses the RF module through CPLD registers. CPLD register act as interface between processor and RF module, also used to store temporary data. Each section of block diagram is explained in detail in the subsequent section.

B. DSP STAR Personal Hardware Board

DSP STAR Personal hardware consists of two hardware components: DSP processor module and Input Output (I/O) board. Each DSP processor module is connected with the I/O board [4]. The C6713 is high performance, advanced very-long-instruction-word (VLIW) architecture it is excellent for multichannel and multifunction applications. It operates at 225MHz, the C6713 delivers up to 1350 million floating-point operations per second (MFLOPS).

The two I2C ports on the C6713 allow the DSP to easily control peripheral devices and communicate with a host processor. In addition, the standard multichannel buffered serial port (McBSP) may be used to communicate with serial peripheral interface (SPI) mode peripheral devices [6]. I/O board has CPU expansion port contains 16 bit data and address bus which is used to connect RF wireless module. Also I/O board has audio codec which is used to convert analog input at line in pin into 13 bit digital data, ADC, DAC, serial port and LCD display.
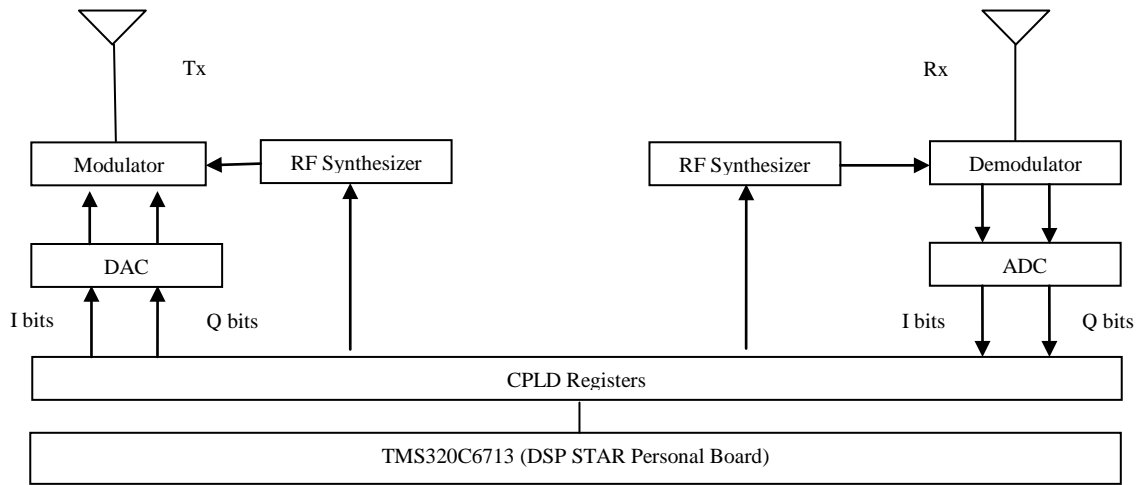
Fig. 1. Block diagram

C. RF wireless communication module

The RF Wireless Communications Module (CM2025) is a small electronics circuit used for radio communications, which allows users to use radio frequency from 2.3GHz to 2.5GHz. It has the Silicon Laboratories's RF synthesizer Si4136. The RF module contains both transmitter and receiver hardware including separate control logics in one hardware board. The module is a plug-in for DSP STAR Personal expansion port. It has 8 bit ADC and 8 bit DAC for each I and Q channel [3].

D. Interface between DSP STAR Personal Board and RF Communication

The RF module is connected to DSP hardware through CPU expansion port. Four address pins A0 ~ A3 are used as shown in table I.

TABLE I.　　CM2025 REGISTER ADDRESS MAP

A3~A0	Byte Address	Name	Description
0	EIOBASE1 + 0x0	CONTL	RF Synthesizer Control Register
1	EIOBASE + 0x4	RXADJ	Receive Carrier Frequency Adjust
2	EIOBASE + 0x 8	CONFG	Receive / Transmit Configuration Register
3	EIOBASE + 0x C	IQDAT	I/Q channel Data Register
4	EIOBASE + 0x 10	LEDCS	LED Chip Select
5~15	Reserved	.	.

There are five CPLD registers that control and access the RF wireless module. Registers CONTL, RXADJ, and CONFG are used to set up the RF synthesizer frequency, the ADC/DAC sampling rate, and the interrupt behavior. The IQDAT register is used for I and Q channel data transmissions [5].

III. WORKING PRINCIPLE

DSP processor is used as basic processing and controling unit in this syetem. Processor stores program for different algorithems in its memory and process the data based on algorithm witch is to be implement. Processed data is transmitted through the RF module's transmitting section and received through receiver section. Transmitter and receiver sections are described in detail in following sections.

A. Transmitter

Initially DSP processor sets up the parameters of the RF synthesizer (*Si4136*) at a transmitter side by setting the values of N and R register along with phase detector gain register (Kb) and their corresponding values are given in table II. Generated carrier is mathematically given as follows.

$$RFout = (19.2MHz)2N / R \tag{1}$$

TABLE II.　　SET UP VALUES OF KP AND R REGISTERS

N Value	Kp	R
992 ~ 4095	0	7 ~ 8189
4096 ~ 8191	1	8 ~ 8189
8192 ~ 16383	2	10 ~ 8189
16383 ~ 262143	3	14 ~ 8189

Digital data is separated into 8 bit I and Q channels, then each channel signal is converted into analog signal using at DAC converter (AD9763) and fed into RF modulator (AD8346). The RF modulator generates an orthogonal signal

corresponding to a carrier signal generated from the RF synthesizer, and multiplies these two orthogonal carrier signals by I and Q channel data. These two signals are added and output is transmitted via TX antenna. AD9763 used is dual channel, 8 bit CMOS DAC.

a) RF synthesizer Si4136

The Si4136 is a monolithic integrated circuit that performs both IF and RF synthesis for wireless communications applications. The Si4136 includes three Voltage Controlled Oscilators (VCO), loop filters, reference and VCO dividers, and phase detectors. Divider and power down settings are programmable through a three-wire serial interface.
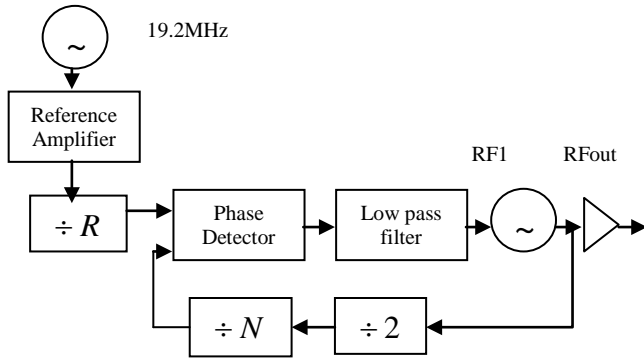
Fig. 2. RF synthesizer

Temperature Compensated Crystal Oscillator (TCXO) clock input to phase locked loop generates a carrier signal in frequency range of 2.3 ~ 2.5 GHz. Two values R and N of internal register can be used to change a frequency. An output frequency is fed back and compared with a reference frequency for more accurate carrier signal.The reference frequency is divided by R and the divided frequency is divided again by 2N. The resulting clock inputs to phase detector. The phase detector computes a difference of two frequencies to generate a pulse. The generated pulse is passed through a low pass filter and converted into voltage. Then the converted voltage inputs to the VC port of RF1 to generate an output radio frequency [3].

b) Quadrature Modulator AD8346

The AD8346 is a silicon RFIC I/Q modulator for use from 0.8 GHz to 2.5 GHz. Its excellent phase accuracy and amplitude balance allow high performance direct modulation to RF.Modulator generates a signal orthogonal to receiving carrier signal from RF synthesizer. Then, multiplies two analog signals coming from I and Q channels by two orthogonal carrier signals, respectively.

B. Receiver

The DSP processor drives the receiver RF synthesizer (Si4136) to generate a carrier signal. Receiver RF synthesizer is same as transmitter one. The received signal at RX antenna enters RF demodulator (AD8347). The RF demodulator generates an orthogonal signal to a carrier signal coming from

the RF synthesizer, and multiplies each of these two carrier signal by a received signal. Multiplied signals are separated into I and Q channels. After that separated I and Q signals are converted into digital data using ADC (AD9281) converter, which is 8 bit ADC. The resulting digital data is stored at the CPLD data register called IQDAT. The DSP reads data from the CPLD register. The CPLD register RXADJ is used to change a driving voltage at the VC port of the receiver TCXO. change in voltage causes change in an input clock of RF synthesizer and in carrier frequency [3].

a) Quadrature Demodulator AD8347

The AD8347 is a broadband direct quadrature demodulator with RF and baseband Automatic Gain Control (AGC) amplifiers. It is suitable for use in many communications receivers, performing quadrature demodulation directly to baseband frequencies. The input frequency range is 800 MHz to 2.7 GHz. It generates signal orthogonal to incoming carrier and then two orthogonal carrier signals multiplied to incoming RF signal. It generates I and Q channel output signals, respectively.

IV. MATHEMATICAL MODELLING

A. BPSK Transmitter

BPSK is the digital modulation technique in which phase of carrier signal changes according to input binary data signal. Transmitter section modulates the signal using BPSK technique and transmites through transmitting antenna as given in (2). f_T is the trasmitter carrier frequency.

$$S_m(t) = A_T\{m_I(t)\cos(2\pi f_T t) + m_Q(t)\cos(2\pi f_T t - \frac{\pi}{2})\}$$

(2)

Where, $S_m(t)$ is the BPSK modulated message signal, A_T is amplitude of modulated signal, $m_I(t)$ and $m_Q(t)$ are quadrature shifted components.
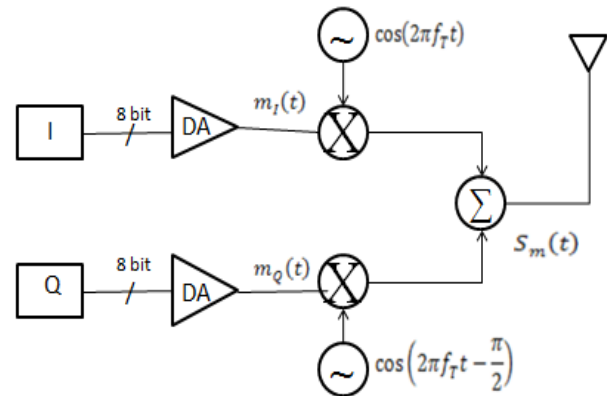

Fig. 3. BPSK transmitter structure

B. BPSK Receiver

Coherent detection is used for demodulation. Receiving antenna receives the transmitted signal $S_m(t)$ along with channel random noise $N(t)$ as given in (3).

$$S'_m(t) = S_m(t) + N(t) \tag{3}$$
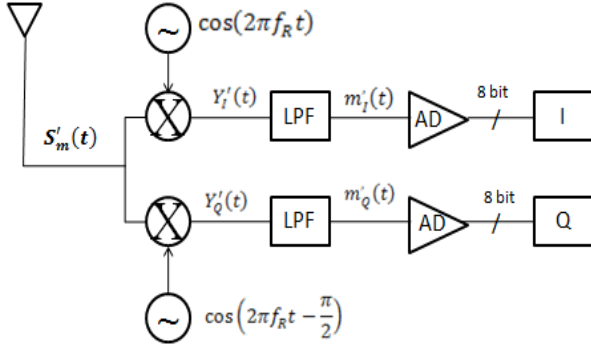
Where, $S'_m(t)$ is the received signal.

Fig. 4. BPSK receiver structure

For I channel,

$$Y'_I(t) = \{S_m(t) + N(t)\}A_R \cos(2\pi f_R t) \tag{4}$$

Where, f_R is the receiver carrier frequency.
Here, it is assumed that channel is noise free i.e $N(t) = 0$

$$Y'_I(t) = S_m(t) A_R \cos(2\pi f_R t)$$
$$= A_T A_R \{m_I(t)\cos(2\pi f_T t) + m_Q(t)\cos(2\pi f_T)\}\cos(2\pi f_R t)$$
$$= \frac{1}{2} A_T A_R [m_I(t)\{\cos(2\pi(f_T - f_R)t)$$
$$+ \cos(2\pi(f_T + f_R)t)\} + m_Q(t)\{\sin(2\pi(f_T - f_R)t) + \sin(2\pi(f_T + f_R)t)\} \tag{5}$$

Let us substitute $f_T - f_R = \Delta f$ in (5) and applied to low pass filter, output of low pass filter is given in (6).

$$\{Y'_I(t)\}_{LPF} = m'_I(t)$$
$$= \frac{1}{2} A_T A_R [m_I(t)\cos(2\pi\Delta f) + m_Q(t)\sin(2\pi\Delta f)] \tag{6}$$

When transmitted signal and received signal has the same carrier frequency i.e. $f_T = f_R$ then $\Delta f = 0$ hence (6) becomes

$$\{Y'_I(t)\}_{LPF} = \frac{1}{2} A_T A_R m_I(t) \tag{7}$$

For Q channel,

$$Y'_Q(t) = \{S_m(t) + N(t)\}A_R \cos(2\pi f_R t - \frac{\pi}{2}) \tag{8}$$

As N(t)=0

$$= S_m(t) A_R \cos(2\pi f_R t - \frac{\pi}{2}) \tag{9}$$

$$= A_T A_R \{m_I(t)\cos(2\pi f_T t) + m_Q(t)\sin(2\pi f_T t)\}\cos(2\pi f_R t - \frac{\pi}{2})$$

$$= \frac{1}{2} A_T A_R [m_I(t)\{\sin(2\pi(f_T - f_R)t) + \sin(2\pi(f_T + f_R)t)\} + m_Q(t)$$
$$\{\cos(2\pi(f_T - f_R)t) - \cos(2\pi(f_T + f_R))\}]$$

As $\Delta f = f_T - f_R$

$$\{Y'_Q(t)\}_{LPF} = m'_Q(t)$$
$$= \frac{1}{2} A_T A_R [m_I(t)\cos(2\pi\Delta ft) + m_Q(t)\sin(2\pi\Delta ft)] \tag{10}$$

As $\Delta f = 0$ for same carrier frequency of transmitted and received signal (10) becomes,

$$\{Y'_Q(t)\}_{LPF} = \frac{1}{2} A_T A_R m_Q(t) \tag{11}$$

we get the I and Q bits as given in (7) and (11) .

V. SOFTWARE INTERFACE

Code Builder is a compiler that allows the user to write code, compile/link, debug, execute on DSP STAR personal board and control the hardware. The Code Builder also provides environments for code generation and a number of tools C source break point, symbol view, watch window, disassembly view, memory view,edit,copy,fill, register view, flash memory read/write, and graphical view that help the user debug the programs and control the hardware [4].

VI. RESULTS

A. Reception of RF Carrier Signal(2.4 GHz)

Two sets of DSP STAR hardware with RF antenna,one set as transmitter and other as receiver is used.At transmitter set pllN to 120000, pllR to 1920 and Kp to 3. At receiver side we use frequency tunning, for different frequency tunning time graph of received signal are shown in Figure 5 and 6.
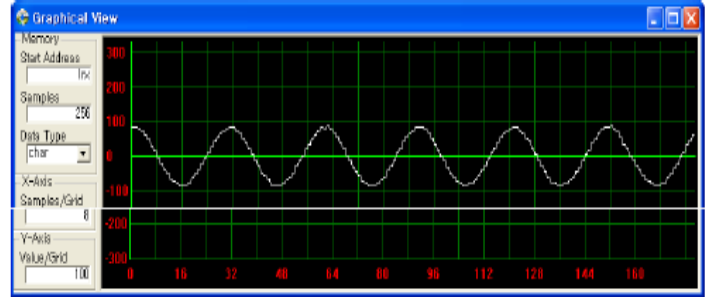

Fig. 5. Time graph of received data after frequency tunning at 20 KHz
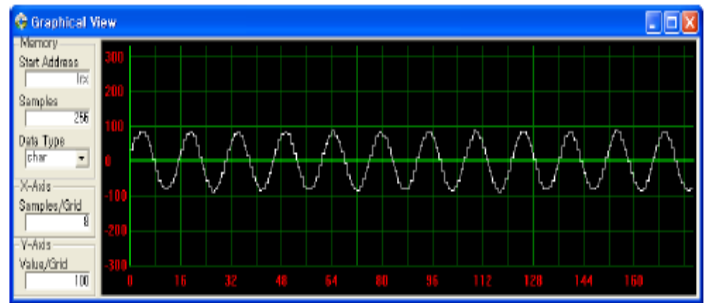

Fig. 6. Time graph of received data after frequency tunning at 40 KHz

B. Fine Tuning of Receiver Carrier

We can fine tune a receiver carrier frequency by choosing optimum value of RXADJ register such that frequency difference between two modules is minimised.

Waveforms for different values of RXADJ are as shown in Figure 7. For 2.4 GHz carrier we get fine tunning at value 15 of RXADJ register.
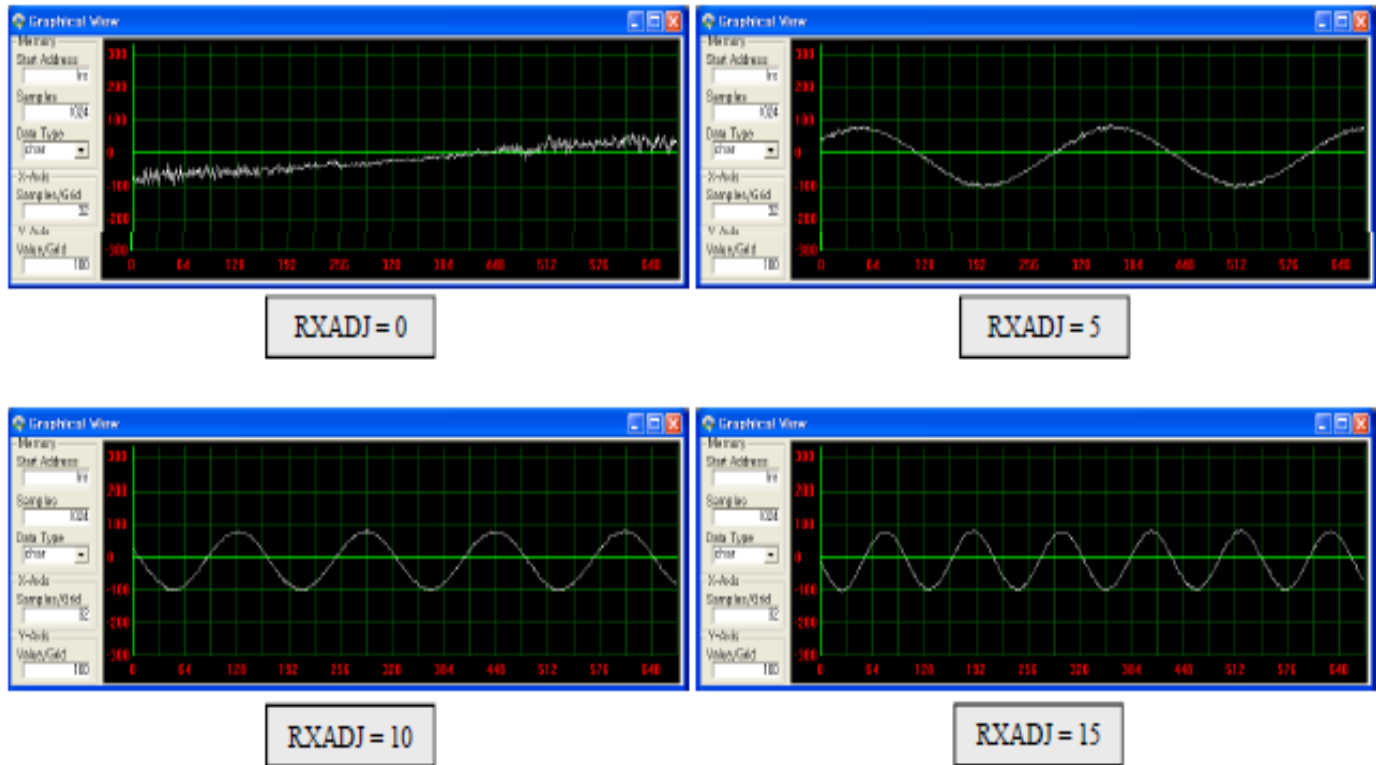

RXADJ = 0

RXADJ = 5

RXADJ = 10

RXADJ = 15

Fig. 7. Change in waveforms according to RXADJ register

C. Reception of BPSK Signal

Data is binary in BPSK and phase of carrier signal vary according to data value. Coherent detection is used for demodulation. Received BPSK signal graph is as shown in Figure 8.
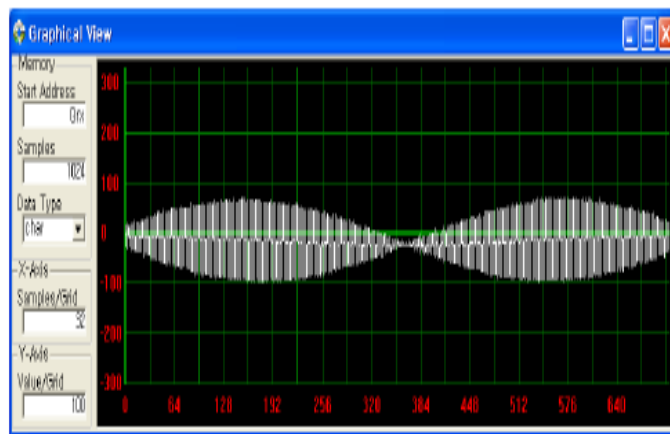

111Fig. 8. Received BPSK signal

D. Constellation Diagram for Received BPSK Signal

A constellation diagram represents a digital-modulated signal in a two-dimensional complex plane. Modulated carrier $S_m(t)$ is divided into in-phase (I) and quadrature (Q) components, expressed as complex signal.
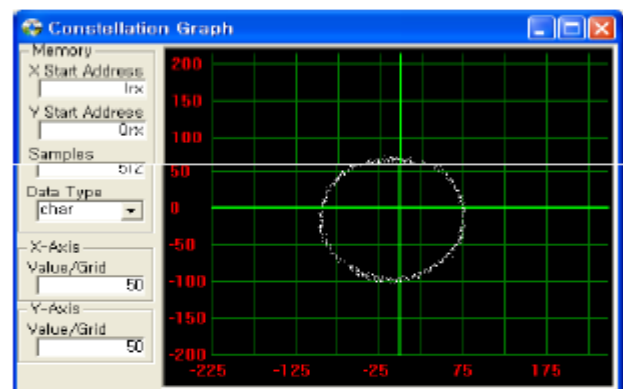

Fig. 9. Constellation diagram before compensation

Before Compensation

On x-axis I components and y-axis Q components are presented. Signal constellation rotates due to carrier synchronization between two boards. Offset of received signal is due to AD8347 demodulator and AD9281 AD converter. After compensating offset we get optimised results. Before and after compenesation graphs are as shown in Figure 9 and 10 respectively.
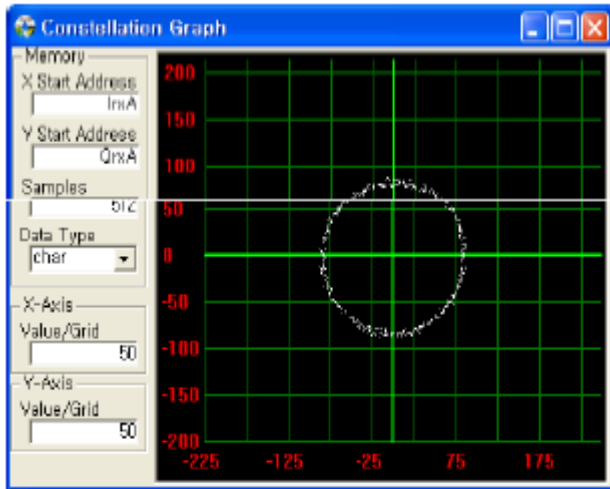

Fig. 10. Constellation diagram after compensation

CONCLUSION

This paper has presented an alternative solution for RF communication using DSP STAR personal board and plugged in RF module. RF communication does not require direct transmission path as IR. This paper has presented broad overview of RF wireless communication using DSP processor. Floating point DSP processor reduces overall computation time, system complexity and enhances performance of system with increased reliability. Using DS/SS -BPSK modulation technique we can make communication more secure.

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