A Multimode Reconfigurable FFT Processor Design

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Abstract: -This paper designed and implemented a multimode FFT processor for WLAN/WPAN system applications. In the design, we used a multi-path delay feedback structure, approach the FFT processing point configurable multi-mode, and the processor is capable of handling different points for WPAN and WLAN applications, capable of handling up to 512 points FFT operation at 300MHz, it also achieves the performance targets required by the respective application environment. Simulation results show that compared with the general Xilinx IP, this design has greatly improved the power consumption and chip area of the FFT processor.

Key-Words: Multimode, Reconfigurable, FFT, wireless network, WPAN, WLAN

1 Introduction

Wireless network develops rapidly in recent years, and gets more and more popularity. Nowadays it plays an important role in digital signal processing technology. Fast Fourier Transform (FFT) is a digital signal processing algorithm. There is much demand of FFT processor for a variety of applications on the market. In Orthogonal Frequency Division Multiplexing (OFDM)system, a fast Fourier transform is the key data transmission processing module in modulation and demodulation, FFT processor require to process more FFT points, needs better real-time, more flexibility, and lower power consumption.

Firstly, this paper analyses common algorithms of discrete Fourier transform and fast Fourier transform then several FFT algorithms are compared in resource consumption and operational efficiency. After that this paper discusses the proposed base-2^m flexible point optimization algorithm for flexibly configurable hardware design. In addition this design determines to select the structure of multi-path delay feedback to implement multi-mode reconfigurable FFT processor design. In this FFT processor, the twiddle factor requires a lot of computation. So this paper chooses the Coordinate Rotation Digital Computer (CORDIC) module to perform this function, which reduces the complexity of the complex multiplication, and also this paper proposed a corresponding optimized structure. In order to reach the throughput requirement of Wireless Personal Area Networks (WPAN) network, this paper design a 8-way parallel processing architecture, it can work at the highest processing frequency of 309.789MHz to achieve 2.478GS/s data throughput. This FFT processor can work in Wireless Local Area Networks (WLAN) mode to achieve 64/128-points FFT processing of spatial streams; WPAN mode to achieve 128/256/512-points FFT processing. Finally, this paper uses FPGA of Vertex-6 and MATLAB 7.0 to co-simulation the multimode reconfigurable processor design for FFT computation correctness, and through the ISE Xpower Analyser to verify low-power-consumption of the system which is very significant for further improvement.

2 Specification and Considerations

Figure1 shows the system block diagram of multimode reconfigurable FFT processor, which consists of WMAN mode processing module and WLAN mode processing module. As shown in figure 2-1, the WMAN signals, WLAN signals are sent to the corresponding synchronization unit, and then these signals can be sent into the FFT processor.

After the data is sent to the processor to complete operation, and then it will be sent to

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the frequency domain equalizer. The design will used in the area of WLAN IEEE 802.11n [1] and WPAN IEEE 802.15.3c [2] standard applications, the FFT mode for WMAN applications are given in Table 1. The FFT mode for WPAN applications are given in Table 2.

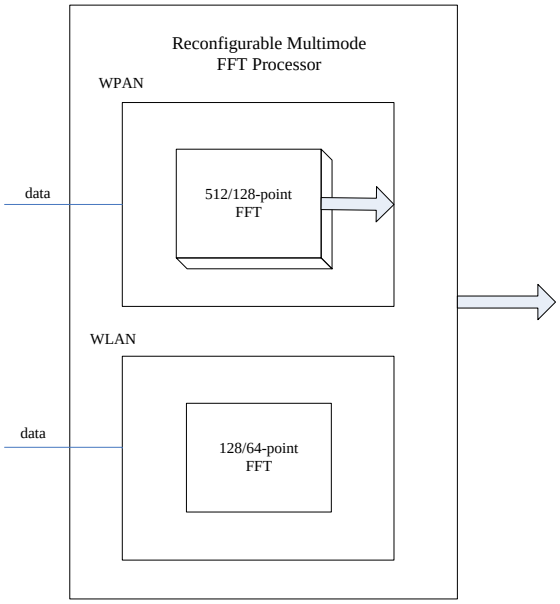

Fig.1 system block diagram of multimode reconfigurable FFT processor

Table1. FFT mode for WPAN applications

FFT size	Input Word length	Specified Throughput
128	10 bit	320MS/s
256	10 bit	1.0GS/s
512	10 bit	2.4GS/s

Table2. FFT mode for WLAN applications

FFT size	Input Word length	Specified Throughput
64	10 bit	20MS/s
128	10 bit	40MS/s

As can be seen from the above two tables, multimode FFT processor design not only to handle the FFT processing 64/128/256/512 points, but also to ensure the normal operation at a frequency of 300MHz. So it requires that the selection FFT algorithm need to be flexible. For achieved technical route mainly refers to different FFT size and input bits wide length. The throughput to be achieved by the corresponding algorithm, in which some parts can be reused, so using this feature we can implement reconfigurable hardware design. This design needs to reach the WPAN mode speeds up to 300MHz, the data throughput reached 2.4GS/s [3][4].

3 Algorithm

Fast Fourier Transform is the conventional techniques for signal change from the time domain to the frequency domain.in communication technology [3].

$$X(k)=\sum_{n=0}^{N-1}x(n)W_N^{kn}, k=0,1,...,N-1 \qquad (1)$$

Where $x(n)$ and $X(k)$ are complex numbers. In the FFT algorithm, Cooley-Tukey algorithm is the most famous algorithm. The basic principle of this algorithm is to divide long DFT into short DFT. For example, sequence length $N=N_1N_2$, then this long sequence is transformed into length N_1 sequence and length N_2 sequence. By using the FFT algorithm, the computational complexity can be reduced. The most famous application for Cooley-Tukey algorithm is r-2 FFT implementation. While the basic idea of Cooley-Tukey algorithm is recursive calculation method, most conventional algorithm will rewrite explicit recursive algorithm for non-recursive form [5]. In addition, since the Cooley-Tukey DFT algorithm is divided into a plurality of smaller DFT length, so it can be used with any other combination of the DFT algorithm.

The design in this paper uses a base-2 FFT, but it is not the usual r-2 butterfly algorithm. The design uses a two-stage FFT algorithm processing module to achieve a flexible point configuration. The following is the details of this algorithm [6].

Now a 512-points discrete Fourier transform (DFT) is defined as (2):

$$X(k)=\sum_{k=0}^{511}x(n)W_{512}^{nk} \qquad k=0,1,2,...,511 \qquad (2)$$

$$\begin{cases} n = 32n_1 + n_2, & n_1 = 0,1,2,...,15; n_2 = 0,1,2...,31 \\ k = k_1 + 16k_2, & k_1 = 0,1,2,...,15; n_2 = 0,1,2...,31 \end{cases} \quad (3)$$

In (2) $W_{512}^{nk} = e^{-j(2\pi nk/512)}$ is the twiddle factor, formula (2) can expressed as formula (4) by formula (3), like this the 512-points FFT operation is divided into two levels, one is DFT processing r-16 and the other one is r-32 .

$$\begin{aligned} X(k) &= \sum_{n_2=0}^{31}\sum_{n_1=0}^{15} x(32n_1+n_2)W_{512}^{(32n_1+n_2)(k_1+16k_2)} \\ &= \sum_{n_2=0}^{31}\{[\sum_{n_1=0}^{15} x(32n_1+n_2)W_{16}^{n_1k_1}]W_{512}^{n_2k_1}\}W_{32}^{n_2k_2} \end{aligned} \quad (4)$$

Then the r-16 operations need 4 steps of r-2 operation. Similarly, the r-32operation can be realized by 5 steps of r-2 operation. Thus the original 512-points FFT can be calculated using the r-16/32 algorithm.

4 The proposed structure

The designed reconfigurable FFT processor works in a variety of network environments. Since the conventional FFT processor architecture cannot reach MIMO-OFDM high throughput and low hardware consumption requirements. In order to achieve adequate data throughput, we use a multi-channel parallel processing method. FFT processor design can be used in MIMO-OFDM system, the implementation architecture shown in fig.2. The system architecture consists of the following modules. In fig.2 the white arrows mean the data channel, solid arrows represent the configure channel.

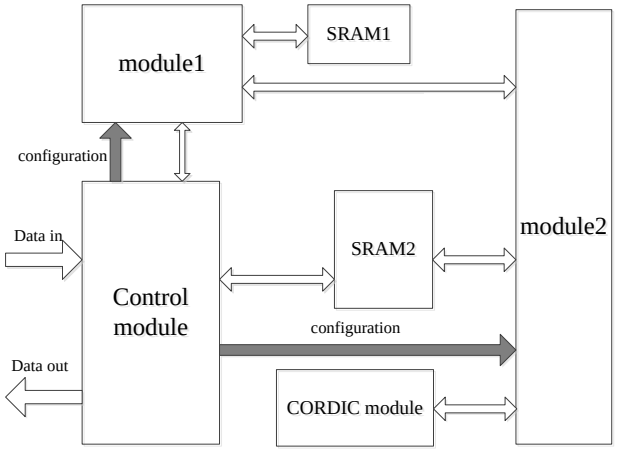

Fig.2 The processor system block diagram

Control module is responsible for controlling the input and output sequence of data, and configuring the working mode of module1 and module2. It also controls state machine conversion, mode allocation, data allocation and other functions.

Module1 is mainly responsible for four stages butterfly-2 operation, and the number of operations controlled by reconfigurable control module configuration.

Module2 is responsible for five stages butterfly-2 operation, the number of operations can also be carried out by the control module reconfigurable configuration.

CORDIC module is a special module. In the calculation process of the FFT processor, the data is multiplied by twiddle factor, we use CORDIC algorithm to implement the design for the multiplication by the twiddle factors. The smaller part of the twiddle factors we choose directly look-up table method which store the data in the memory. This module completes the hardware processing CORDIC algorithm.

SRAM1 is a storage module. The sram is composed by FIFOs. FIFO is generated by corresponding DesignWare IP core. The implementation method is the outside of FIFOs wrapped in a layer, the external interface are rst_n (reset signal), almostfull (full signal), almostempty (almost empty signal), full (full signal), empty (empty signal), readreq (read request signal), writereq (write request signal), chipselect (chip select signal), datain (write data), dataout (read data), clk (clock), etc., the interface varies depending on the actual situation. SRAM2's function is similar with SRAM1, and it also realizes the function of FIFO.

The design uses the Flexible Radix Configuration Multipath Delay Feedback (FRCMDF) structure , specific hardware implementation block diagram shown in fig.3.

The structure is divided into two parts: module1 and module2, module1 contains a 4 stages of r-2 processing (Stage1 ~ 4) and module2 contains 5 stages of r-2 processing (Stage5 ~ 9). In order to achieve different point FFT processing, module1 and module2 required for each stage of reconfiguration according to the algorithm

described above. So the required flexible point FFT processing can be achieved through the multimode MDF structure [7]. Test module responsible for the input signal string conversion and output signals, and test module is a part of the control module in the RTL design. It is mainly composed by two 64 depth of FIFOs, and the FIFO controller.

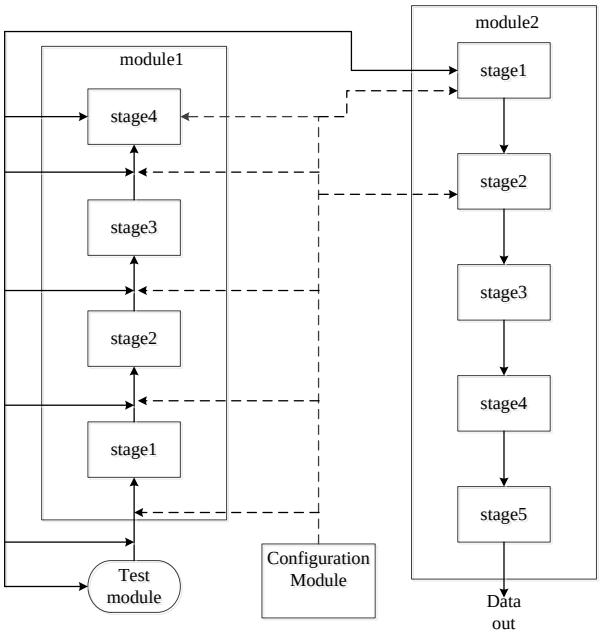

Fig.3 FRCMDF hardware block diagram

Fig.4 is the state machine of the control module.

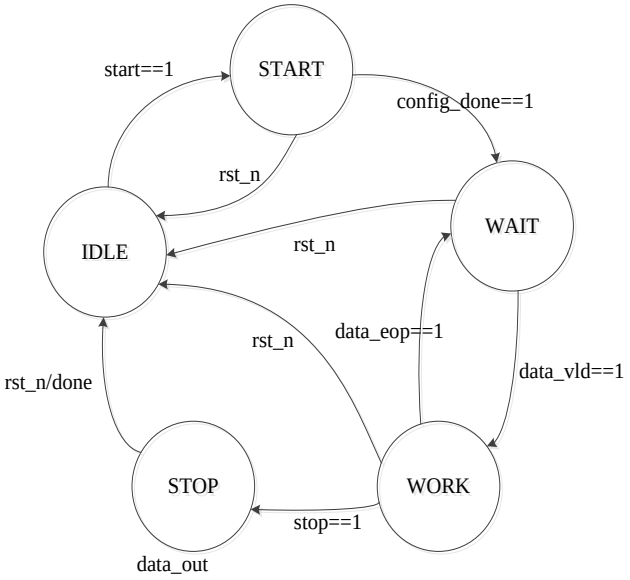

Fig.4 Multimode FFT processor operation processing state transition diagram

A detailed description about the mentioned state transition diagram is given below.

IDLE：This state is the initial state after the system is powered up. In this condition, system is waiting for the input of the environment variable change, and when the system environment is determined (WPAN / WLAN /WMAN), the system jumps from the IDLE state to the STAR state.

START： This state is configured processor operating mode, if rst_n signal is effective, state machine will jump back to IDLE state. This state is responsible for the configuration work in WPAN/WLAN environment; configuration the using FIFO size. Configuration process takes about 5 to 8 clock cycles. After the configuration is complete, processor jumps to WAIT state.

WAIT：This state is waiting for input data. The WAIT state need two cycle to start data transmission, and then state machine will jump to WORK state. If there is no data input, it must stay in current state.

WORK ： This state is FFT operation processing, after processing a set of data, state machine will jump to WAIT state waiting for the next set of input data, the system is reset back to the IDLE state.

STOP： In this state, the FFT processor has completed the calculate operation. The calculation results can be stored in memory, while processor will clean FIFO and RAM, in order to ensure treatment for the next operation. After a period of time system will jump to IDLE state.

5 Experimental Results

The verification for this design using Synopsys' Modelsim simulation software, simulation uses 512-point discrete excitation signal as input data, the high bits for the real part and the imaginary part is the low bits. For multi-channel FFT processor architecture of this

design, it can handle 8 data each cycle, and therefore the FFT processor complete 512 points operation needs 64 cycles to get the results; the data structure includes a real part and an imaginary part. Finally we use ISE as EDA development tool for the design of FFT processor to complete logic synthesis and backend layout, and also the timing of processor power and hardware resources are analysed. For the area and power consumption, we use Design Compiler to comprehensive. To evaluate the proposed FFT processor, the comparison between the proposed FFT processor and Xilinx IP [8][9] based on Xpower analyser. The performance summary is shown in the following tables.

Table.3 DC comprehensive report

Report	area
Design	fft_top
Version	G-2012.06-sp2
Date	Fri Sep 4 16:21:59 2014
Number of ports	324
Number of nets	440
Number of cells	6
Number of references	6
Combinational area	8438.880059
Buf/Inv area	2398.560082
Non combinational area	614197.712448
Total cell area	622636.592507

Table.4 Power consumption comparison of FFT processor and FFT IP

Top-level Entity Name	xilinx_fft	fft_top
Family	Vertex-6	Vertex-6
Device	XC6VLX240T	XC6VLX240T
Power Models	Final	Final
Total Thermal Power Dissipation	920.13mW	683.06mW
Core Dynamic Thermal Power Dissipation	237.23mW	164.99mW
Core Static Thermal Power Dissipation	513.14mW	492.05mW
I/O Thermal Power Dissipation	169.76mW	26.02mW

From the above table it can be seen that the design of FFT processor processing 512 points data at clock frequency of 300MHz shows a higher performance. Compared with the FFT IP this design reduces power consumption [10].

6 Conclusion

In this paper, a design for WLAN/WPAN applications multimode FFT processor that supports high throughput 64/128 points FFT processing in WLAN network environment and 64/128/256/512 points in WPAN network environment. Compared to the traditional FFT processor, the proposed FFT processor reduces the area and power consumption, and supports a variety of data processing mode. Finally, compared to Xilinx IP the performance of this design has greatly improved in energy efficiency and functional diversification. This design has a high social value and practical significance for the study of FFT processor.

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