Analytical Modeling and Characterization of TSV for Three Dimensional Integrated Circuits

G.SUBHASHINI¹, J.MANGAIYARKARASI²
¹PG scholar, M.E VLSI design,
² Faculty, Department of Electronics and Communication Engineering,
Anna University, Regional Centre, Madurai.
INDIA.
gsubhaam@gmail.com, mangaice@autmdu.in

Abstract — In this paper, the operation of S-G pair TSV, coaxial TSV, tapered S-G pair TSV and tapered coaxial TSV are analyzed where the TSV resistance, inductance, and capacitance need to be modeled to find out their impact on the performance of a 3-D circuit. The RLC parameters of the TSV are modeled as a function of physical factor and material characteristics. The performance of the analytically modeled TSV in the form of lumped elements (R, L, and C) circuit was simulated using Virtuoso Schematic editor and Analog Design Environment of Cadence Tool. Delay crosstalk and power are determined and compared between various TSV structures. The delay has been reduced in tapered coaxial TSV structure compared with other types of TSV structure.

Key-Words: - 3D ICs, TSV, RLC, coaxial TSV, S-G pair TSV, tapered TSV, cadence tool.

1 Introduction

Three dimensional integrated circuits (IC) in the form of three-dimensionally stacked chips is the most capable technology for the design of ICs and system with high performance, functionality, device packing density and lower power utilization [2] than those designed by the conventional 2D technologies. 3D ICs are gifted for mixed integration of different technologies (logic, memory, RF, analog) [1] which would enable high performance and compact SOC.

Fig.1 Three Dimensional integration

Compared to the conventional two dimensional integration with one active layer, the three dimensional integration [6] with multiple active layers is efficient to enlarge integration level and improve performance. The electrical performance of 3D IC integration is better than that of 2D due to short wiring. 3D integration supports higher levels of integration for a given area. RLC models are used for TSVs and power/ground networks.

This study presents a comprehensive delay and crosstalk analysis for 3-D integrated systems. Cylindrical power/ground TSVs and coaxial TSVs are investigated as means to ease delay and crosstalk issues in 3-D integration [3]. The coaxial TSV can be the paramount TSV structure in electrical performance, and its basic configuration has a central signal-carrying conductor surrounded by a concentric ground return. Due to the shielding effect of ground shell, coaxial TSV has intrinsically higher noise immunity than that of paired TSVs [8].

1.1 TSV model

Through silicon vias (TSVs) are necessary elements for achieving miniaturized [5] 3D integrated systems. The fabrication of 3D stacked IC involves stacking of one or more chips, and the TSV constitutes a key component for interconnecting chips vertically so that they occupy less space and have a great connectivity. It is a high performance technique to create 3D packages and 3D ICs.
The force of TSV on the 3-D circuit performance needs to be evaluated, and there have been attempts to illustrate the resistance and capacitance of TSV. TSVs are fabricated after FEOL and before BEOL processing [1] and permit the interconnection involving the bottom tier and top tier.

![Fig.2](image)

Fig.2 (a) C TSV model, (b) RC TSV model, (c) RLC TSV model

Fig 2 shows the basic RLC, RL and C TSV model [4]. The electrical characteristics such as delay and crosstalk of a 3-D stacked chip, parasitic modeling and signal transmission characteristics of a TSV are analyzed. TSV resistance, inductance, and capacitance are modeled built by means of TSV RLC parameter is then approximated to form a simple lumped TSV model. First-order expressions for $R_{TSV}$, $C_{TSV}$, and $L_{TSV}$ as a function of physical parameters and material characteristics are derived and validated with numerical simulators.

2. Uniform TSV

The three dimensional integrated circuits are implemented with (uniform radius) cylindrical and coaxial TSV, where the cylindrical TSV structure introduces some crosstalk issues and delay. These problems can be eliminated by using coaxial TSV structure. Uniform TSV radius is 1um.

![Fig.3](image)

Fig.3 Uniform TSV

2.1 S-G pair TSV

![Fig.4](image)

Fig 4 shows the cylindrical S-G pair TSV structure and its equivalent lumped-element circuit model of the three dimensional integrated circuits.

### 2.1.1 Equations for S-G pair TSV

The analytical expression for the resistance of the TSV [1] is given by

$$R = \frac{\rho L}{A}$$  \hspace{1cm} (1)

Where $\rho$ is the resistivity of the conducting material. $L$ and $A$ represents the length and area of the TSV respectively.

$$A = \pi (d/2)^2$$  \hspace{1cm} (2)

$$d = D - 2t$$  \hspace{1cm} (3)

The analytical model and Cadence simulations show very good agreement for different TSV architectures. The TSV capacitance is the series combination of the insulation and depletion capacitance. The depletion and insulation capacitance [1] are given by

$$C_{DEP} = \frac{2\pi \varepsilon_i L}{\ln \left( \frac{D}{d} \right)}$$  \hspace{1cm} (4)

$$C_{INS} = \frac{2\pi \varepsilon_{si} L}{\ln \left( \frac{DEP}{d} \right)}$$  \hspace{1cm} (5)

$$C = \frac{C_{INS}C_{DEP}}{C_{INS} + C_{DEP}}$$  \hspace{1cm} (6)
Where $\varepsilon_i$ and $\varepsilon_{si}$ are the dielectric constant of insulator and the dielectric constant of silicon, respectively. The inductance \[1\] of the TSV depends upon the diameter and length of the TSV. It is given by the following expression:

$$L_{\text{TSV}} = \frac{\mu_0}{4\pi} \left[ 2l_{\text{TSV}} \ln \left( \frac{2l_{\text{TSV}} + \sqrt{r_{\text{TSV}}^2 + (2l_{\text{TSV}})^2}}{r_{\text{TSV}}} \right) \right]$$

$$+ r_{\text{TSV}} \sqrt{r_{\text{TSV}}^2 + (2l_{\text{TSV}})^2}$$

Where $\mu_0$ is the permeability of free space given by $4\pi \times 10^{-7}$, $l_{TSV}$ and $r_{TSV}$ represents the length and radius of the TSV, respectively. The analytical model and Cadence simulations show very good agreement for different TSV architectures.

### 2.1.2. Simulation results for S-G pair TSV

**a) Transient Response capacitance(nF)**

![Transient Response capacitance(nF)](image1)

**b) Transient Response capacitance(pF)**

![Transient Response capacitance(pF)](image2)

**c) Transient Response capacitance(fF)**

![Transient Response capacitance(fF)](image3)

Fig. 5 illustrates the transient response of various capacitance ranges, when the S-G TSV pair performs the necessary signal transmission under nano farad and pico farad ranges, it will introduce more crosstalk problem. The best TSV structure should propose the signal transmission without any correlation of noises, whereas the S-G TSV structure can generate the better result only in femto farad range. So that the need for elimination of noise in all the required ranges, move on to the coaxial TSV structure.

**Fig. 6 Delay measurement**

The signal ground pair TSV is implemented between ten tier system then the input signal is given to the three dimensional integrated circuit, it can be observed that the S-G TSV structure introduces more delay and power.
2.2 Coaxial TSV

Fig.7 Equivalent lumped-element circuit model of the coaxial TSV interconnect

Fig 7 shows the equivalent lumped circuit model for the three dimensional integrated circuits.
Length of the TSV: L
Outside diameter of inner conductor: a
Inside diameter of the shield: b
Dielectric constant: $\varepsilon$
Magnetic permeability: $\mu$

2.2.1 Equations for coaxial pair TSV

The analytical expression for the resistance [8] of the TSV is given by

$$R = \frac{1}{2\pi\sigma[a]} + \frac{1}{2\pi\sigma[b]} - [8]$$

The variation of resistance shows the expected linear inverse relationships with radius and conductivity respectively.
The TSV capacitance [8] is given by

$$C = \frac{l_{TSV}2\pi \varepsilon_0 \varepsilon_r}{\ln\left(\frac{D}{d}\right)} - [9]$$

As both radius and length increase, capacitance increases monotonically. The inductance [8] of the TSV depends upon the diameter and length of the TSV and it is given by the following expression:

$$L = \frac{\mu_0 l_{TSV}}{2\pi} \left(\frac{D}{d}\right) - [4.10]$$

Where $\mu_0$ is the permeability of the free space.$l_{TSV}$ and $r_{TSV}$ represents the length and radius of the TSV, respectively. TSV inductance increases with increasing length, but decreases with increasing radius, as predicted by the analytic formulation of inductance for an isolated conductor.

2.2.2 Simulation result for coaxial TSV

a) Transient Response capacitance (nF)

b) Transient Response capacitance (pF)

c) Transient Response capacitance (fF)

Fig 8 shows transient response for coaxial TSV structure with various capacitance ranges. Due to the shielding effect of ground shell, coaxial TSV has intrinsically higher noise immunity than that of signal ground paired TSVs [8].
The root cause is that the coaxial TSV capacitance is almost constant, whereas the capacitance of the S-G TSV pair decreases with the increasing frequency because isolation layer capacitance and
Si substrate capacitance become series connections at high frequency [8]. In general, coaxial TSV electrical characteristics depend on its conductor/dielectric materials and geometries.

The signal ground pair TSV is implemented between ten tier system then the input signal is given to the three dimensional integrated circuit, it can be observed that the S-G TSV structure introduces more delay and power.

3. Tapered TSV

![Fig.10 Tapered TSV](image1)

The power and delay can be reduced with the help of tapered TSV. The tapered TSVs can be a potential solution for mitigating power and delay issues in 3-D integration. The number of TSVs remains unchanged but their radiuses vary from one tier to another tier. Tapered TSVs radiuses are: 1µm, 2µm, 3µm, 4µm, 5µm, 6µm, 7µm, 8µm, 9µm.

![Fig.11 Tapered S-G pair TSV](image2)

![Fig.12 Tapered coaxial TSV](image3)

Fig 11, 12 shows the delay measurement of tapered TSV. The impact of $R_{TSV}$ and $C_{TSV}$ on the TSV delay can be analyzed with the help of S-G pair TSV structure and coaxial TSV structure. The delay measurements with worst case TSV, best case TSV and without TSVs are analyzed in [9].

<table>
<thead>
<tr>
<th>TSV structure</th>
<th>Delay</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-G pair TSV</td>
<td>2.15 ns</td>
<td>0.78*10^{-9}</td>
</tr>
<tr>
<td>Tapered S-G TSV</td>
<td>1.6 ns</td>
<td>-0.9*10^{-9}</td>
</tr>
<tr>
<td>Coaxial TSV</td>
<td>1.2 ns</td>
<td>-1.5*10^{-9}</td>
</tr>
<tr>
<td>Tapered coaxial TSV</td>
<td>931ps</td>
<td>-2.8*10^{-9}</td>
</tr>
</tbody>
</table>

**Table 1. Performance of various TSV**

Table 1 shows that the tapered coaxial TSV offers better performance compared with other structures.

5. Conclusion

In this work the three dimensional integrated circuits are implemented with different types of TSV structures, where the S-G pair TSV structure introduces more cross talk issues and delay. Due to
the shielding effect of ground shell, coaxial TSV has intrinsically higher noise resistance than that of paired TSVs. Delay and crosstalk are evaluated and compared between coaxial TSV and signal ground TSV pair. For analytical modeling of the three dimensional integration the TSV structure is designed with ten active layers, where the 50% of delay and crosstalk has been reduced using coaxial TSV structure.

REFERENCES


